

Features

- Wide Supply Voltage Range: 4.5V to 20V
- Guaranteed 2A continuous load current
- 2% 0.6V reference
- Cycle-by-cycle peak current limitation
- Instant PWM architecture to achieve fast transient responses Internal softstart limits the inrush current
- Current Limiting Protection
- Low RDS(ON) for internal switches (top/bottom):90/70 mΩ
- Fixed 1MHz Switching Frequency
- RoHS and Halogen free compliance
- Compact package: SOT23-6

Applications

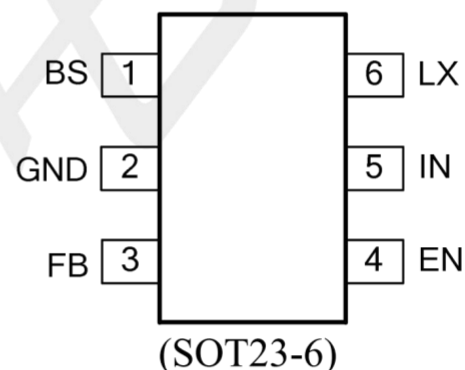
- Networking
- IP CAM
- LCD TV
- DSL Modem
- Access Point Router
- Digital TV
- Set Top Box

Pin Configurations

General Description

develops high efficiency synchronous step down DC-DC converter capable of delivering 2A load current . operates over a wide input voltage range from 4.5V to 20V and integrates main switch and synchronous switch with very low RDS(ON) to minimize the onduction loss. adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 1MkHz under heavy load conditions to minimize the size of inductor and capacitor.

Pinout (top view)



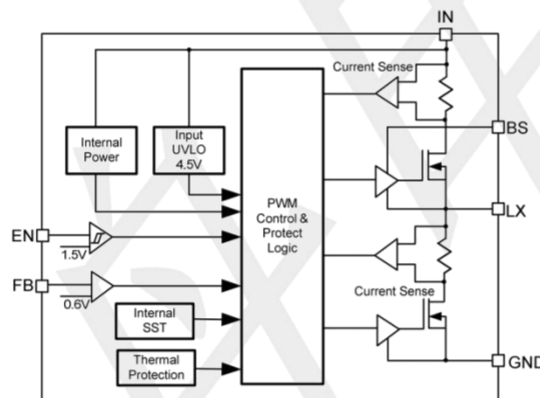
Pin Number	Pin Name	Pin Function
1	BS	Boot-Strap Pin. Supply high side gate driver. Decouple this pin to LX pin with 0.1uF ceramic cap.
2	GND	Ground pin.
3	FB	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{out}=0.6*(1+R1/R2)$.
4	EN	Enable control. Pull high to turn on. Do not float.
5	IN	Input pin. Decouple this pin to GND pin with at least 1uF ceramic cap.
6	LX	Inductor pin. Connect this pin to the switching node of inductor.

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VIN	Continuous input voltage range	-0.3	20	V
LX	LX voltage range	-0.3	VIN+0.3V	
EN	EN pin voltage range	-0.3	VIN+0.3V	
FB, BS-LX	FB, BS-LX pin voltage range	-0.3	4	W
PD	PD @ TA = 25°C SOT23-6	0.6		
LT	Lead Temperature (Soldering, 10 sec.)	260		°C
Temperature	Junction Temperature, TJ	-40	125	
	Storage, Tstg	-65	150	
θJA	Thermal Resistance from Junction to ambient		170	°C/W
θJC	Thermal Resistance from Junction to case		75	

BLOCK DIAGRAM



Typical Application Circuit

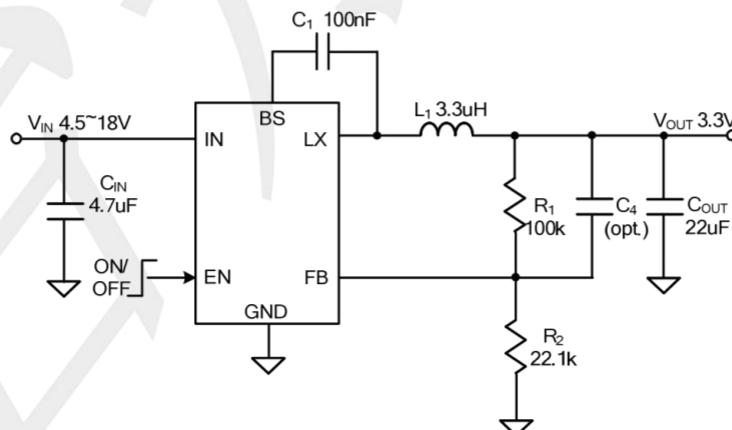


Figure 1. Schematic Diagram

Electrical Characteristics

(VIN = 12V, VOUT = 3.3V, L = 3.3uH, COUT = 22uF, TA = 25°C, IOU = 1A, unless otherwise specified)

PARAMETER	SYMBOL	TEST Conditions	MIN	TYP	MAX	UNIT
Supply Voltage	VIN		4.5	--	18	V
Quiescent Current	IQ	VIN=12V,VOUT=3.3V No Load	--	410	--	uA
Shutdown Current	ISHDN	EN=0	--	5	10	uA
Feedback Reference Voltage	VREF		0.588	0.6	0.612	V
FB Input Current	IFB	VFB=VIN	-50	--	50	nA
Top FET RON	RDS(ON)1		--	90	--	mΩ
Bottom FET RON	RDS(ON)2		--	70	--	mΩ
TOP FET Peak Current Limit	ILIM, TOP		--	3	3.6	A
Bottom FET Valley Current Limit	ILIM, BOTTOM		2	--	--	A
EN Threshold	VIL	Low Voltage	0.5	--	--	V
	VIH	High Voltage	--	--	2	V
EN Input Current	ISINK	VEN From 0V to 2V	--	1	--	uA
Input UVLO Threshold	VUVLO		--	--	4.4	V
Switching Frequency	FSW		--	1	--	MHz
Min ON Time			--	50	--	nS
Min Off Time			--	100	--	nS
Soft-start Time	tSS		--	200	--	nS
Thermal Shutdown Threshold	TSD	Enabled	--	150	--	°C
Thermal Shutdown Hysteresis	THYS	VOUT = 0V	--	20	--	°C

Note 1: Stresses beyond “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

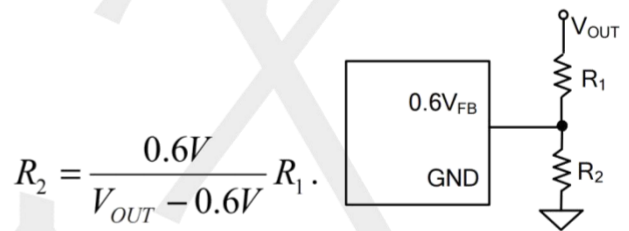
Note 2: The device is not guaranteed to function outside its operating conditions.

Function Description

Because of the high integration in the IC, the application circuit based on this regulator IC is rather simple. Only input capacitor CIN, output capacitor COUT, output inductor L and feedback resistors (R1 and R2) need to be selected for the targeted applications specifications.

Feedback resistor dividers R1 and R2

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If Vout is 3.3V, R1=100k is chosen, then using following equation, R2 can be calculated to be 22.1k:



Input capacitor CIN

The ripple current through input capacitor is calculated as:

$$I_{CIN_RMS} = I_{OUT} \cdot \sqrt{D(1-D)}$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by CIN, and IN/GND pins. In this case, a 4.7uF low ESR ceramic capacitor is recommended.

Output capacitor COUT

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor greater than 22uF capacitance.

Output inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT} (1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where Fsw is the switching frequency and IOUT,MAX is the maximum load current. The regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

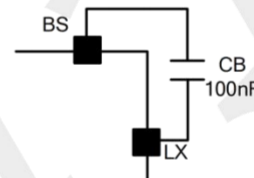
2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT, MIN} > I_{OUT, MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with $DCR < 50m\Omega$ to achieve a good overall efficiency.

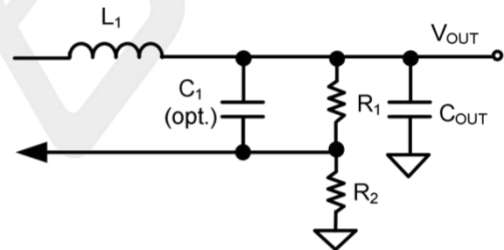
External Bootstrap Cap

This capacitor provides the gate driver voltage for internal high side MOSEFET. A 100nF low ESR ceramic capacitor connected between BS pin and LX pin is recommended.



Load Transient Considerations

The regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22pF ceramic cap in parallel with R1 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.

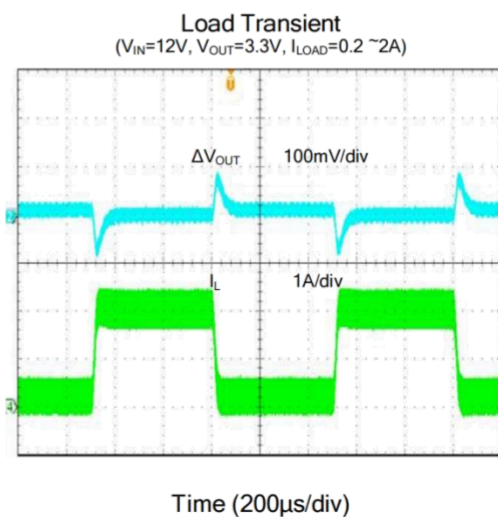
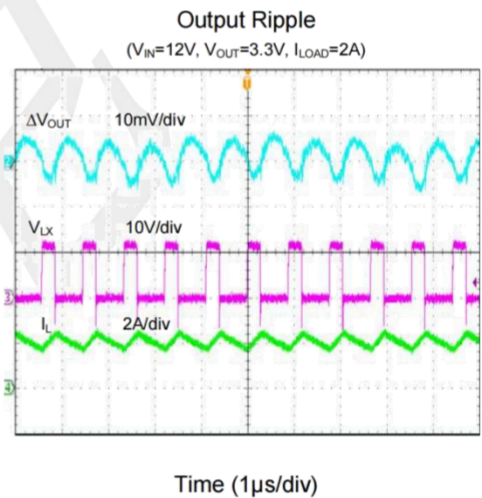
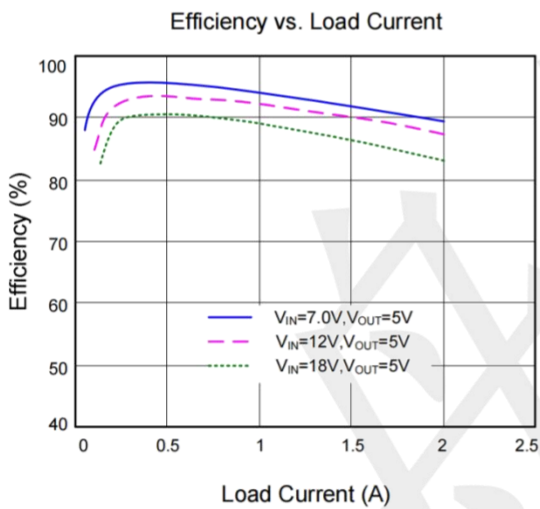
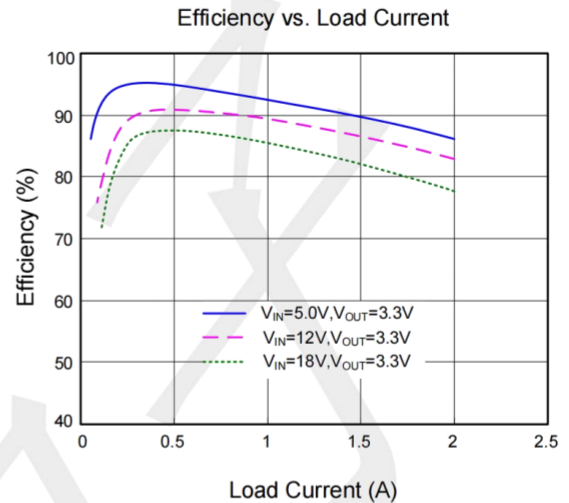
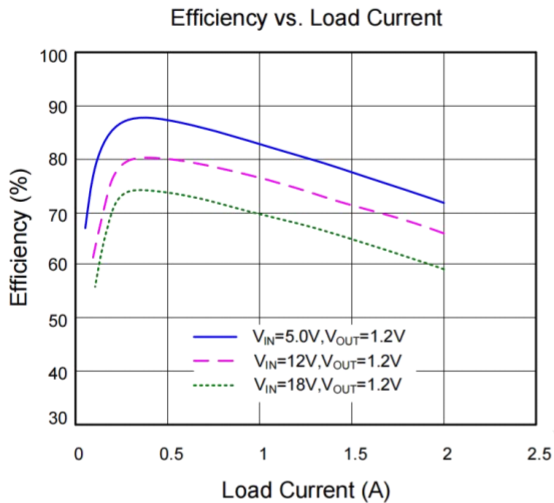


Layout Design

The layout design of regulator is relatively simple. For the best efficiency and minimum noise problem, we should place the following components close to the IC: CIN, L, R1 and R2.

- 1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
- 2) CIN must be close to Pins IN and GND. The loop area formed by CIN and GND must be minimized.
- 3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
- 4) The components R1 and R2, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.
- 5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

Typical Operating Characteristics



Package information

SOT23-6

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	0.035		0.057
A1	0		0.10	0		0.004
A2	0.90		1.30	0.035		0.051
b	0.35		0.50	0.014		0.02
C	0.09		0.20	0.004		0.008
D	2.80		3.05	0.110		0.120
E	1.50		1.75	0.059		0.069
e		0.95			0.037	
H	2.60		3.00	0.102		0.118
L	0.10		0.60	0.004		0.024
θ	0°		10°	0°		10°

Suggested Land Pattern(mm)

