# UMW OPA2333/OPA333

1.8-V, microPower, CMOS Operational Amplifiers, Zero-Drift Series

## 1.Description

The UMW OPA2333,OPA333 series of CMOS operational amplifiers use a proprietary auto-calibration technique to simultaneously provide very low offset voltage (10 μV, maximum) and near-zero drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the rails, and rail-to-rail output that swings within 50 mV of the rails. Single or dual supplies as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V) can be used. These devices are optimized for low-voltage, single-supply operation.

The OPAx333 family offers excellent CMRR without the crossover associated with traditional complementary input stages. This design results in superior performance for driving analog-to-digital converters (ADCs) without degradation of differential linearity.

The OPA333 (single version) is available in the 5-pin SOT-23, SOT, and 8-pin SOP packages, while the OPA2333 (dual version) is available in the 8-pin SOP packages. All versions are specified for operation from -40°C to 125°C.

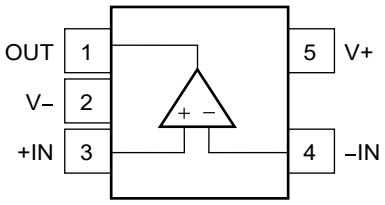
## 2.Features

- Low Offset Voltage: 10μV(Maximum)
- Zero Drift: 0.05 μV/°C (Maximum)
- 0.01-Hz to 10-Hz Noise: 1.1$\mu V_{PP}$
- Quiescent Current: 17μA
- Single-Supply Operation
- Supply Voltage: 1.8V to 5.5V
- Rail-to-Rail input/Output
- microSize Packages: SC70 and SOT23

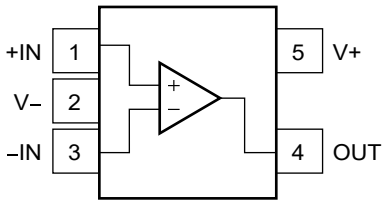
## 3.Applications

- Transducers
- Temperature Measurements
- Electronic Scales
- Medical instrumentation
- Battery-Powered Instruments
- Handheld Test Equipment

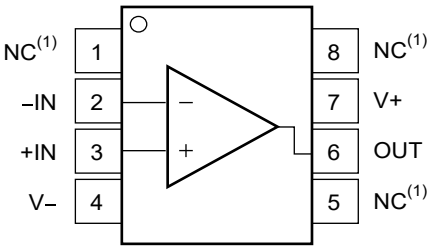
## 4.1 Pinning Information (OPA333)




SOT23-5




SC70-5

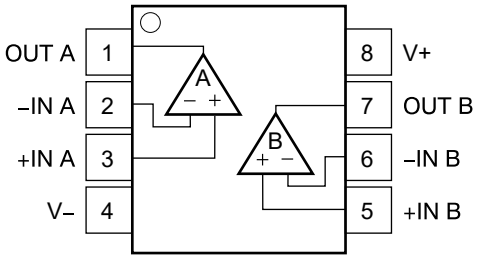



SOP-8

Pin Functions

| PIN | | | | I/O | Description |
|---|---|---|---|---|---|
| Name | SOP | SOT | SC70 | | |
| +IN | 3 | 3 | 1 | I | Noninverting input |
| -IN | 2 | 4 | 3 | I | Inverting input |
| NC | 1,5,8 | - | - | - | No internal connection (can be left floating) |
| OUT | 6 | 1 | 4 | O | Output |
| V+ | 7 | 5 | 5 | - | Positive (highest) power supply |
| V- | 4 | 2 | 2 | - | Negative (lowest) power supply |

## 4.2 Pinning Information (OPA2333)




**SOP-8**

Pin Functions

| PIN | | I/O | Description |
|---|---|---|---|
| Name | SOP | | |
| +IN | - | I | Noninverting input |
| +INA | 3 | I | Noninverting input, channel A |
| +INB | 5 | I | Noninverting input, channel B |
| -IN | - | I | Inverting input |
| -INA | 2 | I | Inverting input, channel A |
| -INB | 6 | I | Inverting input, channel B |
| OUT | - | O | Output |
| OUTA | 1 | O | Output, channel A |
| OUTB | 7 | O | Output, channel B |
| V+ | 8 | - | Positive (highest) power supply |
| V- | 4 | - | Negative (lowest)power supply |

## 5.Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| Parameter | | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| Voltage | Supply voltage | | | 7 | V |
| | Signal input terminals (2) | | -0.3 | (V+)+0.3 | V |
| Current | Signal input terminals (2) | | -1 | 1 | mA |
| | Output short circuit (3) | | Continuous | | |
| Operating junction temperature | | $T_J$ | | 150 | °C |
| Operating temperature | | $T_A$ | -40 | 150 | °C |
| Storage temperature | | $T_{STG}$ | -65 | 150 | °C |

Notes:

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.

(3) Short-circuit to ground, one amplifier per package

## 6.ESD Ratings

| Parameter | | Symbol | Value | Units |
|---|---|---|---|---|
| Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | $V_{(ESD)}$ | ±4000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | | ±1000 | V |

Notes:

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| Parameter | Min | Max | Units |
|---|---|---|---|
| Supply voltage, $V_S$ | 1.8 | 5.5 | V |
| Specified temperature | -40 | 125 | °C |

## 8.1 Thermal Information (OPA333)

| Thermal Metric (1) | Symbol | D(SOIC) | DBV(SOT) | DCK(SC70) | Units |
|---|---|---|---|---|---|
| | | 8 Pins | 5 Pins | 5 Pins | |
| Junction-to-ambient thermal resistance | $R_{\theta JA}$ | 140.1 | 220.8 | 298.4 | °C/W |
| Junction-to-case (top) thermal resistance | $R_{\theta JC(top)}$ | 89.8 | 97.5 | 65.4 | °C/W |
| Junction-to-board thermal resistance | $R_{\theta JB}$ | 80.6 | 61.7 | 97.1 | °C/W |
| Junction-to-top characterization parameter | $\psi_{JT}$ | 28.7 | 7.6 | 0.8 | °C/W |
| Junction-to-board characterization parameter | $\psi_{JB}$ | 80.1 | 61.1 | 95.5 | °C/W |
| Junction-to-case(bottom)thermal resistance | $R_{\theta JC(bot)}$ | - | - | - | °C/W |

## 8.2 Thermal Information (OPA2333)

| Thermal Metric (1) | Symbol | D(SOP) | Units |
|---|---|---|---|
| | | 8 Pins | |
| Junction-to-ambient thermal resistance | $R_{\theta JA}$ | 124 | °C/W |
| Junction-to-case (top) thermal resistance | $R_{\theta JC(top)}$ | 73.7 | °C/W |
| Junction-to-board thermal resistance | $R_{\theta JB}$ | 64.4 | °C/W |
| Junction-to-top characterization parameter | $\psi_{JT}$ | 18 | °C/W |
| Junction-to-board characterization parameter | $\psi_{JB}$ | 63.9 | °C/W |
| Junction-to-case(bottom)thermal resistance | $R_{\theta JC(bot)}$ | - | °C/W |

## 9.Electrical Characteristics

At $T_A$=+25°C, $R_L$=10kΩ connected to $V_S$ / 2, $V_{CM}$=$V_S$/2, and $V_{OUT}$=$V_S$/2, unless otherwise noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| Input offset voltage | $V_{OS}$ | $V_S$=5V | | 2 | 10 | μV |
| Input offset voltage drift | $dV_{OS}/dT$ | $T_A$=-40°C to 125°C | | 0.02 | 0.05 | μV/°C |
| Power-supply rejection ratio | PSRR | $V_S$=1.8V to 5.5V,$T_A$=-40°C to 125°C | | 1 | 5 | μV/V |
| Long-term stability (1) | | | See note (1) | | | μV |
| Channel separation, dc | | | | 0.1 | | μV/V |
| **INPUT BIAS CURRENT** | | | | | | |
| Input bias current | $I_B$ | $T_A$=25°C | | ±70 | ±200 | pA |
| | | $T_A$=-40°C to 125°C | | ±150 | | pA |
| Input offset current | $I_{OS}$ | | | ±140 | ±400 | pA |
| **NOISE** | | | | | | |
| Input voltage noise | | f=0.01Hz to 1Hz | | 0.3 | | $μV_{PP}$ |
| | | f=0.1Hz to 10Hz | | 1.1 | | $μV_{PP}$ |
| Input current noise | $i_n$ | f=10Hz | | 100 | | fA/√Hz |
| **INPUT VOLTAGE** | | | | | | |
| Common-mode voltage range | $V_{CM}$ | | (V-)-0.1 | | (V+)+0.1 | V |
| Common-mode rejection ratio | CMRR | (V-)-0.1V<$V_{CM}$<(V+)+0.1V<br>$T_A$=-40°C to 125°C | 106 | 130 | | dB |
| **INPUT CAPACITANCE** | | | | | | |
| Differential | | | | 2 | | pF |
| Common-mode | | | | 4 | | pF |
| **OPEN-LOOP GAIN** | | | | | | |
| Open-loop voltage gain | $A_{OL}$ | (V-)+100mV<$V_O$<(V+)-100mV<br>$R_L$=10kΩ, $T_A$=-40°C to 125°C | 106 | 130 | | dB |
| **FREQUENCY RESPONSE** | | | | | | |
| Gain-bandwidth product | GBW | $C_L$=100pF | | 350 | | kHz |
| Slew rate | SR | G=+1 | | 0.16 | | V/μs |

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | |
| Voltage output swing from rail | | $R_L$=10kΩ | | 30 | 50 | mV |
| | | $R_L$=10kΩ, $T_A$=-40°C to 125°C | | | 70 | mV |
| Short-circuit current | $I_{SC}$ | | | ±5 | | mA |
| Capacitive load drive | $C_L$ | | See Typical Characteristics | | | |
| Open-loop output impedance | | f=350kHz, $I_O$=0A | | 2 | | kΩ |
| **POWER SUPPLY** | | | | | | |
| Specified voltage range | $V_S$ | | 1.8 | | 5.5 | V |
| Quiescent current per amplifier | $I_Q$ | $I_O$=0A | | 17 | 25 | μA |
| | | $T_A$=-40°C to 125°C | | | 28 | μA |
| Turn-on time | | $V_S$=5V | | 100 | | μs |
| **TEMPERATURE** | | | | | | |
| Specified range | $T_A$ | | -40 | | 125 | °C |
| Operating range | | | -40 | | 150 | °C |
| Storage range | $T_{STG}$ | | -65 | | 150 | °C |

(1) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately 1μV.

## 10.1 Typical characteristic

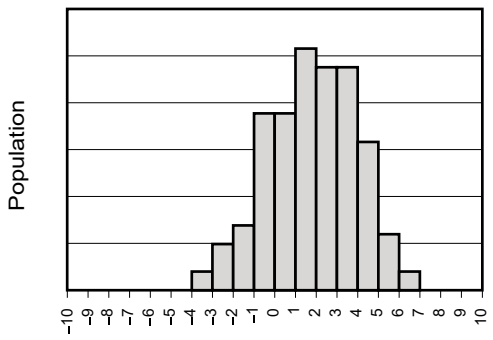



Figure 1: Offset Voltage Production Distribution

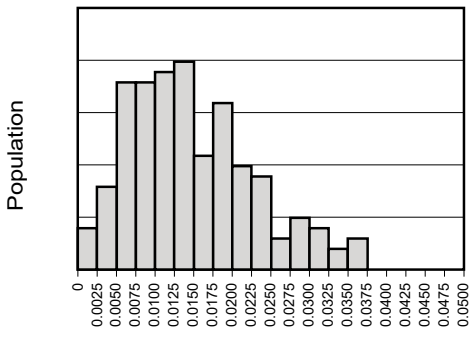



Figure 2: Offset Voltage Drift Production Distribution

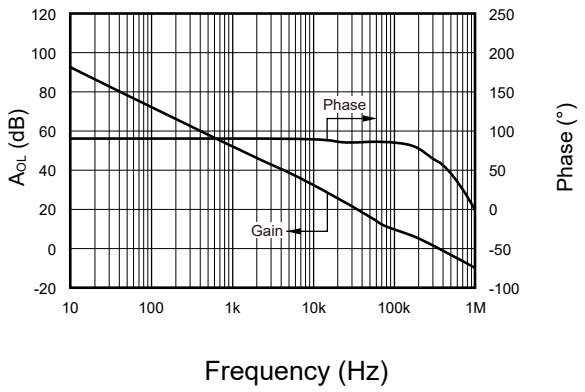



Figure 3: Open-Loop Gain and Phase vs Frequency

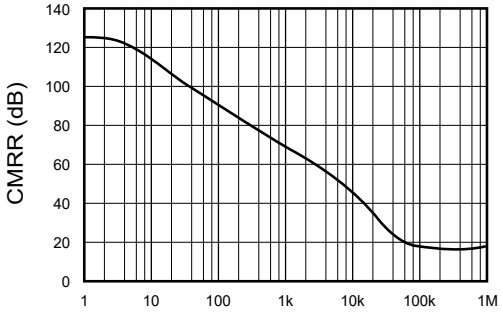



Figure 4: Common-Mode Rejection Ratio vs Frequency

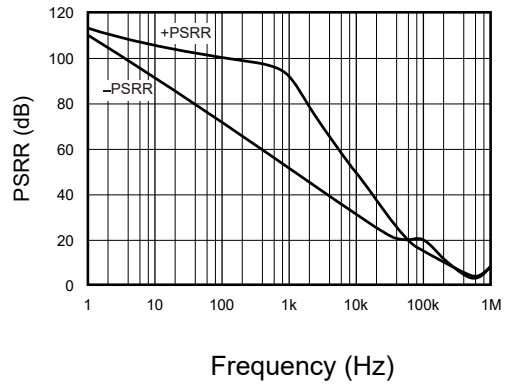



Figure 5: Power-Supply Rejection Ratio vs Frequency

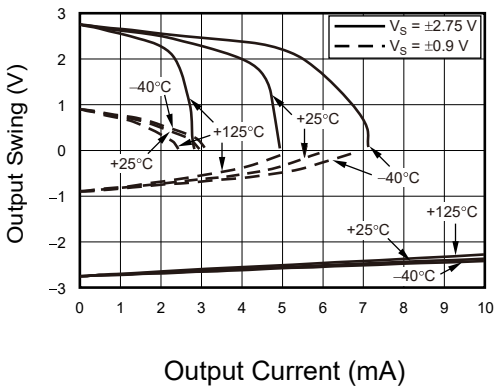



Figure 6: Output Voltage Swing vs Output Current

## 10.2 Typical characteristic

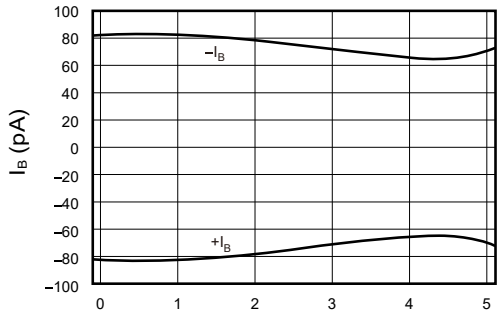



Figure 7: Input Bias Current vs Common-Mode Voltage

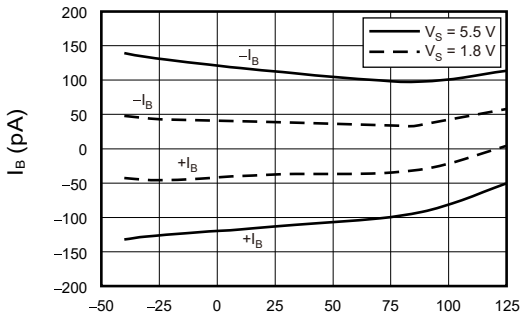



Figure 8: Input Bias Current vs Temperature

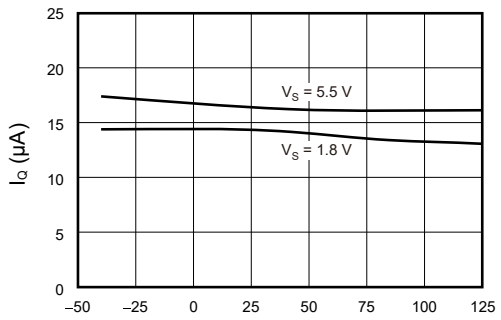



Figure 9: Quiescent Current vs Temperature

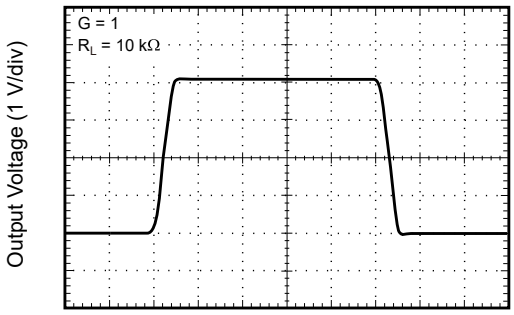



Figure 10: Large-Signal Step Response

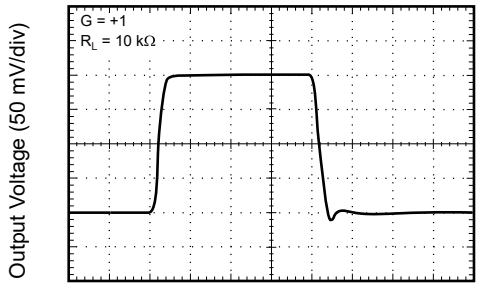



Figure 11: Small-Signal Step Response

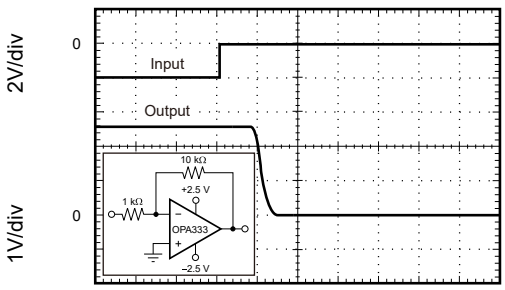
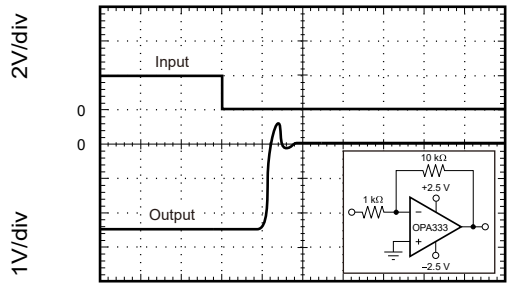


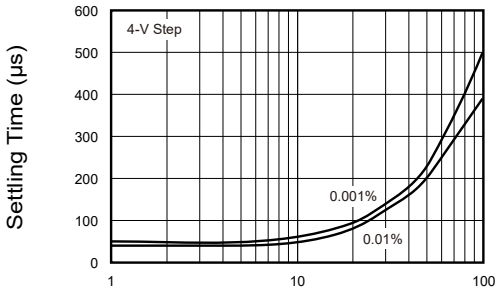

Figure 12: Positive Overvoltage Recovery

## 10.3 Typical characteristic



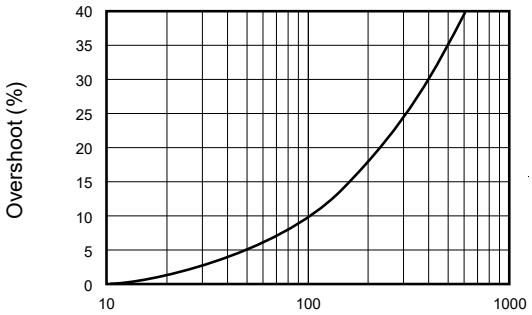

Time (50µs/div)

Figure 13: Negative Overvoltage Recovery



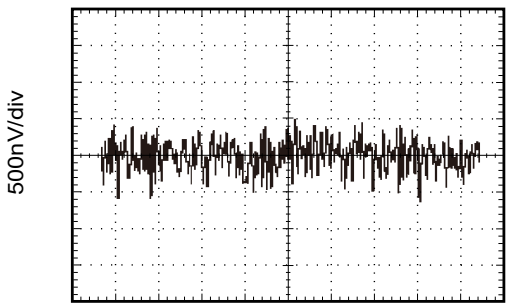

Gain (dB)

Figure 14: Settling Time vs Closed-Loop Gain



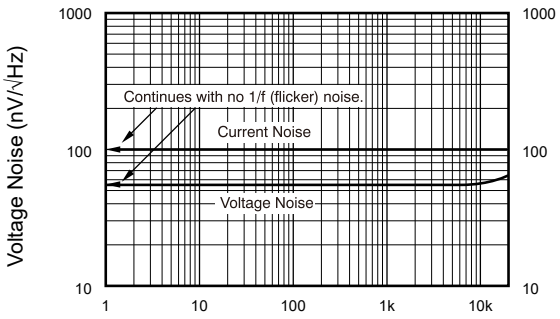

Load Capacitance (pF)

Figure 15: Small-Signal Overshoot vs Load Capacitance




1s/div

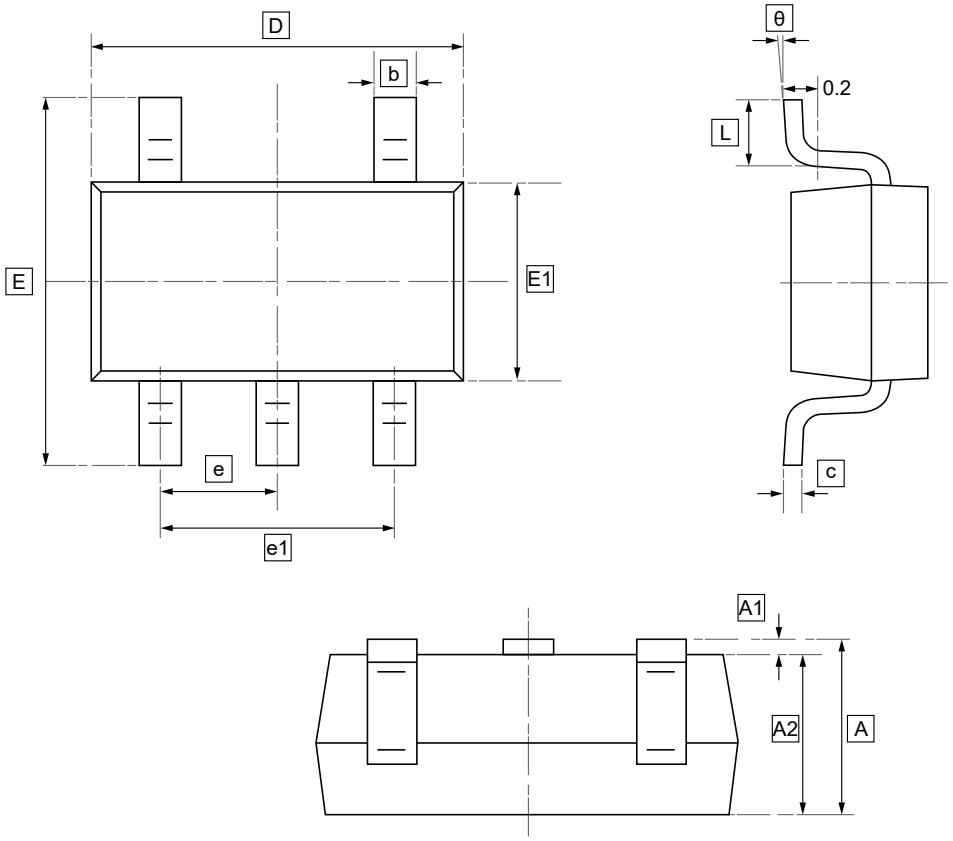
Figure 16: 0.1-Hz to 10-Hz Noise




Frequency (Hz)

Figure 17: Current and Voltage Noise Spectral Density vs Frequency

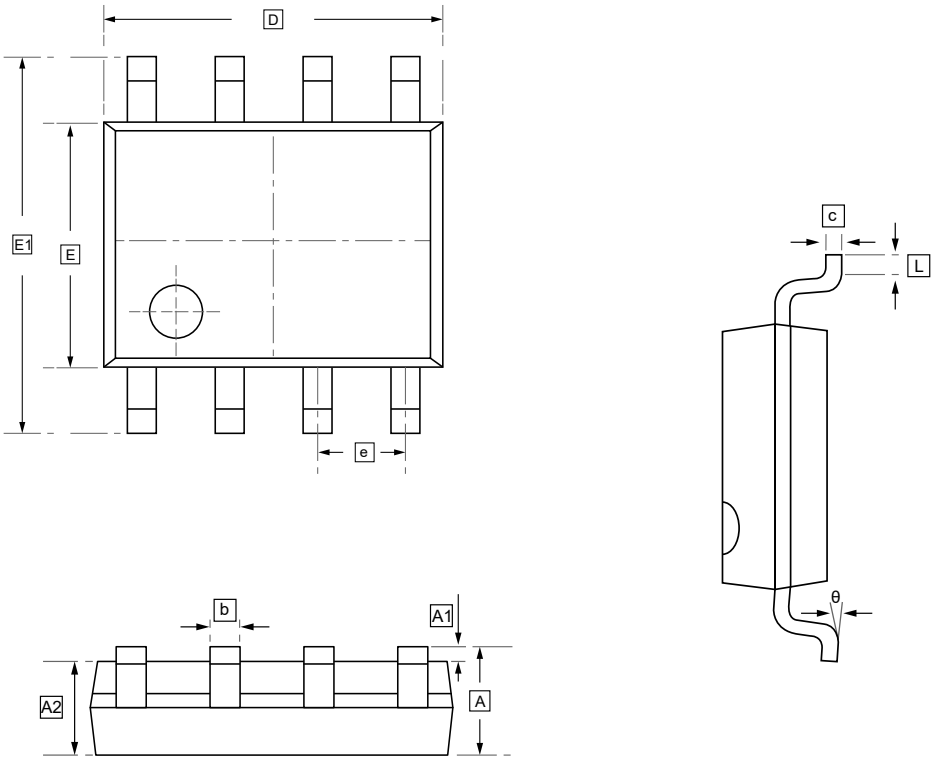
## 11.1 SOT-23-5 Package Outline Dimensions




**DIMENSIONS (mm are the original dimensions)**

| Symbol | A | A1 | A2 | b | c | D | E1 | E | e | e1 | L | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Min** | 1.050 | 0.000 | 1.050 | 0.300 | 0.100 | 2.820 | 1.500 | 2.650 | 0.950 | 1.800 | 0.300 | 0° |
| **Max** | 1.250 | 0.100 | 1.150 | 0.500 | 0.200 | 3.020 | 1.700 | 2.950 | BSC | 2.000 | 0.600 | 8° |

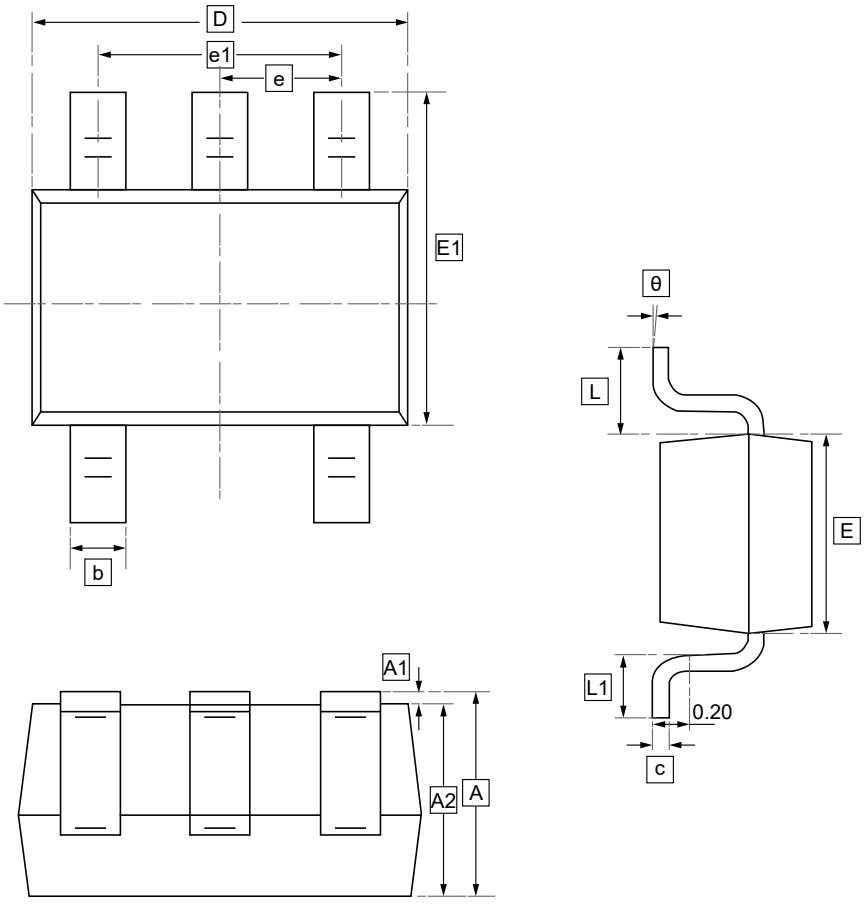
## 11.2 SOP-8 Package Outline Dimensions




**DIMENSIONS (mm are the original dimensions)**

| Symbol | A | A1 | A2 | b | c | D | E | E1 | e | L | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Min** | 1.350 | 0.000 | 1.350 | 0.330 | 0.170 | 4.700 | 3.800 | 5.800 | 1.270 | 0.400 | 0° |
| **Max** | 1.750 | 0.100 | 1.550 | 0.510 | 0.250 | 5.100 | 4.000 | 6.200 | BSC | 1.270 | 8° |

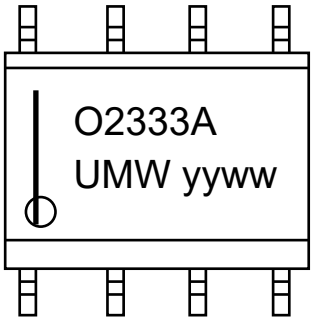
## 11.3 SC70-5 Package Outline Dimensions




**DIMENSIONS (mm are the original dimensions)**

| Symbol | A | A1 | A2 | b | c | D | E | E1 | e | e1 | L | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Min** | 0.90 | 0.00 | 0.90 | 0.15 | 0.08 | 2.05 | 1.15 | 2.15 | 0.65 | 1.20 | 0.26 | 7° |
| **Max** | 1.10 | 0.10 | 1.00 | 0.35 | 0.15 | 2.25 | 1.35 | 2.45 | TYP | 1.40 | 0.46 | REF. |

## 12.Ordering information




yy: Year Code
ww: Week Code

| Order Code | Marking | Package | Base QTY | Delivery Mode |
|---|---|---|---|---|
| UMW OPA2333AIDR | O2333A | SOP-8 | 2500 | Tape and reel |
| UMW OPA333AIDR | O333A | SOP-8 | 2500 | Tape and reel |
| UMW OPA333AIDBVR | OAXQ | SOT23-5 | 3000 | Tape and reel |
| UMW OPA333AIDCKR | BQY | SC70-5 | 3000 | Tape and reel |

## 13.Disclaimer

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