

### Product Summary

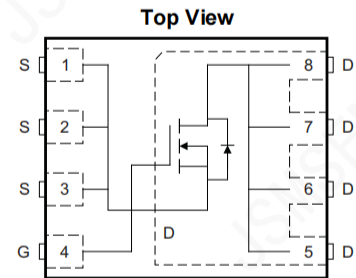
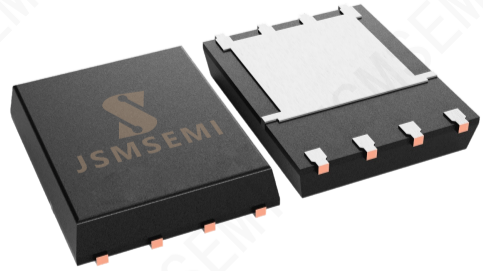
- $V_{DS}$  40V
- $I_D$  120A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ ) < 3.5m $\Omega$
- 100% EAS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor



### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Unit	
<b>Common Ratings</b>				
$V_{DSS}$	Drain-Source Voltage	40	V	
$V_{GSS}$	Gate-Source Voltage	$\pm 20$		
$I_D^G$	Continuous Drain Current	$T_C=25^\circ\text{C}$	120 <sup>G</sup>	
		$T_C=25^\circ\text{C}$	205 <sup>I</sup>	
		$T_C=100^\circ\text{C}$	80 <sup>G</sup>	
$I_{DM}^C$	Pulsed Drain Current	480	A	
$I_{DSM}$	Continuous Drain Current	$T_A=25^\circ\text{C}$	40	
		$T_A=70^\circ\text{C}$	32	
$P_D^B$	Power Dissipation	$T_C=25^\circ\text{C}$	157	
		$T_C=100^\circ\text{C}$	62	
$I_S^G$	Diode Continuous Forward Current	120	A	
$T_{STG}, T_J$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$	
$P_{DSM}$	Power Dissipation	$T_A=25^\circ\text{C}$	6.2	
		$T_A=70^\circ\text{C}$	4	
$I_{AS}^C$	Single pulsed avalanche Current	47	A	
$E_{AS}^C$	Single pulsed avalanche energy	$L=0.3\text{mH}$	331	mJ
$R_{\theta JC}$	Thermal Resistance-Junction to Case	0.8	$^\circ\text{C/W}$	
$R_{\theta JA}^{AD}$	Thermal Resistance-Junction to Ambient	$t \leq 10\text{S}$		20
		Steady State		50

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	40			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	1.8	2.5	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		2.9 3.2	3.5 4	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		3.1	3.9	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		100		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current <sup>G</sup>				120	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =20V, f=1MHz		1825		pF
C <sub>OSS</sub>	Output Capacitance			895		pF
C <sub>rSS</sub>	Reverse Transfer Capacitance			55		pF
R <sub>g</sub>	Gate resistance	f=1MHz	1	2	3.1	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, I <sub>D</sub> =20A		68	95	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge			28	40	nC
Q <sub>gs</sub>	Gate Source Charge			16.5		nC
Q <sub>gd</sub>	Gate Drain Charge			4.5		nC
Q <sub>OSS</sub>	Output Charge	V <sub>GS</sub> =0V, V <sub>DS</sub> =20V		37		nC
t <sub>D(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, R <sub>L</sub> =1Ω, R <sub>GEN</sub> =3Ω		12.5		ns
t <sub>r</sub>	Turn-On Rise Time			9.5		ns
t <sub>D(off)</sub>	Turn-Off Delay Time			57.5		ns
t <sub>f</sub>	Turn-Off Fall Time			10.5		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, di/dt=500A/μs		20		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, di/dt=500A/μs		60		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.

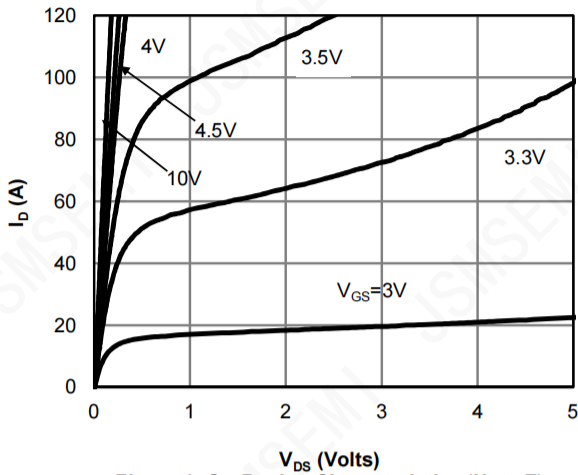
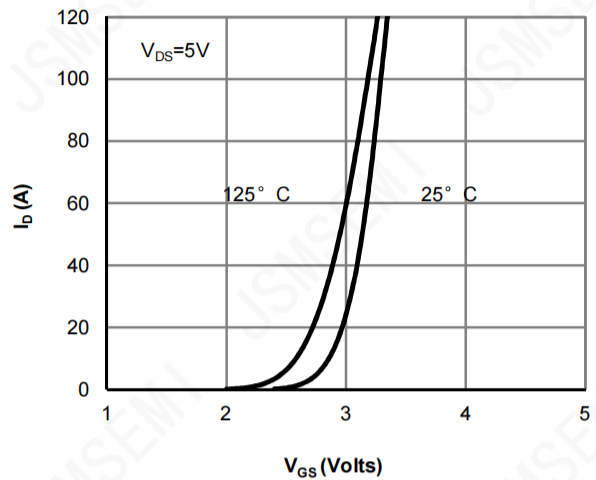
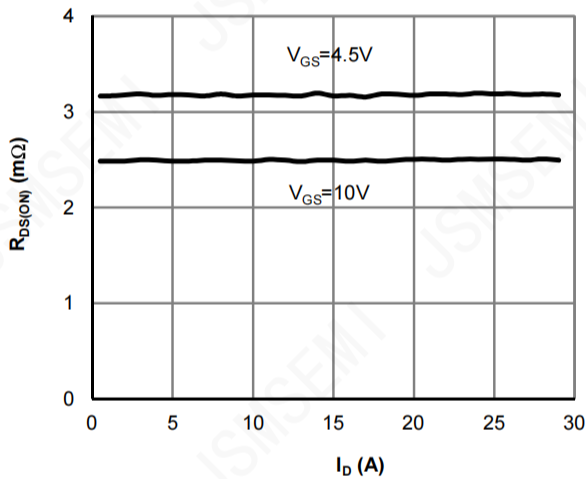
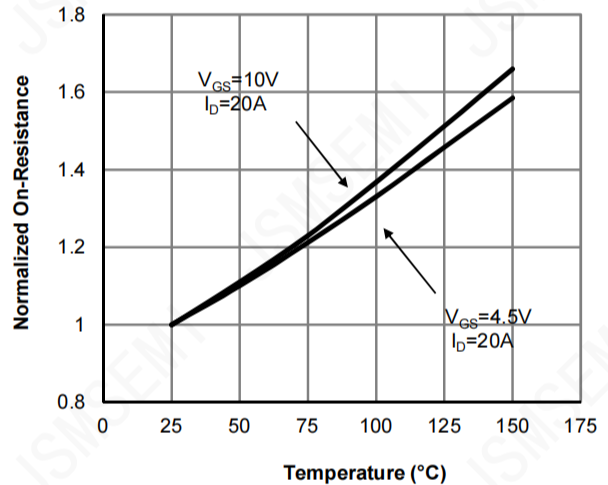
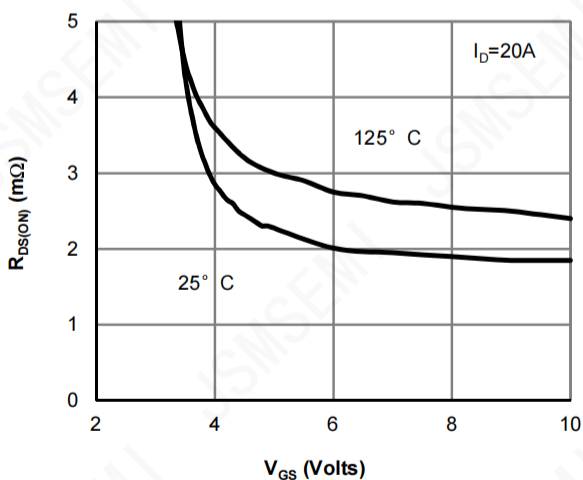
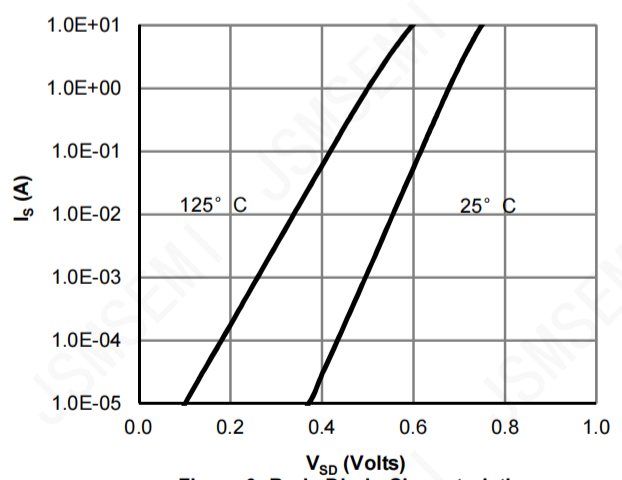
G. The maximum current rating is package limited.

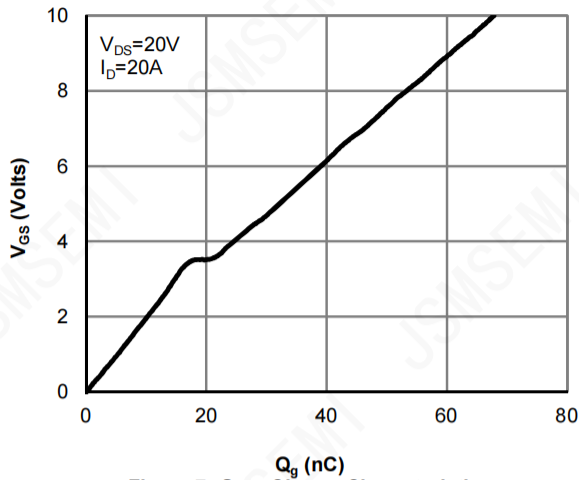
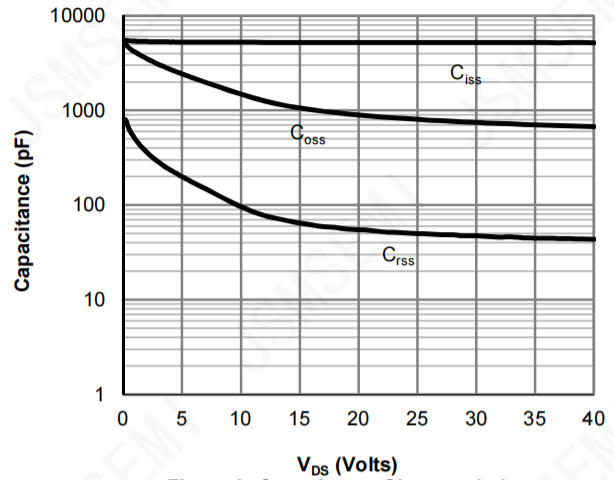
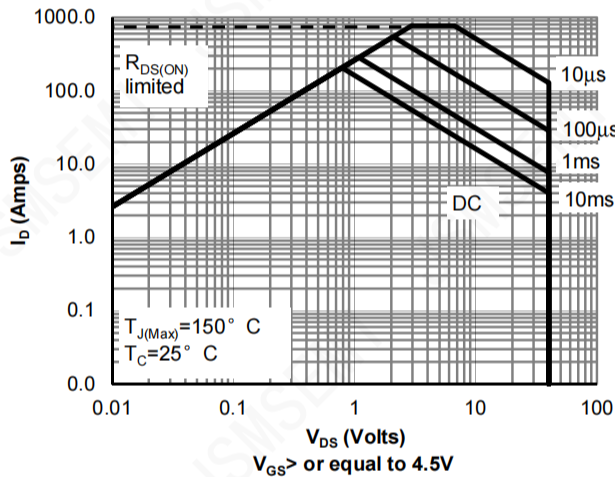
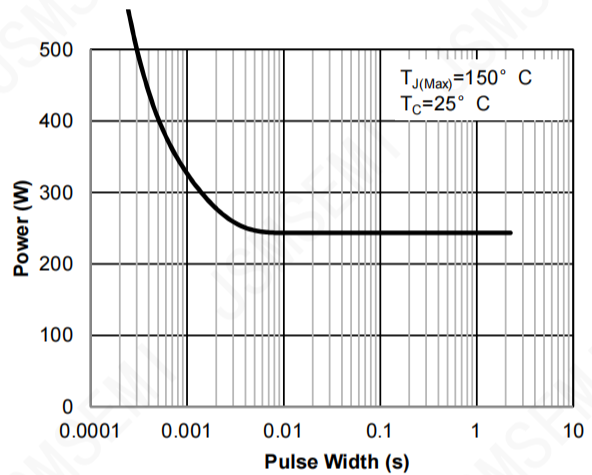
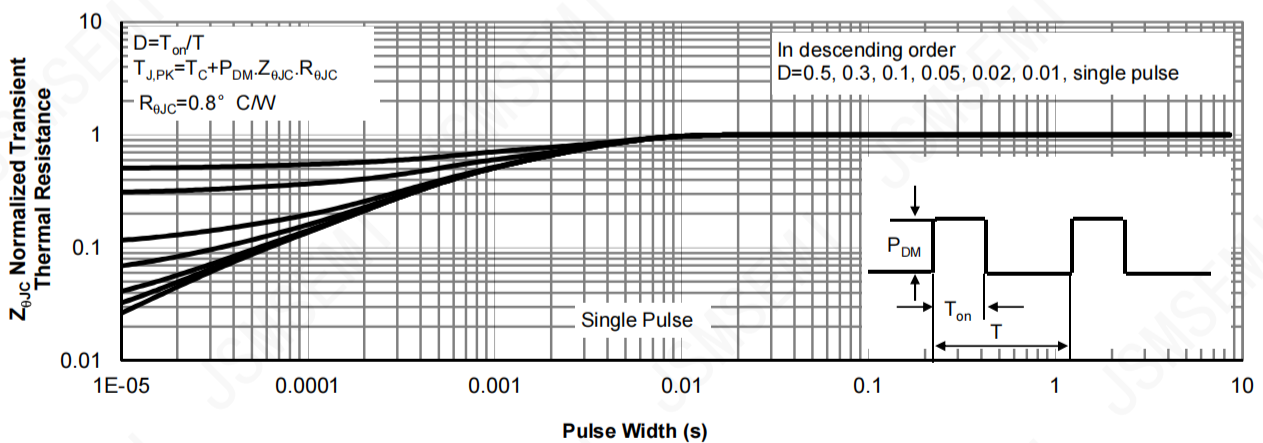
H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

I. The maximum current rating is silicon limited

**Ordering Information**

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship, Quantity	Green
BSC035N04LSGATMA1-JSM	DFN5060-8L	030N04QGL	-55 to 150°C	1	T&R, 5000	Rohs

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

**Figure 1: On-Region Characteristics (Note E)**

**Figure 2: Transfer Characteristics (Note E)**

**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**

**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

**Figure 6: Body-Diode Characteristics (Note E)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

**Figure 7: Gate-Charge Characteristics**

**Figure 8: Capacitance Characteristics**

**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**

**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

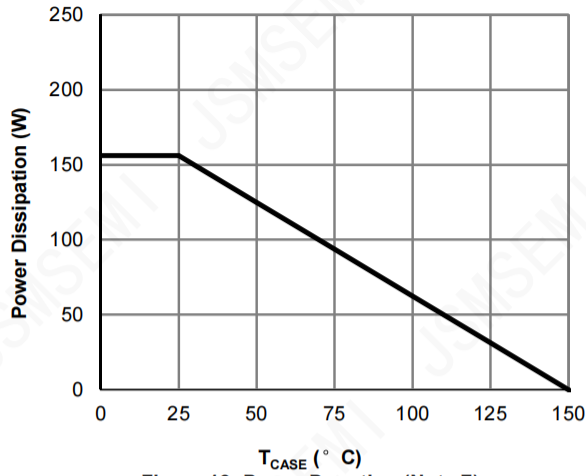
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**


Figure 12: Power De-rating (Note F)

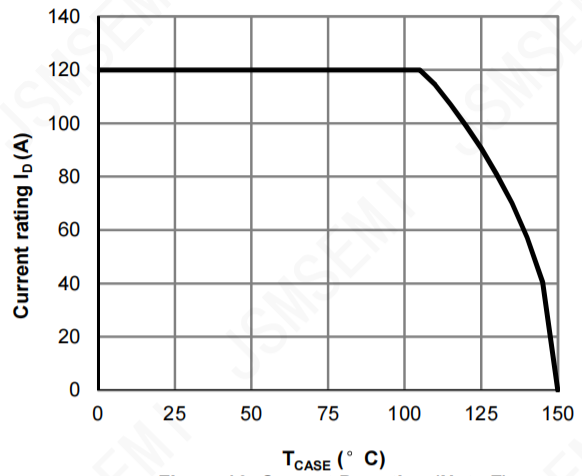


Figure 13: Current De-rating (Note F)

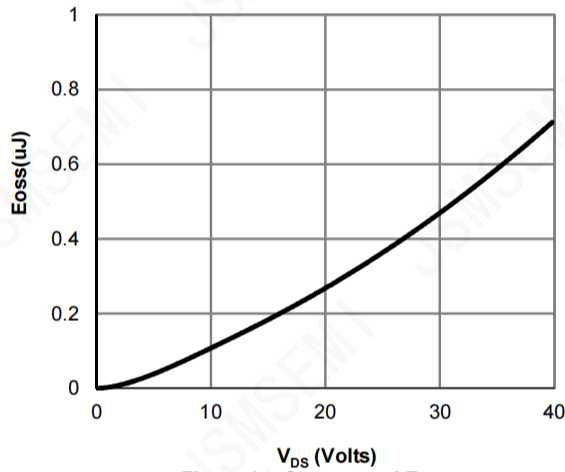


Figure 14: Coss stored Energy

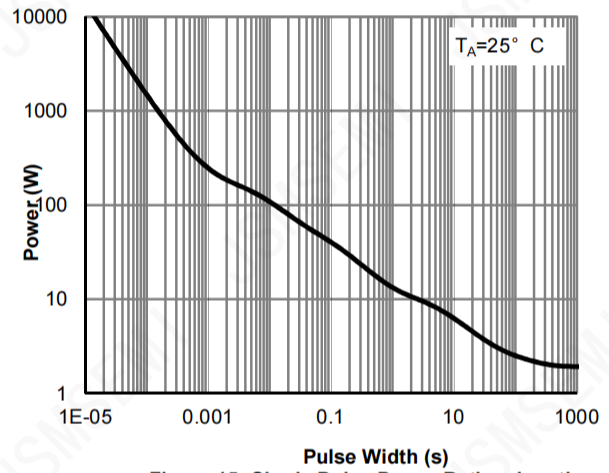


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

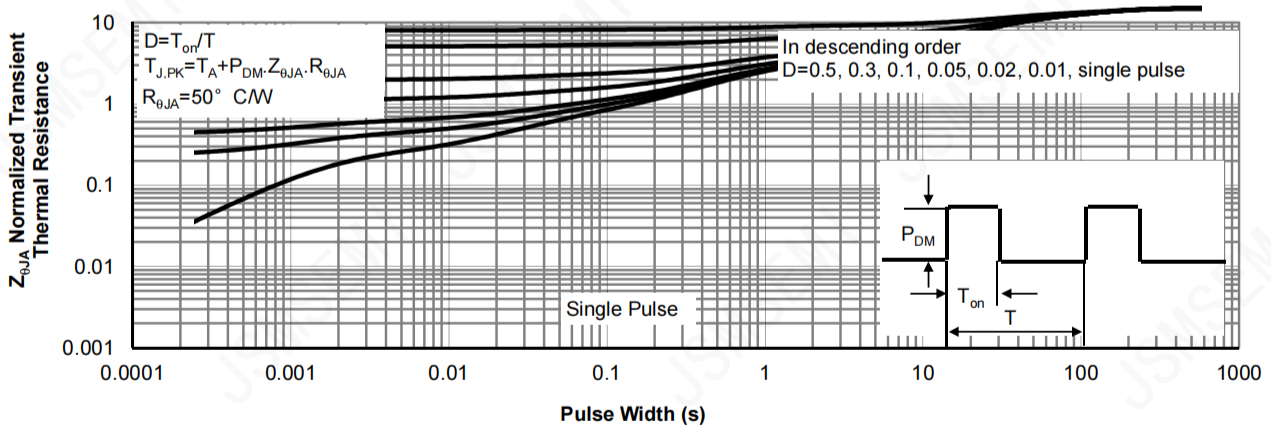


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

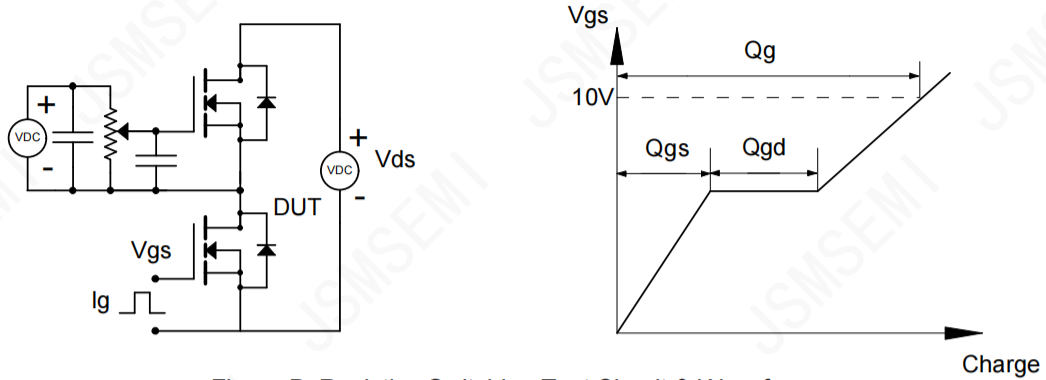


Figure B: Resistive Switching Test Circuit & Waveforms

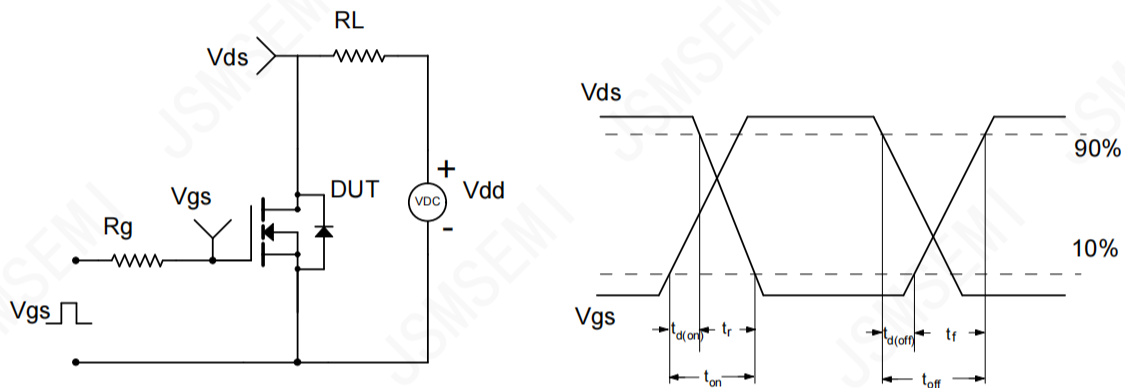


Figure C: nclamped Inductive Switching(UIS)Test Circuit & Waveforms

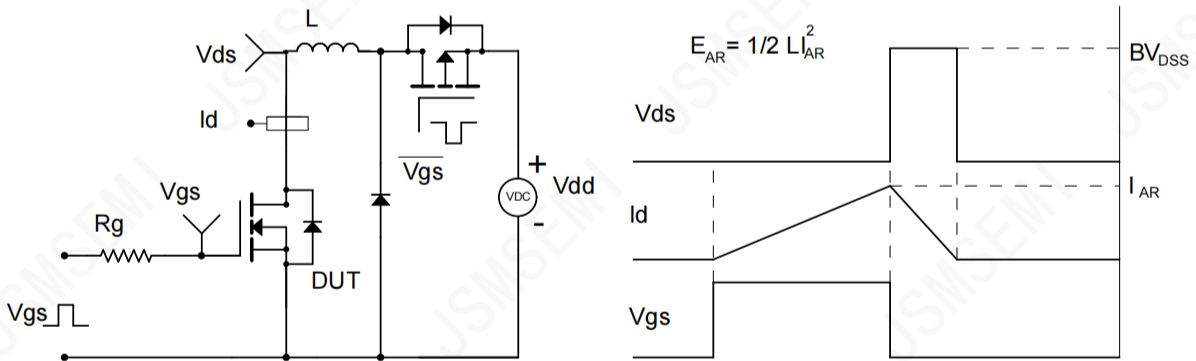
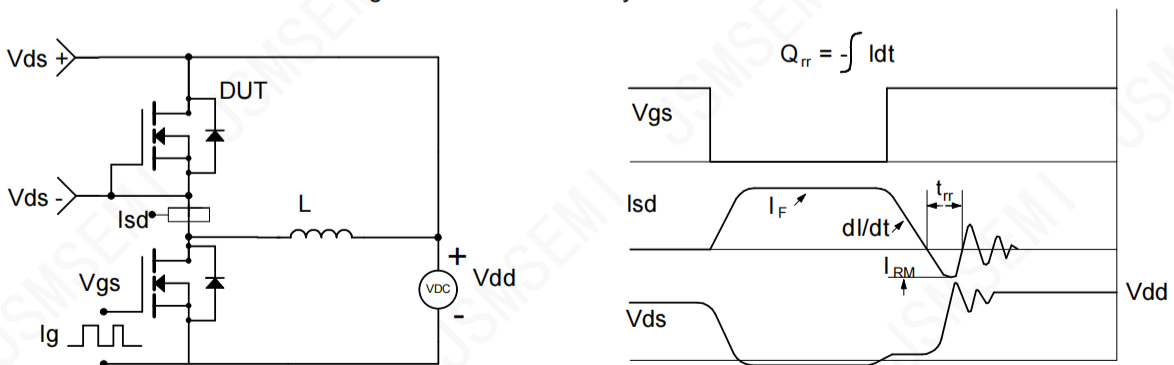
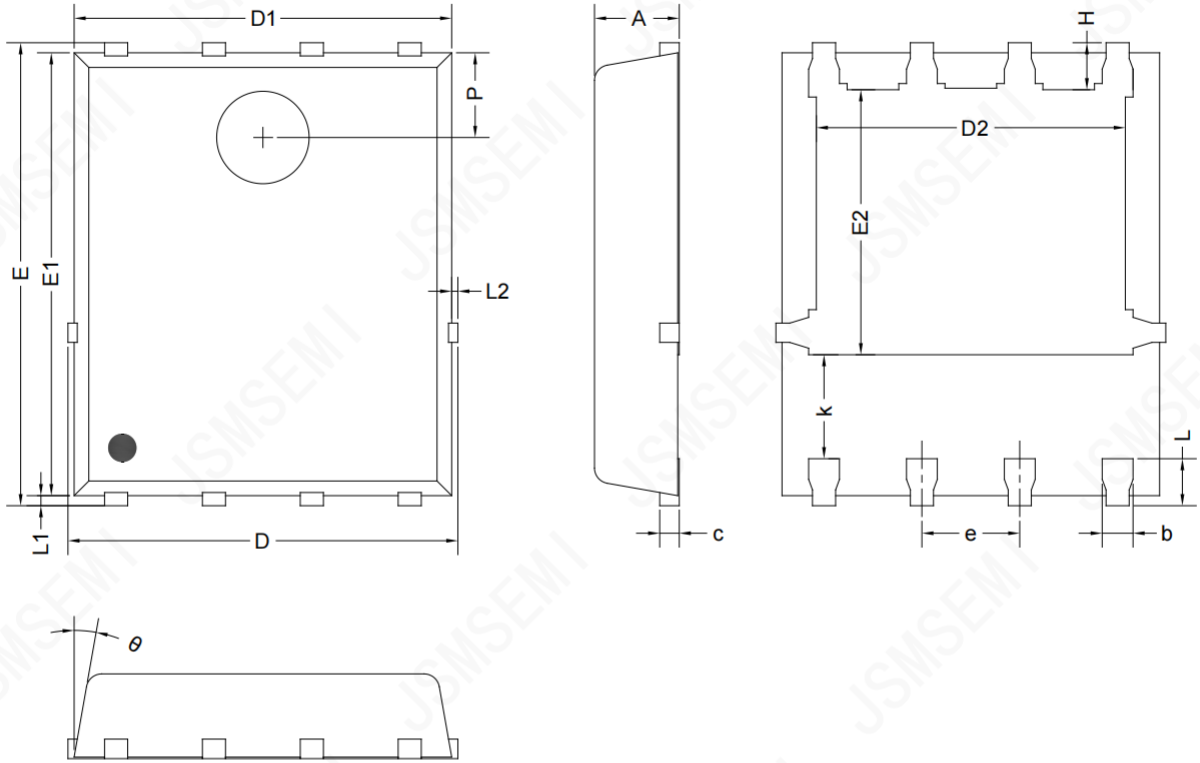


Figure D: Diode Recovery Test Circuit & Waveforms



**Package Information**
**DFN5060-8L**


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.000	1.100	1.200
b	0.350	0.400	0.450
c	0.210	0.250	0.340
D	4.800	-	5.100
D1	4.800	4.900	5.000
D2	3.910	4.010	4.110
E	5.900	6.000	6.100
E1	5.700	5.750	5.800
E2	3.340	3.440	3.540
e	1.270 BSC		
H	0.510	0.610	0.710
k	1.100	-	-
L	0.510	0.610	0.710
L1	0.060	0.130	0.200
L2	-	-	0.100
P	1.000	1.100	1.200
$\theta$	8°	10°	12°

NOTE: This drawing is subject to change without notice.

## Revision History

Rev.	Change	Date
V1.0	Initial version	6/27/2021

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