

钍地半导体
Tudi Semiconductor

Product Specification

TUDI-UC284xA UC384xA

Current-Mode PWM Controller

网址 www.sztdbdt.com

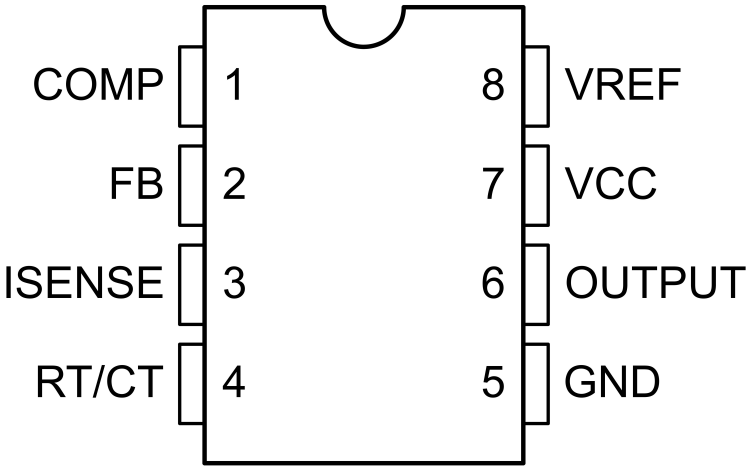
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semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- Optimized for Off-Line and DC-DC Converters
- Low Start-Up Current (< 0.5mA)
- Trimmed Oscillator Discharge Current
- Automatic Feedforward Compensation
- Pulse-by-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Undervoltage Lockout With Hysteresis
- Double Pulse Suppression
- High-Current Totem Pole Output
- Internally-Trimmed Bandgap Reference
- Up to 500kHz Operation



SOP8/DIP8

Description

The UCx84xA family of control devices is a pin-for-pincompatible improved version of the UCx84x family. Providing the necessary features to control currentmode or switched-mode power supplies, this family of devices has many improved features: startup current is less than 0. 5mA, oscillator discharge is trimmed to8.3mA, and during UVLO, the output stage can sink at least 10mA at less than 1.2V for Vcc over 5V.

Applications

- Switch Mode Power Supplies (SMPS)
- DC-DC Converters
- Power Modules
- Industrial PSU
- Battery Operated PSU

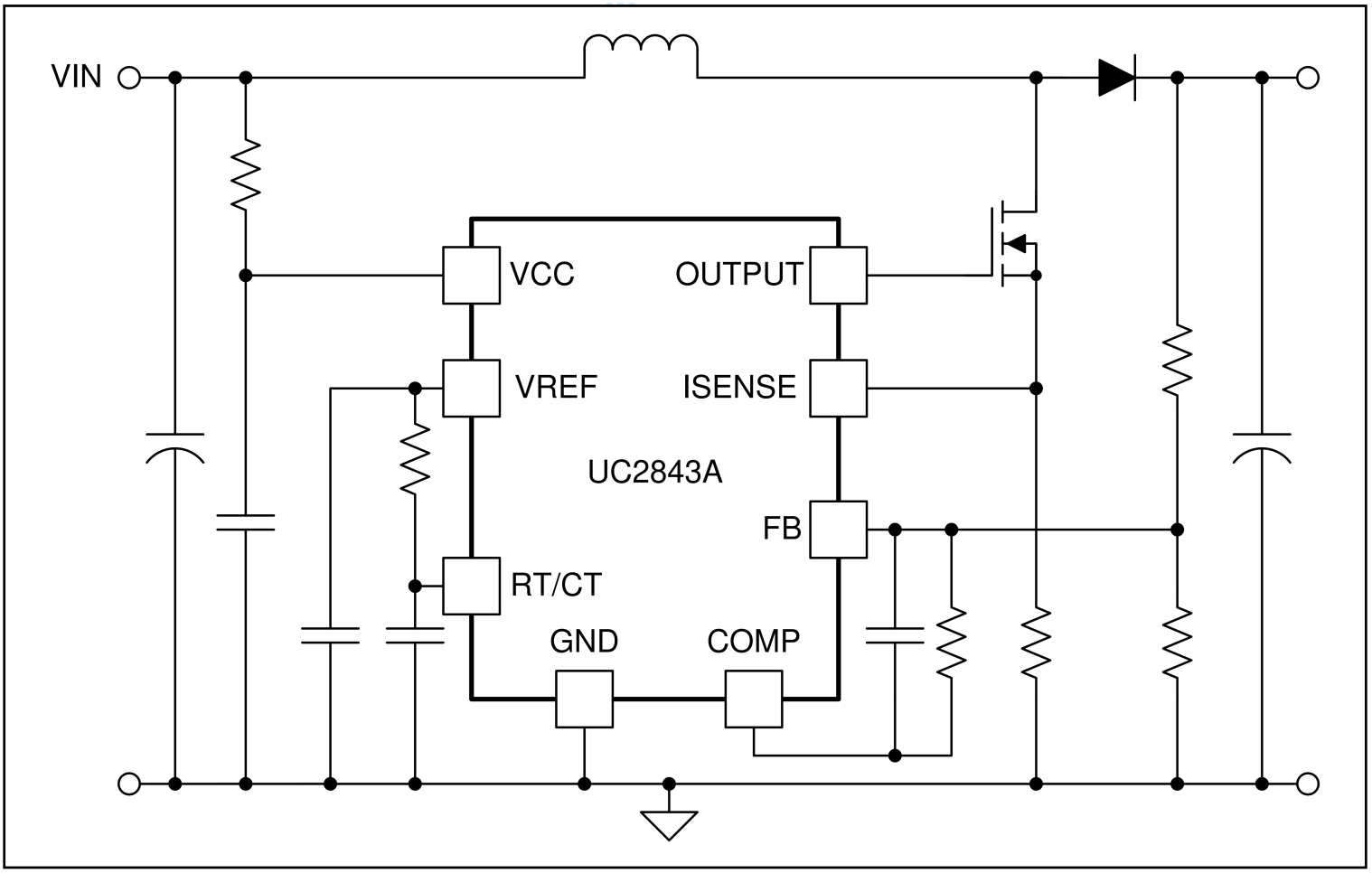


Figure 1.Simplified Application Diagram

Table 1.Pin Functions

PIN		Type (1)	DESCRIPTION
NAME	NO. PDIP(8), SOIC(8)		
COMP	1	O	Outputs the low impedance 1-MHz internal error amplifier that isalso the input to the peak current limit or PWM comparator,with anopen-loop gain (AVOL) of 80 dB.This pin is capable of sinking a maximum of 6 mA and is not internally current limited.
FB	2	I	Input to the error amplifier that can be used to control the power converter voltage-feedback loop for stability.
ISENSE	3	I	Input to the peak current limit,PWM comparator of the UCx84×A controllers.When used in conjunction with a current sense resistor,the error amplifier output voltage controls the power systems cycle-by-cycle peak current limit.The maximum peak current sense signalis internally clamped to 1V.
RT/CT	4	I	Input to the internal oscillator that is programmed with an external timing resistor(RT)and timing capacitor (CT).TUDI recommends using capacitance values from 470 pF to 4.7 nF.TUDI also recommends that the timing resistor values chosen be from 5kΩ to100 kΩ.
GND	5	—	This is the controller signal ground.
OUTPUT	6	O	Output of 1-A totem pole gate driver.This pin can sink and source upto 1 A of gate driver current.A gate driver resistor must be used to limit the gate driver current.
VCC	7	I	Bias input to the gate driver.This pin must have a biasing capacitorthat is at least 10 times greater than the gate capacitance of themain switching FET used in the design.
VREF	8	O	Reference voltage output of the PWM controller.This pin mustsupply no more than 10 mA under normal operation.This outputis short-circuit protected at roughly 100 mA.This reference is also used for internal comparators and needs a high frequency bypass capacitor of 1μF.The VCC capacitor also must be at least 10 times greater than the capacitor on the VREF pin.

(1)I = Input; O = Output

Specifications

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage(low impedance source)	VCC pin		30	V
Output current,IOUT			± 1	A
Output energy(capacitive load)			5	μJ
Analog inputs		-0.3	6.3	V
Maximum negative voltage	All pins	-0.3		V
Differential voltage between VC and VCC	VC pin	-0.3		V
Error amplifier output sink current,I_{COMP}			10	mA
Power dissipation at $T_A \leq 25°C$			1	W
Lead temperature (soldering,10 s)			300	°C
Junction temperature,T_J		-55	150	°C
Storage temperature,T_{stg}		-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage.Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM),per ANSI/ESDAJJEDEC JS-001 (1)	±2000	V
	Charged-device model (CDM),per JEDEC specification JESD22-C101(2)	± 1500	

(1)JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2)JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC} Bias supply voltage	V_{CC} pin		11		V
V_{FB},V_{RC},V_{VFB} Voltage on analog pins	FB,ISENSE,and RT/CT pins	-0.1		5	V
V_{OUT} Gate driver output voltage		-0.1		VCC	V
I_{VCC} Supply bias current				25	mA
I_{VREF} Output current	VREF pin			10	mA
f_{OSC} Oscillator frequency				500	kHz
T_A Operating free-air temperature	UC284xA	-40		85	℃
	UC384xA	0		70	

Thermal Information

THERMAL METRIC		UC284xA,UC384xA		UNIT
		P(PDIP)	D (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermalresistance	74.1	117.4	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top)thermal resistance	63.4	51.5	℃/W
$R_{\theta JB}$	Junction-to-board thermalresistance	50.5	61	℃/W
ψ_{JT}	Junction-to-topcharacterization parameter	34.6	7.8	℃/W
ψ_{JB}	Junction-to-boardcharacterization parameter	49.2	60.2	℃/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom)thermal resistance	—	—	℃/W

Electrical Characteristics

Unless otherwise stated, these specifications apply for T_A= – 40 ° C to 125 ° C (UC284xAQ), T_A= – 40 ° C to 85 ° C (UC284xA), T_A= 0 ° C to 70 ° C (UC384xA); T_A=T_J;V_{CC}= 15V(4);R_T= 10 kΩ; C_T= 3.3 nF.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE						
Output voltage	T_J=25°C,Io=1mA	UC284xA	4.95	5	5.05	V
		UC384xA	4.9	5	5.1	
Line regulation	12≤V_{IN}≤25V			6	20	mV
Load regulation	1≤Io≤20 mA			6	25	mV
Temperature stability	See(1)(6)			0.2	0.4	mV°C
Total output variation	Line,Load,Temperature	UC284xA	4.9		5.1	V
		UC384xA	4.82		5.18	
Output noise voltage	10 Hz≤f≤10 kHz;T_J=25°°C(1)			50		μV
Long-term stability	T_A=125°C,1000 hrs(1)			5	25	mV
Output short circuit			-30	-100	-180	mA
OSCILLATOR						
Initial accuracy	T_J=25°°C(5)		47	52	57	kHz
Voltage stability	12≤Vcc≤25V			0.2%	1%	
Temperature stability	T_{MIN}≤T_A≤T_{MAX}(1)			5%		
Amplitude	$V_{RT/CT}$ peak to peak(1)			1.7		V
Discharge current	T_J=25°C,$V_{RT/CT}$=2V(7)		7.8	8.3	8.8	mA
	$V_{RT/CT}$=2V(7)	UC284xA	7.5		8.8	
		UC384xA	7.6		8.8	
ERROR AMPLIFIER						
Input voltage	V_{COMP}=2.5V	UC284xA	2.45	2.5	2.55	V
		UC384xA	2.42	2.5	2.58	
Input bias current				-0.3	-1	μA
				-0.3	-2	
A_{VOL} Open-loop gain	2≤Vo≤4V		65	90		dB
Unity gain bandwidth	T_J=25°C(1)		0.7	1		MHz
CMRR Common mode rejection ratio	12≤Vcc≤25V		60	70		dB
Output sink current	V_{FB}=2.7V,V_{COMP}=1.1V		2	6		mA
Output source current	V_{FB}=2.3 V,V_{COMP}=5V		-0.5	-0.8		mA
V_{OUT} high	V_{FB}=2.3V,R_L=15kΩ to ground		5	6		V
V_{OUT} low	V_{FB}=2.7V,R_L=15kΩ to VREF			0.7	1.1	V

Electrical Characteristics(continued)

Unless otherwise stated, these specifications apply for T_A= – 40 ° C to 125 ° C (UC284xAQ), T_A= – 40 ° C to 85 ° C (UC284xA), T_A= 0 ° C to 70 ° C (UC384xA); T_A=T_J;V_{CC}= 15V(4);R_T= 10 kΩ; C_T= 3.3 nF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE					
Gain	See (2)(3)	2.85	3	3.15	VIN
Maximum input signal	V_{COMP}=5V(2)	0.9	1	1.1	V
PSRR Power supply rejection ratio	12≤Vcc≤25V(2)		70		dB
Input bias current			-2	-10	μA
Delay to output	V_{ISENSE}=0 to 2V(1)		150	300	ns
OUTPUT					
Output low level	I_{SINK}=20 mA		0.1	0.4	V
	I_{SINK}=200 mA		1.5	2.2	
Output high level	I_{SOURCE}=20 mA	13	13.5		V
	I_{SOURCE}=200 mA	12	13.5		
Rise time	T_J=25℃,C_L=1nF(1)		25	150	ns
Fall time	T_J=25°℃,C_L=1nF(1)		25	150	ns
UVLO saturation	Vcc=5V,I_{SINK}=10 mA		0.7	1.2	V
UNDERVOLTAGE LOCKOUT					
Start threshold	UC2842Aand UC2844A	15	16	17	V
	UC3842A and UC3844A	14.5	16	17.5	
	UCx843A and UCx845A	7.8	8.4	9	
Minimum operation voltage afterturnon	UC2842A and UC2844A	9	10	11	V
	UC3842A and UC3844A	8.5	10	11.5	
	UCx843A and UCx845A	7	7.6	8.2	
PWM					
Maximum duty cycle	UCx842A,UCx843A	92%	96%	100%	
	UCx844A,UCx845A	46%	48%	50%	
Minimum duty cycle				0%	
TOTAL STANDBY CURRENT					
Start-up current			0.3	0.5	mA
Operating supply current	V_{FB}=V_{ISENSE}=0V		11	17	mA
Vcc Zener voltage	Icc=25 mA	30	39		V

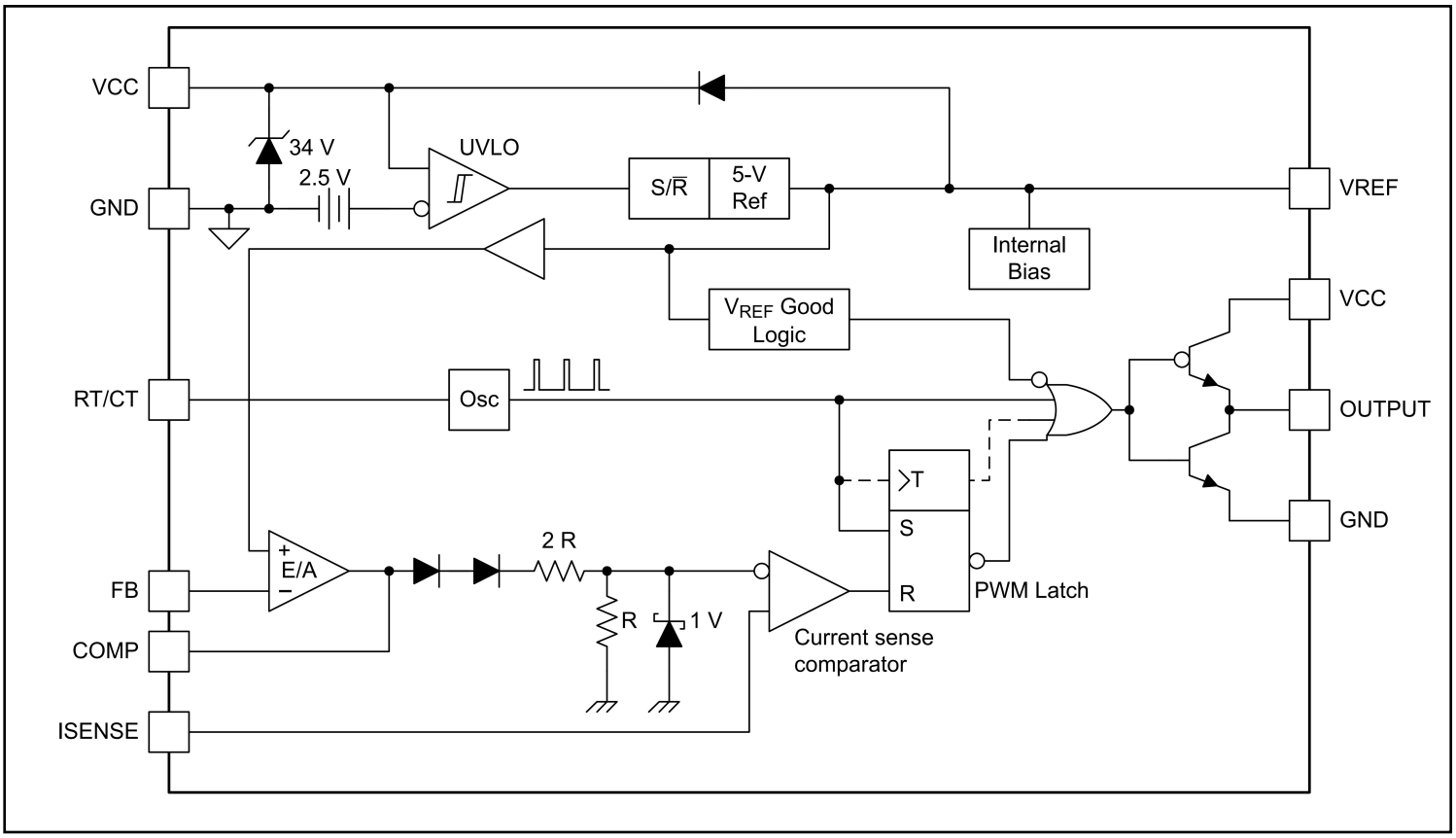
(1)Verified by design, but not 100% production tested.
(2)Parameter measured at trip point of latch with V_{FB} = 0.
(3)Gain defined as:A= Δ V_{COMP}/ Δ V_{ISENSE}; 0 ≤ V_{ISENSE}≤ 0.8 V.
(4)Adjust V_{CC} above the start threshold before setting at 15 V.
(5)Output frequency equals oscillator frequency for the UCx842A and UCx843A. Output frequency is one half oscillator frequency for the UCx844A and UCx845A.
(6)Temperature stability, sometimes referred to as average temperature coefficient, is described by: Temperature stability = (VREF (max)-$V_{REF(min)}$)/($T_{J(max)}$-$T_{J(min)}$).VREF(max)andVREF(min are the maximum and minimum reference voltage measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.
(7)This parameter is measured with R_T= 10 kΩtoV_{REF}. This contributes approximately 300 μA of current to the measurement. The total current flowing into the RT/CT pin is approximately 300 μA higher than the measured value.

Detailed Description

Overview

The UCx84xA family of fixed-frequency pulse-width-modulator (PWM) controllers are designed to operate at switching frequencies of 500 kHz. These controllers are designed for peak current mode (PCM) and can be used in isolated and non-isolated power supply designs. These controllers can drive FETs directly from the output, which is capable of sourcing and sinking up to 1 A of gate driver current. These devices also have a built-in low-impedance amplifier that can be used in non-isolated designs to control the power supply output voltage and feedback loop.

Functional Block Diagram



Feature Description

Pulse-by-Pulse Current Limiting: Pulse-by-pulse limiting is inherent in the current mode control scheme. An upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while providing reliable supply operation.

Current Sense Circuit

Peak current (I_S) is determined by Equation 1 :

$$I_{S(max)} * \frac{1V}{R_S} \quad (1)$$

A small RC filter can be required to suppress switch transients.

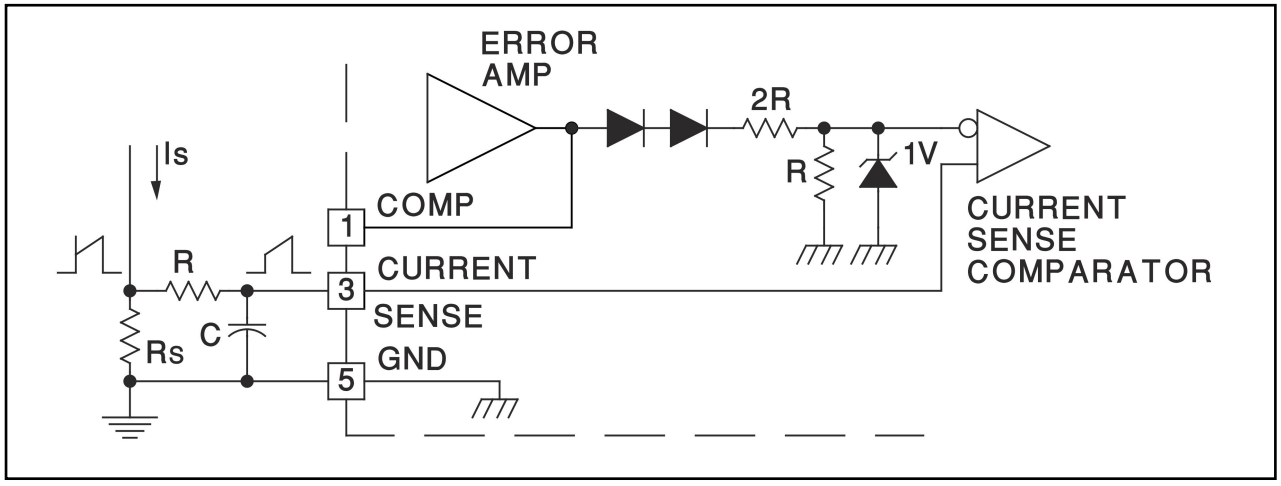


Figure 2. Current Sense Circuit Diagram

Error Amplifier Configuration：The error amplifier can source up to 0.8 mA, and sink up to 6 mA.

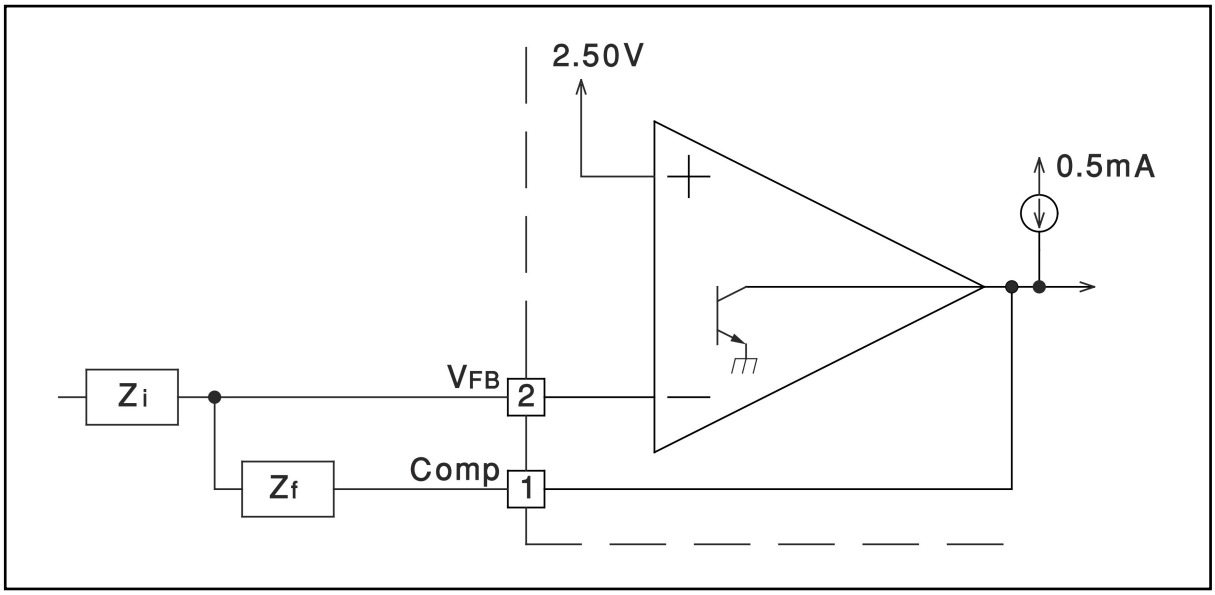


Figure 3. Error Amplifier Configuration Diagram

Device Functional Modes

Normal Operation The IC can be used in peak current mode (PCM) control or voltage mode (VM) control. When the converter is operating in PCM, the voltage amplifier output regulates the converter peak current and duty cycle. When the IC is used in VM control, the voltage amplifier output regulates the power converter duty cycle. The regulation of the system peak current and duty cycle can be achieved with the use of the integrated error amplifier and external feedback circuitry.

Undervoltage Lockout (UVLO) Start-Up: During system start-up, VCC voltage starts to rise from 0. Before the VCC voltage reaches the corresponding start threshold, the IC is operating in UVLO mode. After the UVLO turn start-up threshold is met the device becomes active and the reference comes up to 5 V.

UVLO Turnoff Mode: If the bias voltage to VCC drops below the UVLO minimum operating voltage, PWM switching stops and the reference becomes inactive, returning to 0 V. The device can be restarted by applying a voltage greater than the UVLO start threshold to the VCC pin.

ORDERING INFORMATION

Order Number	Package	Package Quantity	Marking On The park	Temperature
UC2842AD8TR-TUDI	SOP8	Tape,Reel,4000	UC2842A	-40℃ to 85℃
UC2842AN-TUDI	DIP8	Tube,50,A box of 2000	UC2842AN	
UC2842AQD8R-TUDI	SOP8	Tape,Reel,4000	UC2842AQ	
			2842AQ	
UC2843AD8TR-TUDI	SOP8	Tape,Reel,4000	UC2843A	
UC2843AN-TUDI	DIP8	Tube,50,A box of 2000	UC2843AN	
UC2843AQD8RQ1-TUDI	SOP8	Tape,Reel,4000	UC2843AQ	
			2843AQ	
UC2844AD8TR-TUDI	SOP8	Tape,Reel,4000	UC2844A	
UC2844AN-TUDI	DIP8	Tube,50,A box of 2000	UC2844AN	
UC2844AQD8R-TUDI	SOP8	Tape,Reel,4000	UC2844AQ	
			2844AQ	
UC2845AD8TR-TUDI	SOP8	Tape,Reel,4000	UC2845A	-40℃ to 85℃
UC2845AN-TUDI	DIP8	Tube,50,A box of 2000	UC2845AN	
UC2845AQD8R-TUDI	SOP8	Tape,Reel,4000	UC2845AQ	
			2845AQ	

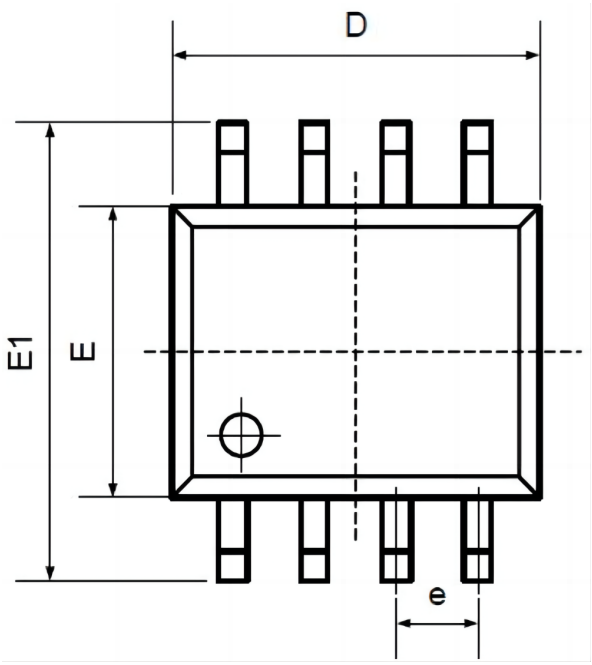
ORDERING INFORMATION

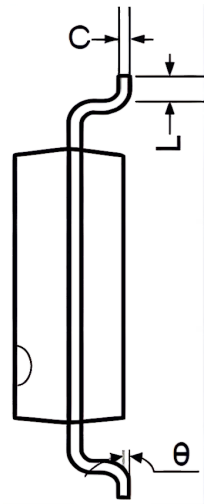
Order Number	Package	Package Quantity	Marking On The park	Temperature
UC3842AD8TR-TUDI	SOP8	Tape,Reel,4000	UC3842A	0℃ to 70℃
UC3842AN-TUDI	DIP8	Tube,50,A box of 2000	UC3842AN	
UC3843AD8TR-TUDI	SOP8	Tape,Reel,4000	UC3843A	
UC3843AN-TUDI	DIP8	Tube,50,A box of 2000	UC3843AN	
UC3844AD8TR-TUDI	SOP8	Tape,Reel,4000	UC3844A	
UC3844AN-TUDI	DIP8	Tube,50,A box of 2000	UC3844AN	
UC3845AD8TR-TUDI	SOP8	Tape,Reel,4000	UC3845A	
UC3845AN-TUDI	DIP8	Tube,50,A box of 2000	UC3845AN	

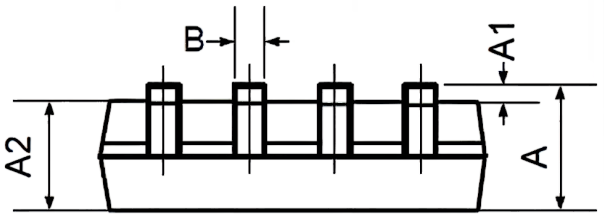
Revision history

	Date	Revision	Page
V1.0	2020/9	New	1-11
V1.1	2025/12	Update model and PDF template	1-16

Package SOP8

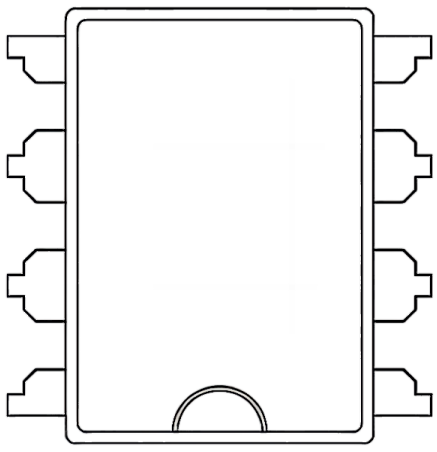


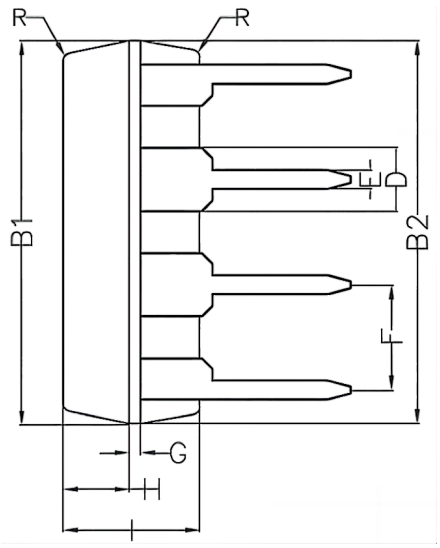


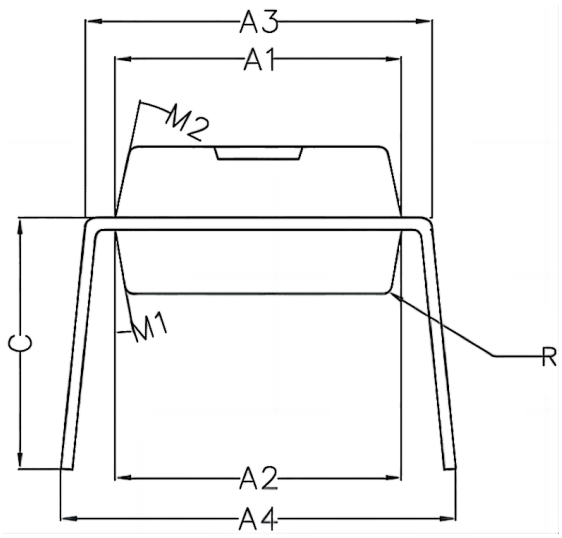


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package DIP8







Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

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