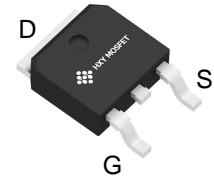




Description

The NVD4810NT4G-VF01 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



TO-252-2L

General Features

$V_{DS} = 30V$ $I_D = 60A$

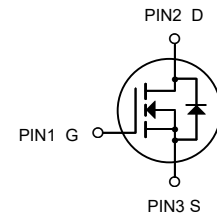
$R_{DS(ON)} < 9m\Omega$ @ $V_{GS}=10V$

Application

Battery protection

Load switch

Uninterruptible power supply



N-Channel MOSFET

Ordering Information

Product ID	Pack	Brand	Qty(PCS)
NVD4810NT4G-VF01	TO-252-2L	HXY MOSFET	2500

Absolute Maximum Ratings (Tc=25°C unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, V_{GS} @ 10V ¹	60	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, V_{GS} @ 10V ¹	40	A
$I_D@T_A=25^\circ C$	Continuous Drain Current, V_{GS} @ 10V ¹	13.6	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, V_{GS} @ 10V ¹	11.4	A
I_{DM}	Pulsed Drain Current ²	110	A
EAS	Single Pulse Avalanche Energy ³	57.8	mJ
I_{AS}	Avalanche Current	34	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	41	W
$P_D@T_A=25^\circ C$	Total Power Dissipation ⁴	2.42	W
T_{STG}	Storage Temperature Range	-55 to 175	°C
T_J	Operating Junction Temperature Range	-55 to 175	°C
$R_{\theta JA}$	Thermal Resistance Junction-ambient (Steady State) ¹	62	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	3.6	°C/W



Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.027	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =30A	---	7	9	mΩ
		V _{GS} =4.5V, I _D =15A	---	11	14	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.2	1.5	2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-5.8	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =24V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =30A	---	38	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	2.2	3.5	
Q _g	Total Gate Charge (4.5V)	V _{DS} =15V, V _{GS} =4.5V, I _D =15A	---	12.6	17.6	nC
Q _{gs}	Gate-Source Charge		---	4.2	5.9	
Q _{gd}	Gate-Drain Charge		---	5.1	7.1	
T _{d(on)}	Turn-On Delay Time	V _{DD} =15V, V _{GS} =10V, R _G =3.3 I _D =15A	---	4.6	9.2	ns
T _r	Rise Time		---	12.2	22	
T _{d(off)}	Turn-Off Delay Time		---	26.6	53	
T _f	Fall Time		---	8	16	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	1317	1843	pF
C _{oss}	Output Capacitance		---	163	228	
C _{rss}	Reverse Transfer Capacitance		---	131	183	
I _S	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	55	A
I _{SM}	Pulsed Source Current ^{2,5}		---	---	110	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.2	V
t _{rr}	Reverse Recovery Time	I _F =30A, di/dt=100A/μs, T _J =25°C	---	9.2	---	nS
Q _{rr}	Reverse Recovery Charge		---	2	---	nC

Note :

- 1 .The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=34A
- 4.The power dissipation is limited by 175°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



Typical Characteristics

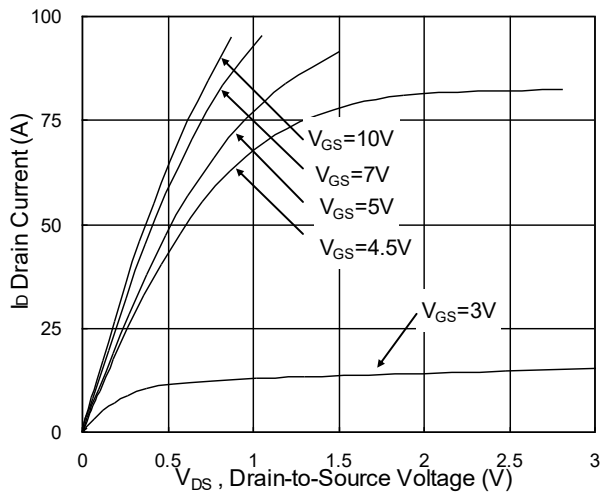


Fig.1 Typical Output Characteristics

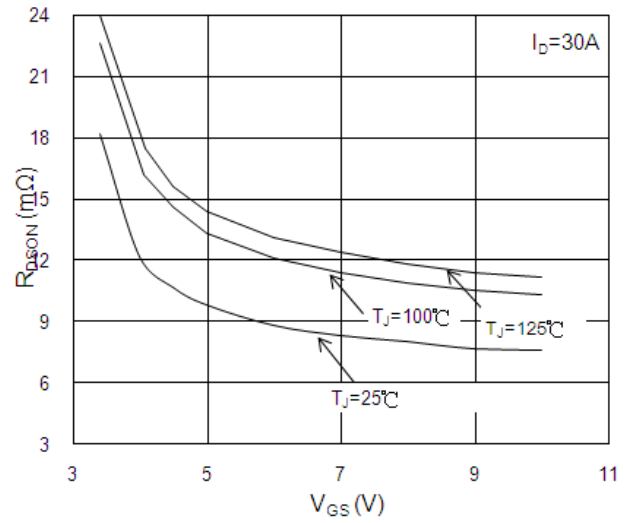


Fig.2 On-Resistance vs. G-S Voltage

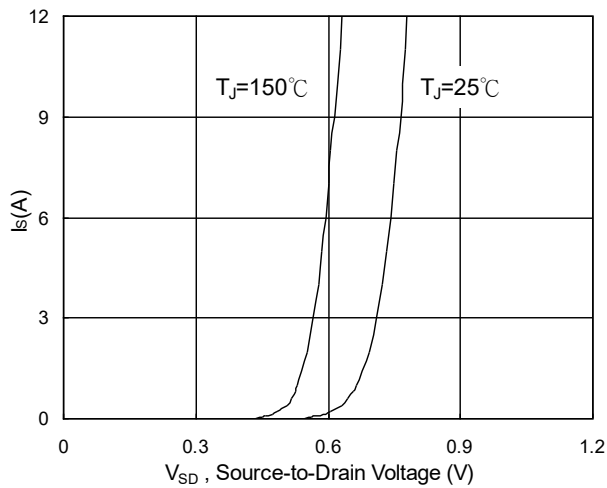


Fig.3 Forward Characteristics of Reverse

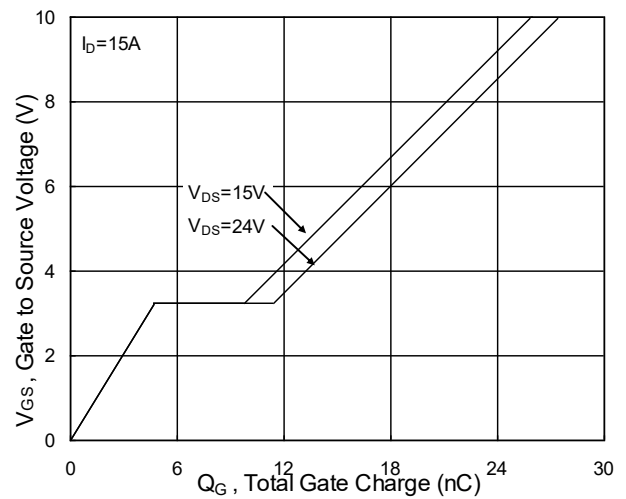


Fig.4 Gate-Charge Characteristics

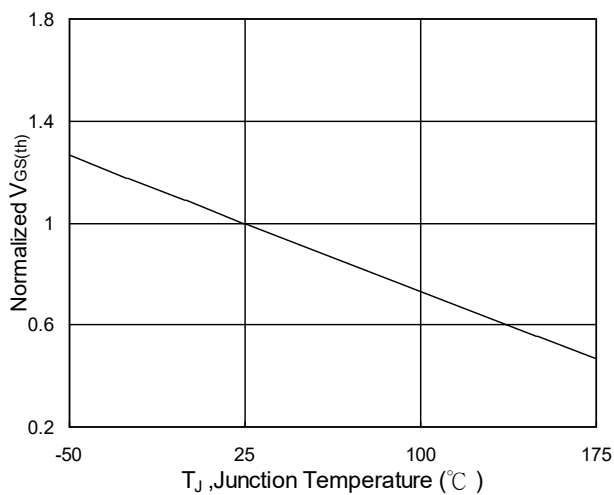


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

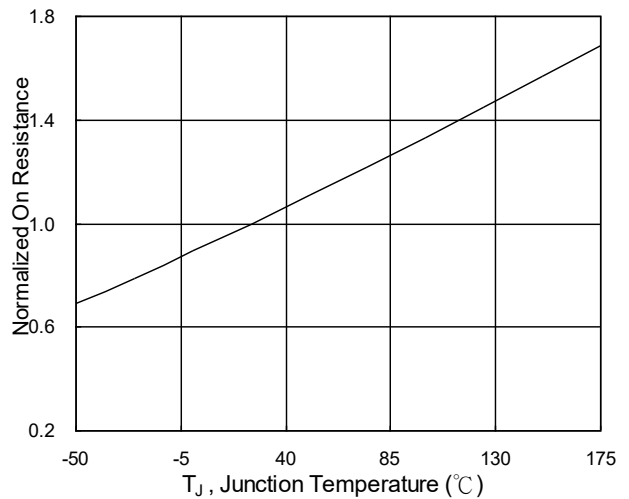


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

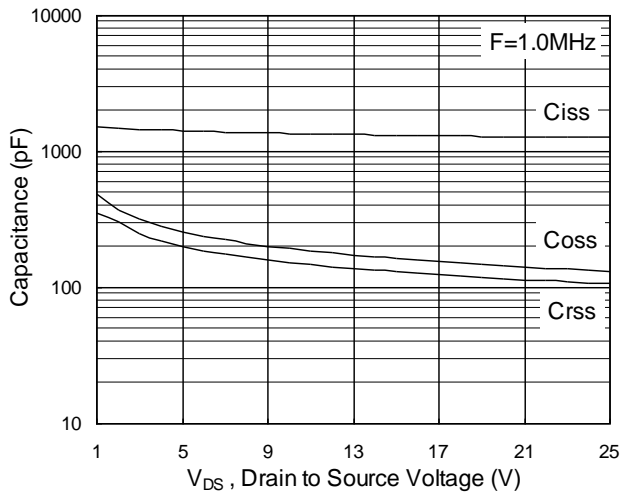


Fig.7 Capacitance

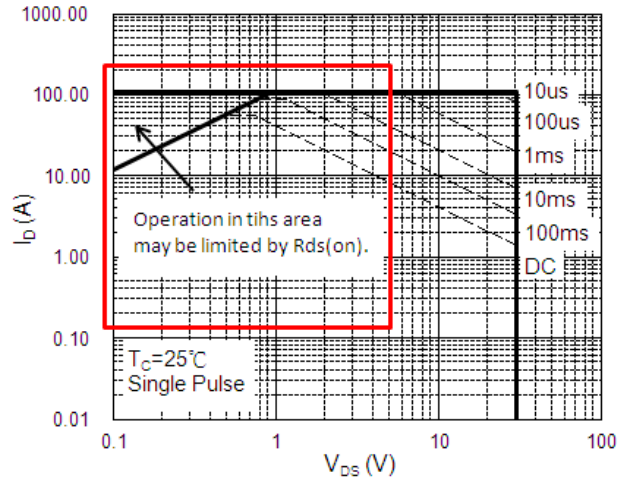


Fig.8 Safe Operating Area

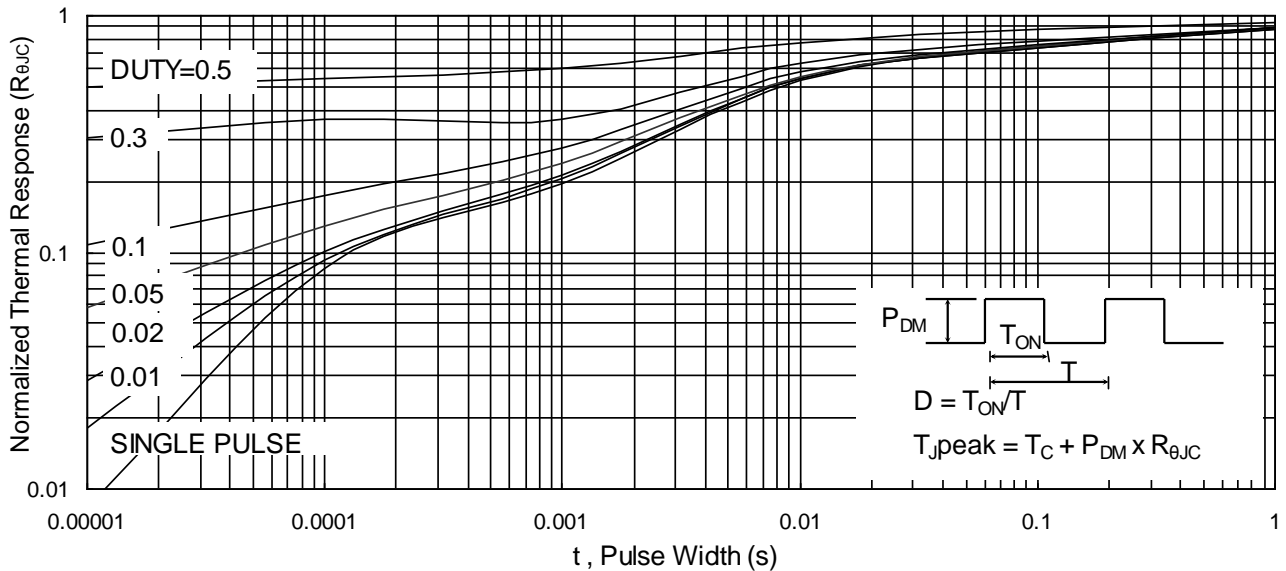


Fig.9 Normalized Maximum Transient Thermal Impedance

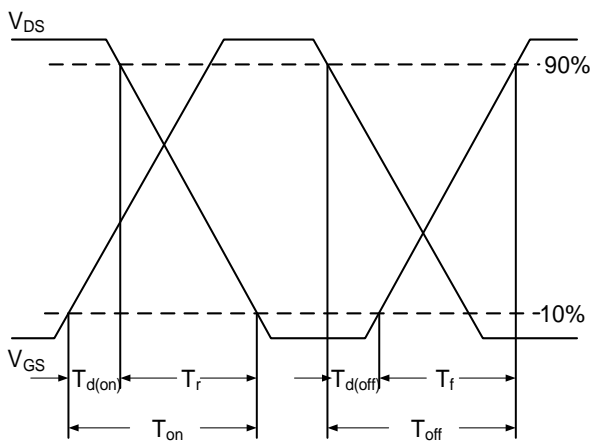


Fig.10 Switching Time Waveform

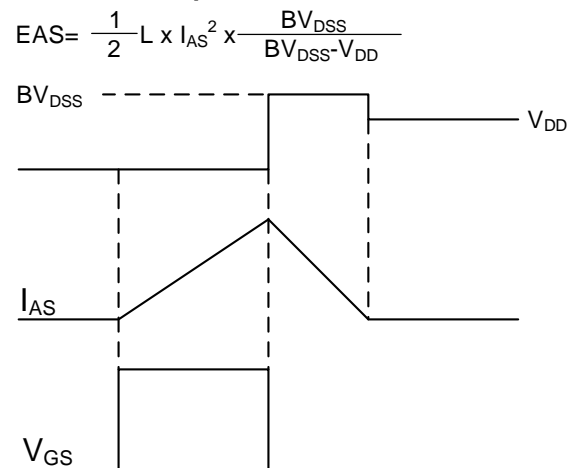


Fig.11 Unclamped Inductive Switching Waveform



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