128 Taps Digital Potentiometer with I²C Interface

Features

- Single-channel, 128-position Resolution
- INL: ±0.1 LSB
- DNL: ±0.1 LSB
- Low Temperature Coefficient: 20 ppm/°C (10 kΩ)
- I²C Serial Interface
- A and B Versions Have Different I²C Addresses
  A: 0101110; B: 0111110
- 2.7 V to 5.5 V Single Supply Operation
- Resistance Tolerance: ±20%
- Available in Industry Standard SC70-6 Packages
- Temperature Range: -40 °C to +125 °C

Applications

- Laser Gas Detector
- Mechanical Potentiometer Replacement
- Adjustable Power Supplies
- Adjustable Gain Amplifiers and Offset Trimming
- Precision Calibration of Set Point Thresholds
- Sensor Trimming and Calibration

Block Diagram

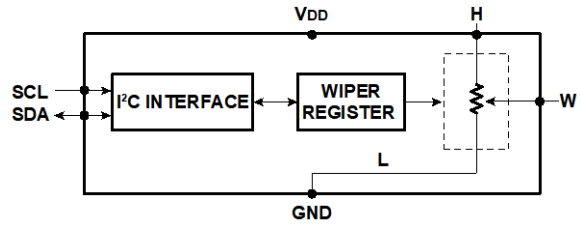

Figure 1. TPL0401 Block Diagram

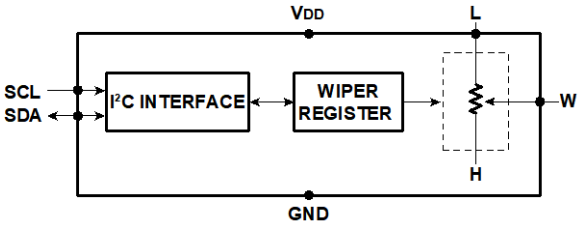

Figure 2. TPL0402 Block Diagram

Typical Characteristics

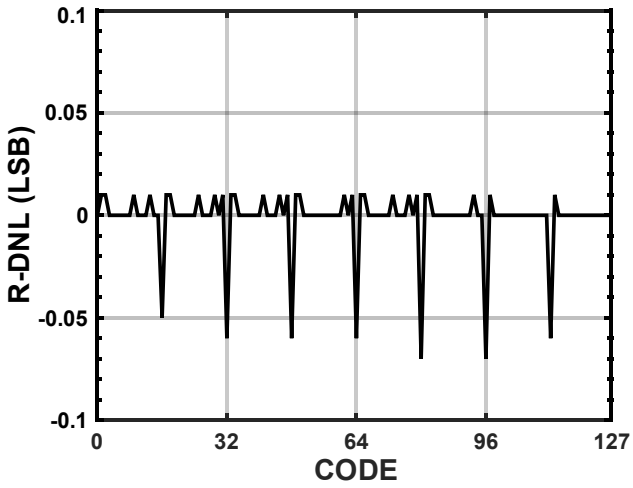

Figure 3. R-DNL vs. Code (10 kΩ)

Pin Configurations and Function Descriptions

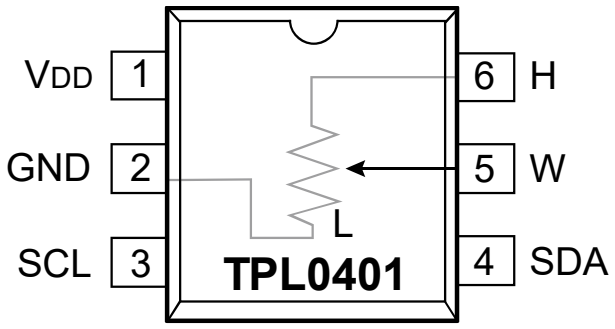

Figure 4. TPL0401 Pin Configuration (SC70-6)

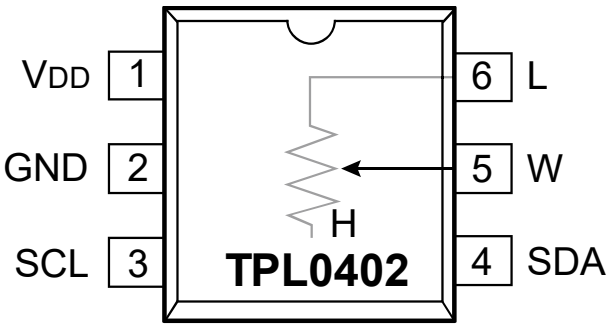

Figure 5. TPL0402 Pin Configuration (SC70-6)

Mnemonic	Pin No. (TPL0401)	Pin No. (TPL0402)	I/O[1]	Description
V_{DD}	1	1	P	Positive Supply Voltage
GND	2	2	G	Ground
SCL	3	3	DI	I²C Clock
SDA	4	4	DI/O	I²C Data
W	5	5	AI/O	Wiper Terminal
H	6	--	AI/O	High Terminal (Internally floating in TPL0402)
L	--	6	AI/O	Low Terminal (Internally connected to GND in TPL0401)

[1] AI: Analog Input; AO: Analog Output; P: Power; G: Ground; DI: Digital Input; DO: Digital Output.

Absolute Maximum Ratings[1]

Parameter	Rating
Supply Voltage, V_{DD} to GND	-0.3 V to + 7 V
Continuous Current, I_A, I_B, I_W	±3 mA (10k version) ±1 mA (100k version)
Digital Input Pins (SDA, SCL)	-0.3 V to (V_{DD} + 0.3 V)
Analog Pins (H, W, L)	-0.3 V to (V_{DD} + 0.3 V)
Operating Temperature Range	-40 °C to +125 °C
Storage Temperature Range	-65 °C to +150 °C
Junction Temperature Range	150 °C
Electrostatic Discharge (ESD)[2]	
Human Body Model (HBM)[3]	±5 kV
Charged Device Model (CDM)[4]	±2 kV

Thermal Resistance[5]

Package Type	θ_{JA}	θ_{JC}	Unit
SC70-6	235	112	°C/W

[1] These ratings apply at 25°C, unless otherwise noted. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

[2] Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[3] ANSI/ESDA/JEDEC JS-001 Compliant.

[4] ANSI/ESDA/JEDEC JS-002 Complaint

[5] θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications (10k version)

The ● denotes the full temperature range (-40 °C to +125 °C) for specified performance. Unless otherwise noted, T_A = 25 °C and V_{DD} = 5.0 V.

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
End-to-end Resistance	R_{TOTAL}				10		kΩ
Terminal Resistance	R_H/R_L				50		Ω
Wiper Resistance	R_W				50		Ω
Terminal Capacitance	C_H/C_L				6		pF
Wiper Capacitance	C_W				8		pF
Resistance Temperature Coefficient	TC_R				20		ppm/°C
V_{DD} Standby Current	$I_{DD(STBY)}$					3	µA
Digital pins Leakage Current (SCL, SDA Inputs)	I_{IN-DIG}					0.2	µA
Serial Interface Specs (SDA, SCL)							
Input High Voltage	V_{IH}		●	0.7×V_{DD}		V_{DD}	V
Input Low Voltage	V_{IL}		●	0		0.3×V_{DD}	V
Output Low Voltage	V_{OL}	SDA Pin, I_{OL} = 4 mA	●			0.3	V
Pin Capacitance	C_{IN}	SCL, SDA Inputs	●		4		pF
Voltage Divider Mode (V_H = V_{DD}, V_W = Not Loaded), only for TPL0401A/B							
Integral Non-linearity	INL[1,2]				±0.1		LSB
Differential Non-linearity	DNL[2,3]				±0.1		LSB
Zero-scale Error	ZS_{ERROR}[4,5]				0.5		LSB
Full-scale error	FS_{ERROR}[5,6]				-0.5		LSB
Ratiometric Temperature Coefficient	T_{CV}	Wiper set at mid-scale			3		ppm/°C
Bandwidth	BW	Wiper set at mid-scale, C_{LOAD} = 10 pF			3500		kHz
Wiper Settling Time	T_{SW}				0.2		µs
Total Harmonic Distortion	THD	V_H = 1 V_{RMS} at 1 kHz, measurement at W			0.013		%
Rheostat Mode (V_H = V_{DD}, V_W = Not Loaded)							
Rheostat-mode Integral Non-linearity	RINL[7,8]				±0.1		LSB
Rheostat-mode Differential Non-linearity	RDNL[8,9]				±0.1		LSB
Rheostat-mode Zero Scale Error	R_{OFFSET}[10,11]				1.0		LSB

[1] INL = ($V_{MEAS[code\ x]}$ – $V_{MEAS[code\ 0]}$) / LSB – [code x]
[2] LSB = ($V_{MEAS[code\ 127]}$ – $V_{MEAS[code\ 0]}$) / 127
[3] DNL = ($V_{MEAS[code\ x]}$ – $V_{MEAS[code\ x-1]}$) / LSB – 1
[4] ZS_{ERROR} = $V_{MEAS[code\ 0]}$ / IDEAL_LSB
[5] IDEAL_LSB = V_H / 127
[6] FS_{ERROR} = ($V_{MEAS[code\ 127]}$ – V_H) / IDEAL_LSB
[7] RINL = ($R_{MEAS[code\ x]}$ – $R_{MEAS[code\ 0]}$) / RLSB – [code x]
[8] RLSB = ($R_{MEAS[code\ 127]}$ – $R_{MEAS[code\ 0]}$) / 127
[9] RDNL = ($R_{MEAS[code\ x]}$ – $R_{MEAS[code\ x-1]}$) / RLSB – 1
[10] R_{OFFSET} = $R_{MEAS[code\ 0]}$ / IDEAL_RLSB
[11] IDEAL_RLSB = R_{TOT} / 127

Specifications (100k version)

The • denotes the full temperature range (-40 °C to +125 °C) for specified performance. Unless otherwise noted, T_A = 25 °C and V_{DD} = 5.0 V.

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
End-to-end Resistance	R_{TOTAL}				100		kΩ
Terminal Resistance	R_H/R_L				50		Ω
Wiper Resistance	R_W				50		Ω
Terminal Capacitance	C_H/C_L				6		pF
Wiper Capacitance	C_W				8		pF
Resistance Temperature Coefficient	TC_R				5		ppm/°C
V_{DD} Standby Current	$I_{DD(STBY)}$					3	µA
Digital pins Leakage Current (SCL, SDA Inputs)	I_{IN-DIG}					0.2	µA
Serial Interface Specs (SDA, SCL)							
Input High Voltage	V_{IH}		•	0.7×V_{DD}		V_{DD}	V
Input Low Voltage	V_{IL}		•	0		0.3×V_{DD}	V
Output Low Voltage	V_{OL}	SDA Pin, I_{OL} = 4 mA	•			0.3	V
Pin Capacitance	C_{IN}	SCL, SDA Inputs	•		4		pF
Voltage Divider Mode (V_H = V_{DD}, V_W = Not Loaded), only for TPL0401B-100							
Integral Non-linearity	INL[1,2]				±0.1		LSB
Differential Non-linearity	DNL[2,3]				±0.1		LSB
Zero-scale Error	ZS_{ERROR}[4,5]				0.05		LSB
Full-scale error	FS_{ERROR}[5,6]				-0.05		LSB
Ratiometric Temperature Coefficient	T_{CV}	Wiper set at mid-scale			2		ppm/°C
Bandwidth	BW	Wiper set at mid-scale, C_{LOAD} = 10 pF			350		kHz
Wiper Settling Time	T_{SW}				0.2		µs
Total Harmonic Distortion	THD	V_H = 1 V_{RMS} at 1 kHz, measurement at W			0.006		%
Rheostat Mode (V_H = V_{DD}, V_W = Not Loaded)							
Rheostat-mode Integral Non-linearity	RINL[7,8]				±0.1		LSB
Rheostat-mode Differential Non-linearity	RDNL[8,9]				±0.1		LSB
Rheostat-mode Zero Scale Error	R_{OFFSET}[10,11]				0.1		LSB

[1] INL = ($V_{MEAS[code\ x]}$ – $V_{MEAS[code\ 0]}$) / LSB – [code x]
[2] LSB = ($V_{MEAS[code\ 127]}$ – $V_{MEAS[code\ 0]}$) / 127
[3] DNL = ($V_{MEAS[code\ x]}$ – $V_{MEAS[code\ x-1]}$) / LSB – 1
[4] ZS_{ERROR} = $V_{MEAS[code\ 0]}$ / IDEAL_LSB
[5] IDEAL_LSB = V_H / 127
[6] FS_{ERROR} = ($V_{MEAS[code\ 127]}$ – V_H) / IDEAL_LSB
[7] RINL = ($R_{MEAS[code\ x]}$ – $R_{MEAS[code\ 0]}$) / RLSB – [code x]
[8] RLSB = ($R_{MEAS[code\ 127]}$ – $R_{MEAS[code\ 0]}$) / 127
[9] RDNL = ($R_{MEAS[code\ x]}$ – $R_{MEAS[code\ x–1]}$) / RLSB – 1
[10] R_{OFFSET} = $R_{MEAS[code\ 0]}$ / IDEAL_RLSB
[11] IDEAL_RLSB = R_{TOT} / 127

Timing Requirements

		Min	Max	Unit
Standard Mode				
I²C Clock Frequency	F_{scl}	0	100	kHz
I²C Clock High Time	T_{sch}	4		µs
I²C Clock Low Time	T_{scl}	4.7		µs
I²C Spike Time	T_{sp}	0	50	ns
I²C Serial Data Setup Time	T_{sds}	250		ns
I²C Serial Data Hold Time	T_{sdh}	0		ns
I²C Input Rise Time	T_{icr}		1000	ns
I²C Input Fall Time	T_{icf}		300	ns
I²C Output Fall Time, 10 pF to 400 pF Bus	T_{ocf}		300	ns
I²C Bus Free Time between Stop and Start	T_{buf}	4.7		µs
I²C Start or Repeater Start Condition Setup Time	T_{sts}	4.7		µs
I²C Start or Repeater Start Condition Hold Time	T_{sth}	4		µs
I²C Stop Condition Setup Time	T_{sps}	4		µs
Valid Data Time, SCL Low to SDA Output Valid	T_{vd}		1	µs
Valid Data Time of ACK Condition, ACK Signal from SCL Low to SDA (out) Low	$T_{vd(ack)}$		1	µs
Fast Mode				
I²C Clock Frequency	F_{scl}	0	400	kHz
I²C Clock High Time	T_{sch}	0.6		µs
I²C Clock Low Time	T_{scl}	1.3		µs
I²C Spike Time	T_{sp}	0	50	ns
I²C Serial Data Setup Time	T_{sds}	100		ns
I²C Serial Data Hold Time	T_{sdh}	0		ns
I²C Input Rise Time	T_{icr}	20	300	ns
I²C Input Fall Time	T_{icf}	$20 \times (V_{DD} / 5.5)$	300	ns
I²C Output Fall Time, 10 pF to 400 pF Bus	T_{ocf}	$(V_{DD} / 5.5) \times 20$	300	ns
I²C Bus Free Time between Stop and Start	T_{buf}	1.3		µs
I²C Start or Repeater Start Condition Setup Time	T_{sts}	1.3		µs
I²C Start or Repeater Start Condition Hold Time	T_{sth}	0.6		µs
I²C Stop Condition Setup Time	T_{sps}	0.6		µs
Valid Data Time, SCL Low to SDA Output Valid	T_{vd}		1	µs
Valid Data Time of ACK Condition, ACK Signal from SCL Low to SDA (out) Low	$T_{vd(ack)}$		1	µs

Start	Slave Address(01x1110)	0	ACK	Register Address (00000000)	ACK	Data	ACK	Stop

Figure 6. I²C Interface 3-Byte Write

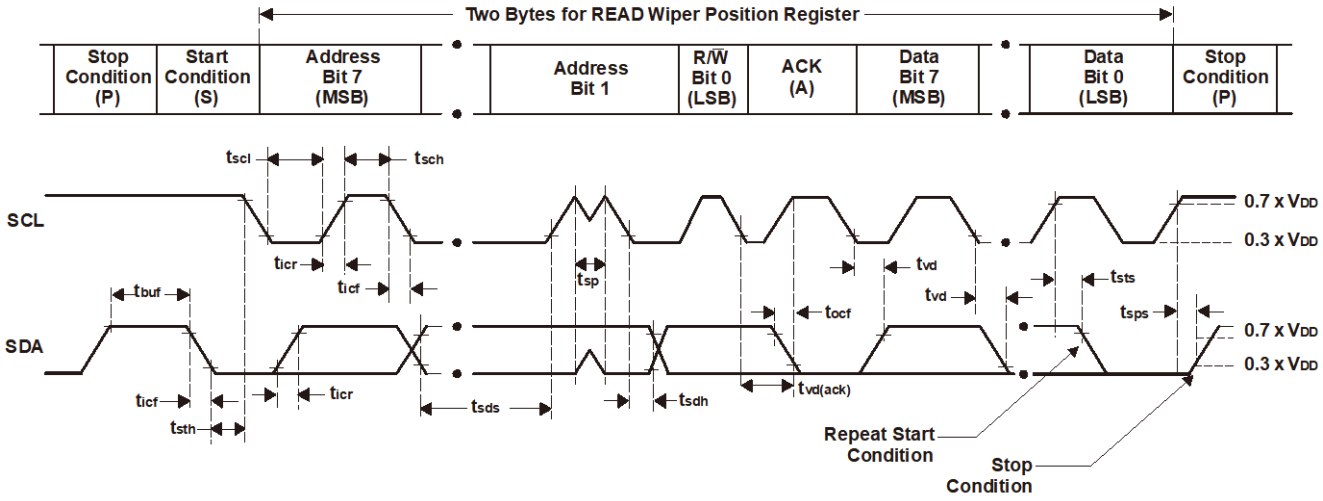

Figure 7. I²C Interface Read Timing

Start	Slave Address(01x1110)	1	ACK	Data Back	noACK	Stop

Figure 8. I²C Interface 2-Byte Read (Short Mode)

Start	Slave Address(01x1110)	0	ACK	Register Address (00000000)	ACK	reStart	Slave Address(01x1110)	1	ACK	Data Back	noACK	Stop

Figure 9. I²C Interface Read

Typical Performance Characteristics

Unless otherwise stated, T_A = 25 °C, V_{DD} = 5.0 V.

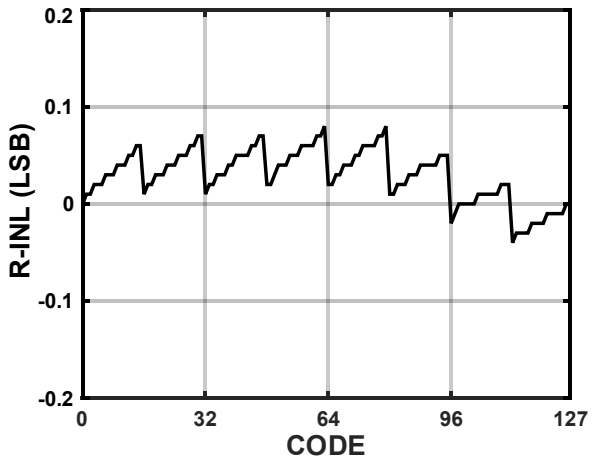

Figure 10. Rheostat-INL vs. Code (10 kΩ)

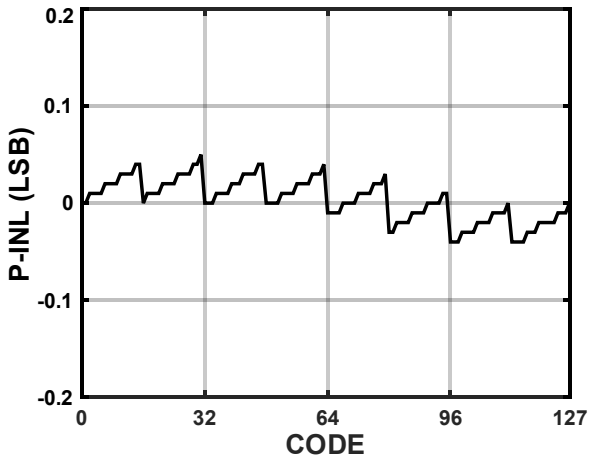

Figure 11. Potentio-INL vs. Code (10 kΩ)

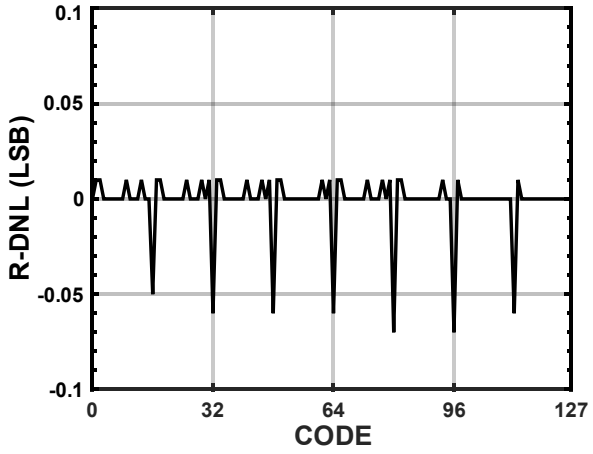

Figure 12. Rheostat-DNL vs. Code (10 kΩ)

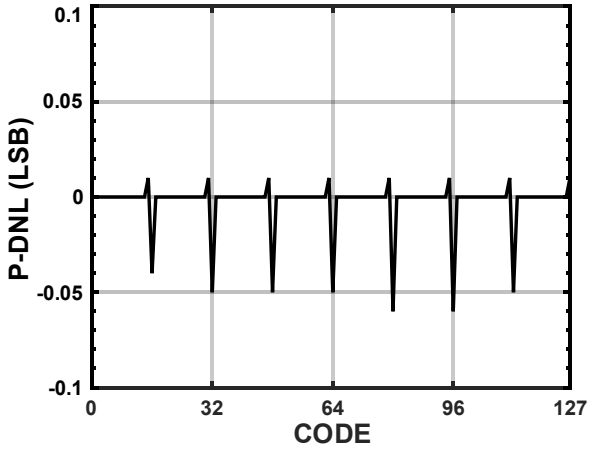

Figure 13. Potentio-DNL vs. Code (10 kΩ)

Serial Interface

Communications from the controller to the TPL0401A/B digital potentiometers is by using the I²C serial interface.

Write Operation

To write on the I²C bus, the master sends a START condition on the bus with the address of the slave, as well as the last bit (the R/W bit) set to 0, which signifies a write. After the slave responds with an acknowledge, the master then sends the register address byte which is 0x00. The slave acknowledges again, letting the master know that it is ready. After this, the master starts sending the register data (LSB 7 bits are used) to the slave until the master has sent all the data necessary (which is sometimes only a single byte), and the master terminates the transmission with a STOP condition.

Start	Slave Address(01x1110)	0	ACK	Register Address (00000000)	ACK	Data	ACK	Stop

Figure 14. I²C Interface 3-Byte Write

Read Operation

Reading from a slave is very similar to writing, but requires some additional steps. in order to read from a slave, the master must first instruct the slave with the register address it wishes to read from. This is done by the master starting off the transmission in a similar fashion as the write, by sending the address with the R/W bit equal to 0 (signifying a write), followed by the register address it wishes to read from. When the slave acknowledges this register address, the master sends a START (or repeat START) condition again, followed by the slave address with the R/W bit set to 1 (Signifying a read). This time, the slave acknowledges the read request, and the master releases the SDA bus but continues supplying the clock to the slave. The master continues to send out the clock pulses, for each byte of data that it wishes to receive. At the end of every byte of data, the master sends an ACK to the slave, letting the slave know that it is ready for more data.

When the master has received the number of bytes it was expecting (or needs to stop communication), it should send a NACK, signaling to the slave to halt communications and release the bus. The master follows this up with a STOP condition.

Start	Slave Address(01x1110)	0	ACK	Register Address (00000000)	ACK	reStart	Slave Address(01x1110)	1	ACK	Data Back	noACK	Stop

Figure 15. I²C Interface Read

It is also possible to read the register data back with 2 bytes, as shown below.

Start	Slave Address(01x1110)	1	ACK	Data Back	noACK	Stop

Figure 16. I²C Interface 2-Byte Read (Short Mode)

Programming the Variable Resistor

Rheostat Operation—±20% Resistor Tolerance

When the TPL0401A/B operates in rheostat mode, only two terminals are used as a variable resistor.

The nominal resistance between Terminal H (internally) and Terminal L, R_{HL}, is 10 kΩ or 100 kΩ, and has 128 tap points accessed by the wiper terminal. The 7-bit data in the RDAC latch is decoded to select one of the 128 possible wiper settings. The general equation for determining the digitally programmed output resistance between Terminal W and Terminal L is

$$R_{WL}(D) = \frac{D}{128} \times R_{HL} + R_W \quad From\ 0x00\ to\ 0x7F$$

where:

- D is the decimal equivalent of the binary code in the 7-bit RDAC register.
- R_{HL} is the end to end resistance.
- R_W is the wiper resistance.

Outline Dimensions

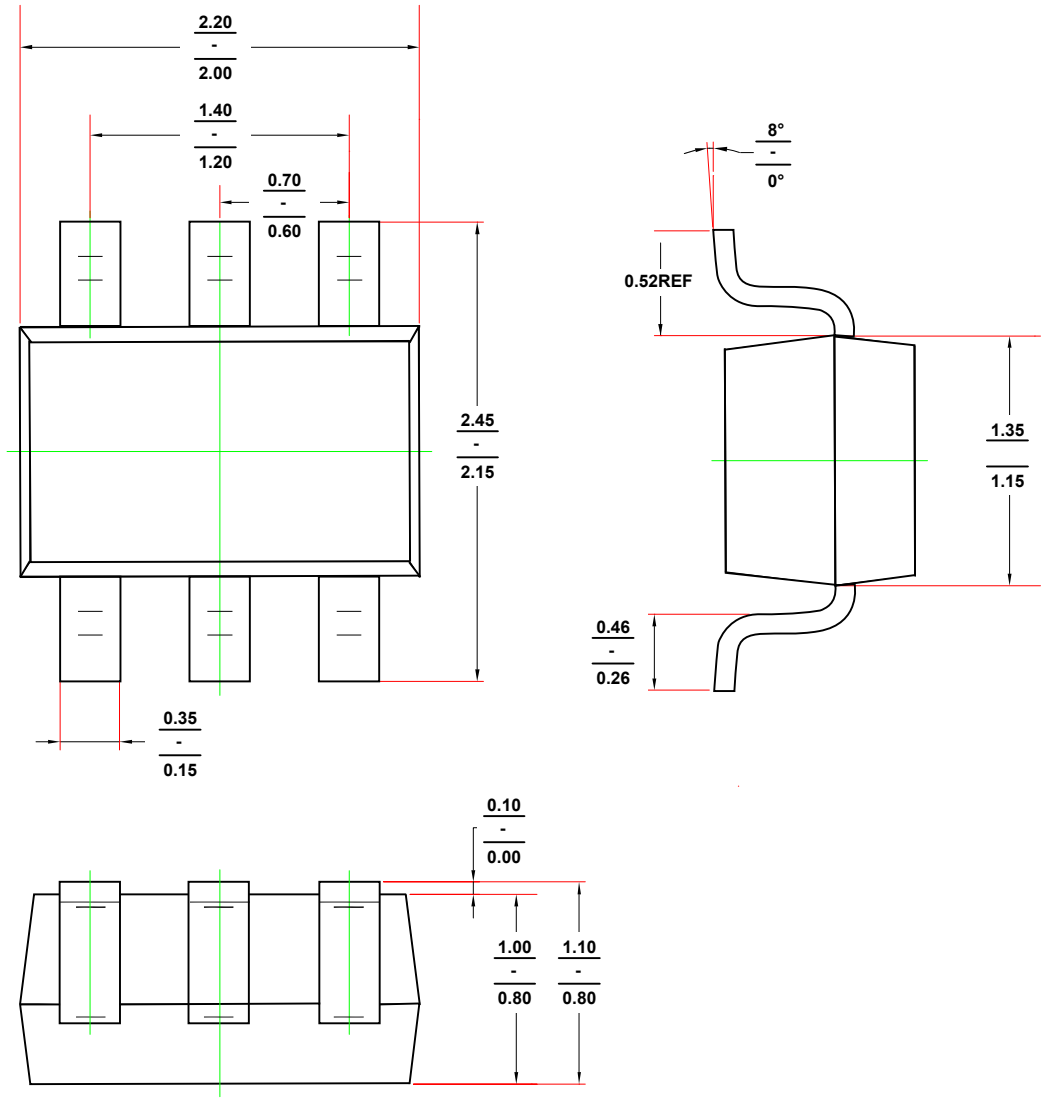

Figure 17. 6-lead SC70 Package Dimensions Shown in Millimeters

Ordering Guide

Model	Orderable Device	Marking (NN: Date Code)	End-to-End Resistance (Ω)	I²C Address	Package	External Package
TLP0401	TPL0401A-10DCKR	01NN	10k	0101110	SC70-6	7” Reel
	TPL0401B-10DCKR	02NN	10k	0111110		
	TPL0401A-100DCKR	05NN	100k	0101110		
	TPL0401B-100DCKR	06NN	100k	0111110		
TLP0402	TPL0402A-10DCKR	03NN	10k	0101110		
	TPL0402B-10DCKR	04NN	10k	0111110		
	TPL0402A-100DCKR	07NN	100k	0101110		
	TPL0402B-100DCKR	08NN	100k	0111110		