



JSC6288

**250V 3-Phase Gate Driver
User Manual**

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1. Description

JSC6288 is an integrated three-independent half-bridge gate driver IC designed for high voltage, high speed drive MOSFETs ,with an operating voltage up to +250V.

JSC6288 has a built-in VCC/VBS under-voltage protection (UVLO) function to prevent the power transistors from operating at too low a voltage.

JSC6288 has built-in shoot-through prevention and dead time to prevent shoot-through of the driven high and low side MOSFET or IGBT, effectively protecting power devices.

JSC6288 is equipped with built-in input signal filtering to prevent input noise interference.

2. Key Features

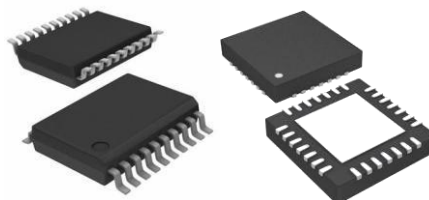
- Suspension absolute voltage + 250V
- Gate driver supply range from 5V to 20V
- Integrated three-independent half-bridge gate driver
- Transient pulse current +1.3A/-1.5A
- 3.3V/5V logic input compatible
- VCC/VBS under-voltage protection (UVLO)
- Internal shoot-through prevention
- Internal dead time of 250 ns
- Integrated input filter function
- Outputs in phase with inputs

3. Application

Three-phase brushless DC motor drive

4. Packages

Packaging as shown in the following figure

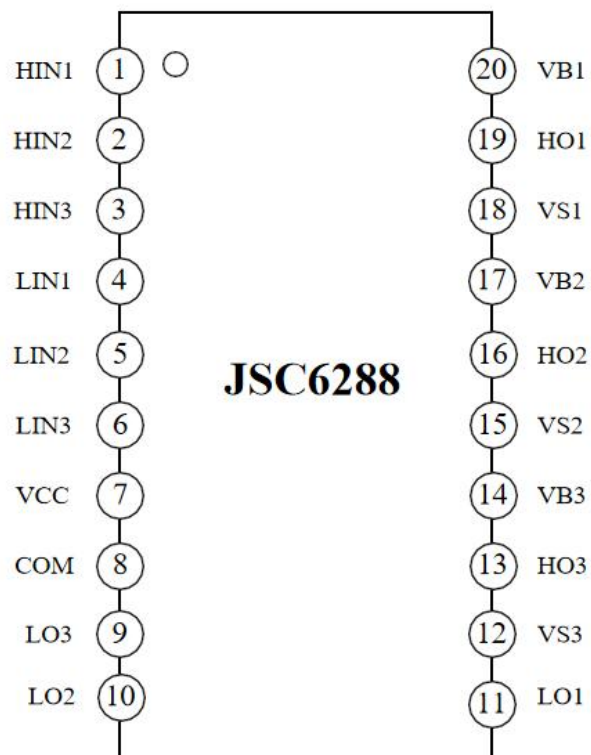


Product name	Packaging forms	Model
JSC6288CTS20(BD)	TSSOP20	JSC6288CTS20
JSC6288QFN24(BD)	QFN24	JSC6288QFN24

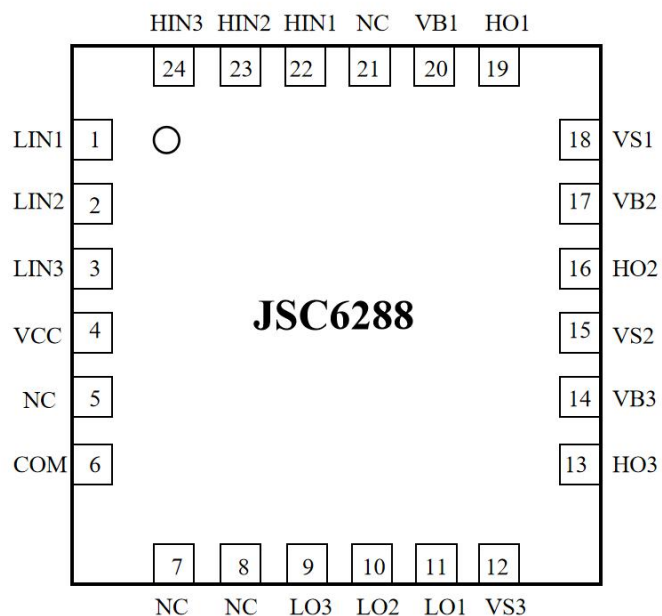
5. Lead Configuration

5.1. Lead Assignments

TSSOP20



QFN24



5.2. Lead Definitions

TSSOP20

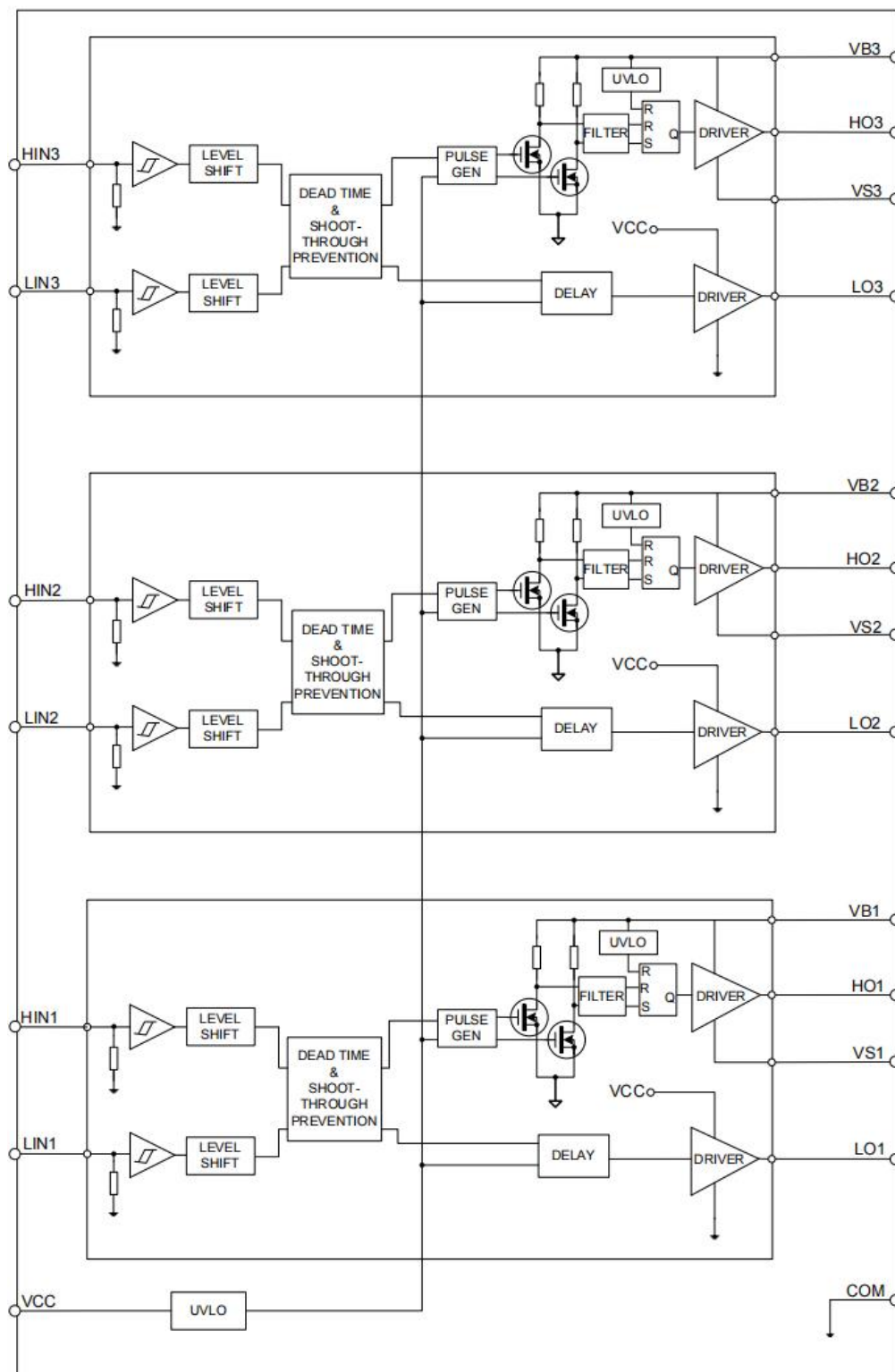
Number	Symbol	Description
1,2,3	HIN1,HIN2,HIN3	High side input
4,5,6	LIN1,LIN2,LIN3	Low side input
7	VCC	Low side supply
8	COM	Low side return
9,10,11	LO3,LO2,LO1	Low side gate drive output
12,15,18	VS3,VS2,VS1	High side floating supply return
13,16,19	HO3,HO2,HO1	High side gate drive output
14,17,20	VB3,VB2,VB1	High side floating supply

QFN24

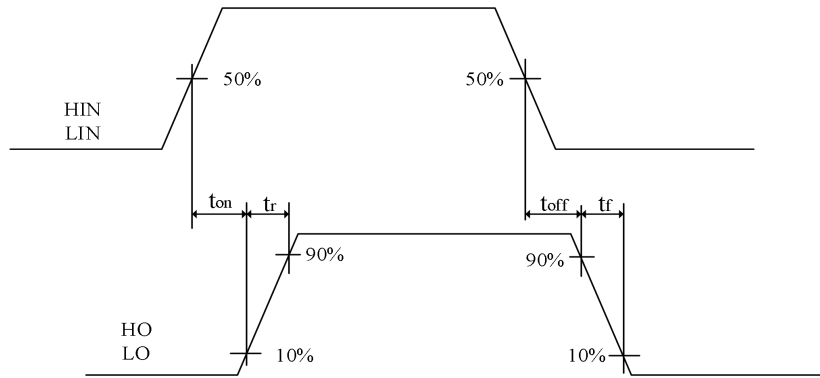
Number	Symbol	Description
22,23,24	HIN1,HIN2,HIN3	High side input
1,2,3	LIN1,LIN2,LIN3	Low side input
4	VCC	Low side supply
6	COM	Low side return
9,10,11	LO3,LO2,LO1	Low side gate drive output
12,15,18	VS3,VS2,VS1	High side floating supply return
13,16,19	HO3,HO2,HO1	High side gate drive output
14,17,20	VB3,VB2,VB1	High side floating supply
5,7,8,21	NC	No connection

6. Functional Block Diagram and Description

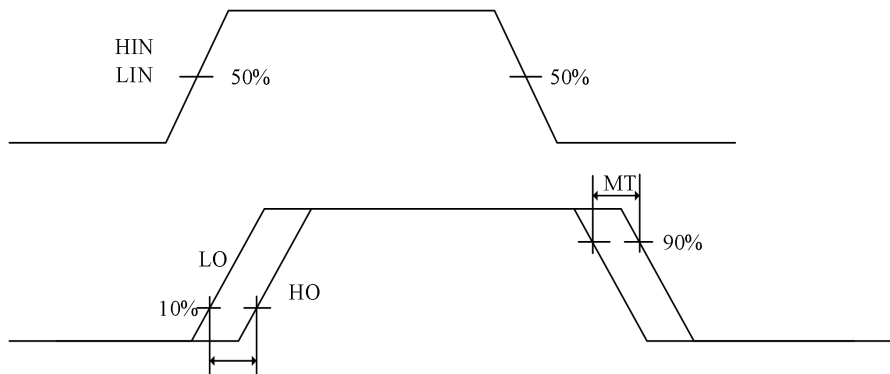
6.1. Functional Block Diagram



6.2. Switching Time Waveform Definitions

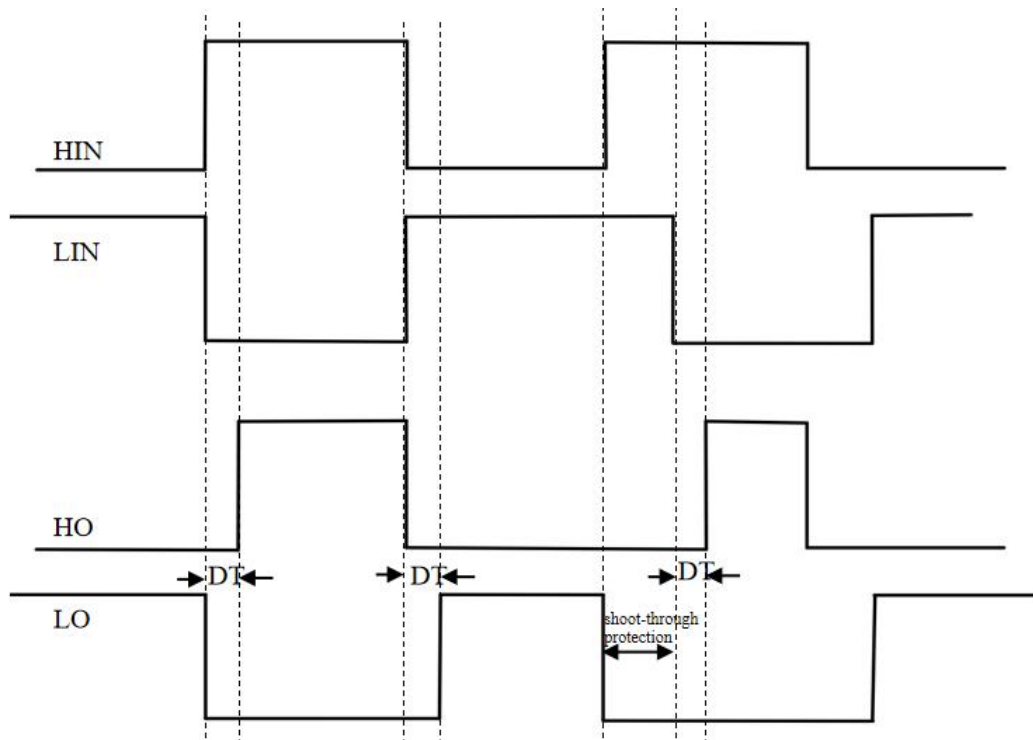


6.3. Delay Matching Waveform Definitions



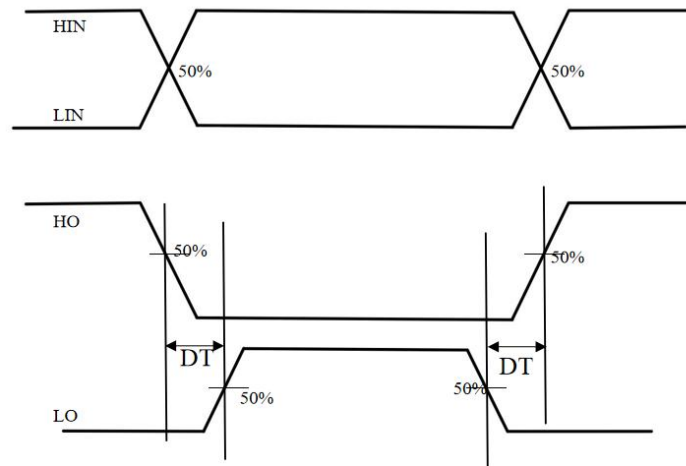
6.4. Function of Shoot-through Protection

The chip is designed with a protection circuit specifically designed to prevent power transistors direct current. This design can effectively prevent direct current damage to the power transistor caused by interference on the high-side and low-side input signals. The working principle of the shoot-through prevention circuit for power transistor protection is illustrated in the following figure.



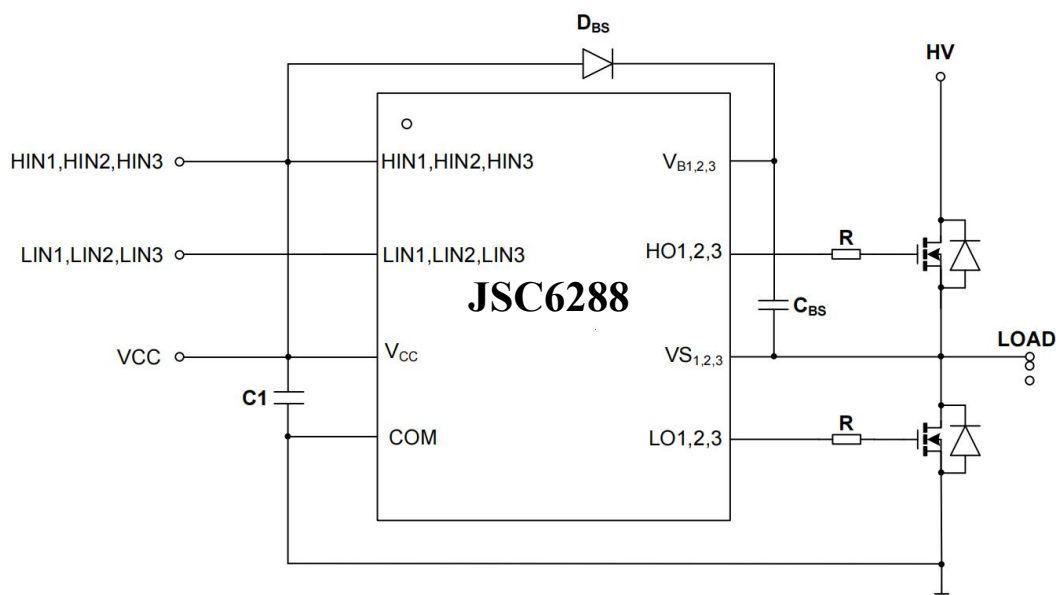
6.5. Deadtime Function

The chip incorporates a fixed dead time protection circuit. During the dead time period, both the high-side and low-side outputs are set to a low level. The configured dead time must ensure that one power transistor is completely turned off before the other is turned on, effectively preventing shoot-through between the upper and lower transistors. If the external dead time set by the logic input is longer than the internal dead time of the chip, the output dead time follows the externally set value. Conversely, if the external dead time set by the logic input is shorter, the chip's output dead time defaults to its internally fixed value. The timing relationship among the dead time, input signals, and driver output signals is illustrated in the following figure.



7. System Applications

The typical application diagram of JSC6288 is shown below:



C1: Power filter capacitor, according to the circuit can choose $1\mu\text{F} \sim 10\mu\text{F}$.

R: Gate drive resistor, and the resistance depends on the device being driven and deadtime.

D_{bs}: Bootstrap diodes. the diodes with high reverse breakdown voltage (> 250V) and short recovery time should be selected.

C_{bs}: Bootstrap capacitors. Ceramic capacitors or tantalum capacitors should be selected, the minimum capacitance can be calculated according to the following formula

$$C_{bs} \geq 15 \cdot \frac{2 \cdot \left[2 \cdot Q_g + Q_{period} + \frac{I_{bs(static)}}{f} + \frac{I_{bs(leak)}}{f} \right]}{V_{CC} - V_F - V_{ds(L)}}$$

Q_g is the gate charge of the high-side power device ;

Q_{period} is the charge requirement of the level conversion circuit in each cycle, which is about 10 nC ;

I_{bs (static)} is the static current of the high-side drive circuit;

I_{bs (leak)} is the leakage current of bootstrap capacitor;

f is the working frequency of the circuit;

V_{CC} is the low-side supply voltage;

V_F is the forward voltage drop of the bootstrap diode;

V_{ds (L)} is the on-state voltage drop of low-side power devices.

Note : The above lines and parameters are for reference only. The actual application circuit sets parameters according to the measured results.

8. Electrical Characteristics

8.1. Maximum Absolute Conditions

Exceeding the absolute maximum ratings of the electrical characteristics may cause permanent damage to the chip. Refer to the functional operating limits for the chip as shown in the table below. (Unless otherwise specified, all pins are referenced to COM.)

Parameter		Symbol	Range	Unit
High side floating absolute voltage		V _{B1,2,3}	-0.3~250	V
Static high-side floating offset voltage		V _{S1,2,3}	V _{B1,2,3} -25~V _{B1,2,3} +0.3	V
Dynamic high-side floating offset voltage		V _{HO1,2,3}	V _{S1,2,3} -0.3~V _{B1,2,3} +0.3	V
High-side output voltage		V _{CC}	-0.3~25	V
Low-side supply voltage		V _{LO1,2,3}	-0.3~V _{CC} +0.3	V
Logic input voltage (HIN, LIN)		V _{IN}	-0.3~V _{CC} +0.3	V
Offset voltage slew rate range		dV _S /dt	≤50	V/ns
Power dissipation@T _A ≤25℃	TSSOP20	P _D	≤1.25	W
	QFN24	P _D	≤3.0	W
Thermal resistance of paired environment	TSSOP-20	R _{thJA}	≤100	C/W
	QFN24	R _{thJA}	≤42	C/W
Junction temperature range		T _j	≤150	℃
Storage temperature range		T _{stg}	-55~150	℃

8.2. Recommended Normal Working Conditions

Do not exceed the recommended operating conditions or design to the absolute maximum ratings. (Unless otherwise specified, all pins are referenced to COM.)

Parameter	Symbol	Min	Max	Unit
High side floating absolute voltage	$V_{B1,2,3}$	$V_{S1,2,3}+4.9$	$V_{S1,2,3}+20$	V
Static high-side floating offset voltage	$V_{S1,2,3}$	COM-4 ^(Note)	250	V
High-side output voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$	$V_{B1,2,3}$	V
Low-side supply voltage	V_{CC}	5	20	V
Low-side output voltage	$V_{LO1,2,3}$	0	V_{CC}	V
Logic input voltage (HIN, LIN)	V_{IN}	0	V_{CC}	V
Ambient temperature	T_A	-40	125	C

Note: When $V_{S1,2,3}$ is (COM-4V) to 250V, HO functions properly. When $V_{S1,2,3}$ is (COM-4V) to (COM- V_{BS}), the logic state of HO is maintained.

8.3. Input Electrical Characteristics

a) Static Electrical Characteristics (Unless otherwise specified, $T_A = 25^{\circ}\text{C}$, $V_{CC} = V_{BS1,2,3} = 15\text{V}$, $V_S = \text{COM}$)

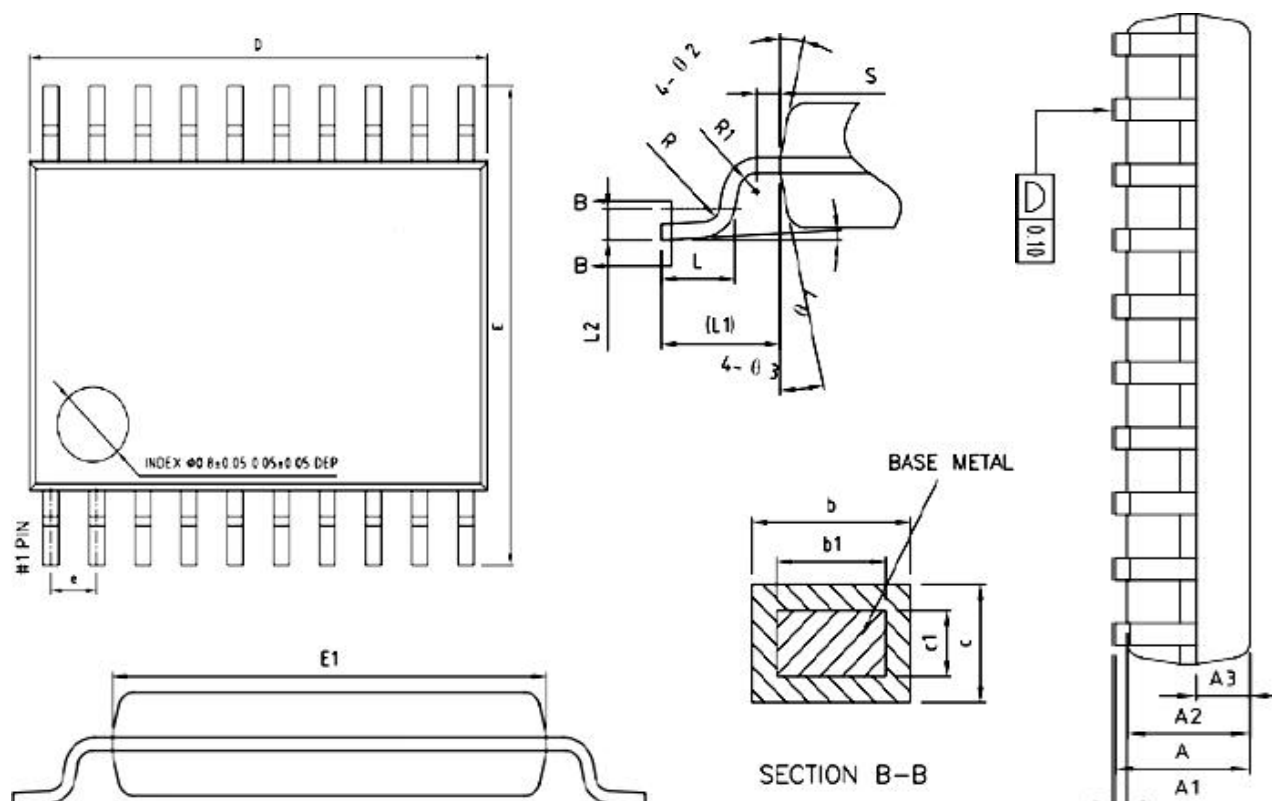
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High level input threshold voltage	V_{IH}		2.7			V
Low level input threshold voltage	V_{IL}				0.8	V
V_{CC} under-voltage protection tripping voltage	V_{CCUV+}		4.1	4.3	4.5	V
V_{CC} undervoltage protection reset voltage	V_{CCUV-}		3.8	4.0	4.2	V
V_{CC} undervoltage protection hysteresis voltage	V_{CCUVH}			0.3		V
V_{BS} undervoltage protection tripping voltage	V_{BSUV+}		4.1	4.3	4.5	V
V_{BS} undervoltage protection reset voltage	V_{BSUV-}		3.8	4.0	4.2	V
V_{BS} undervoltage protection hysteresis voltage	V_{BSUVH}			0.3		V
Leakage current of suspension power supply	I_{LK}	$V_{B1,2,3}=V_{S1,2,3}=250\text{V}$		0.1	5	μA
V_{BS} static current	I_{QBS}	$V_{IN}=0\text{V}$ or 5V		180	270	μA
V_{BS} Dynamic Current	I_{PBS}	$f_{HIN1,2,3}=20\text{kHz}$		180	270	μA
Static current of V_{CC}	I_{QCC}	$V_{IN}=0\text{V}$ or 5V		330	500	μA
V_{CC} dynamic current	I_{PCC}	$f_{LIN1,2,3}=20\text{kHz}$		330	500	μA
LIN high level input bias current	I_{LIN+}	$V_{LIN}=5\text{V}$		25	40	μA
LIN low level input bias current	I_{LIN-}	$V_{LIN}=0\text{V}$			1	μA
HIN high level input bias current	I_{HIN+}	$V_{HIN}=5\text{V}$		25	40	μA
HIN Low Level Input Bias Current	I_{HIN-}	$V_{HIN}=0\text{V}$			1	μA
Input pull-down resistance	R_{IN}		160	200	240	$\text{K}\Omega$
high level output voltage	V_{OH}	$I_O=100\text{mA}$		0.6	1	V
low level output voltage	V_{OL}	$I_O=100\text{mA}$		0.3	0.45	V
High-level output short-circuit pulse current	I_{OH}	$V_O=0\text{V}$, $V_{IN}=5\text{V}$, $\text{PWD}\leq 10\mu\text{s}$	1	1.3	1.7	A
Low-level output short-circuit pulse current	I_{OL}	$V_O=15\text{V}$, $V_{IN}=0\text{V}$, $\text{PWD}\leq 10\mu\text{s}$	1.35	1.5	2.0	A
V_S static negative pressure	V_{SN}			-6		V

b) Dynamic Electrical Characteristics (Unless otherwise specified, $T_A = 25^\circ\text{C}$, $V_{CC} = V_{BS1,2,3} = 15\text{V}$, $V_S = \text{COM}$)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output rising edge transmission time	t_{on}		-	380	450	ns
Output falling edge transmission time	t_{off}		-	130	180	ns
Output rise time	t_r	$C_L=1000\text{pF}$	-	12	25	ns
Output drop time	t_f	$C_L=1000\text{pF}$	-	12	25	ns
High and low side delay matching	MT		-	-	30	ns
Dead time	DT		100	250	300	ns

9. Package Size Diagram

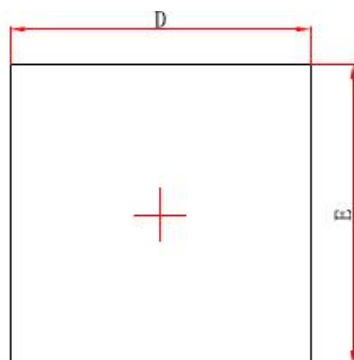
9.1. TSSOP20



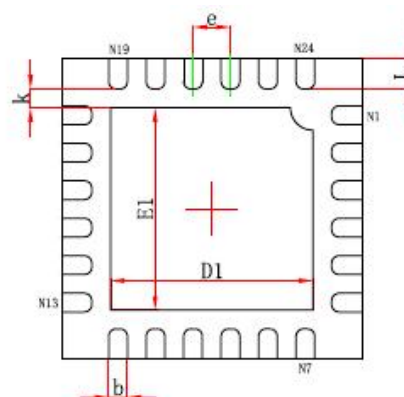
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
b1	0.19	0.22	0.25
c	0.09	—	0.20
c1	0.09	—	0.16
D	6.40	6.50	6.60
E	6.20	6.40	6.60

E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		

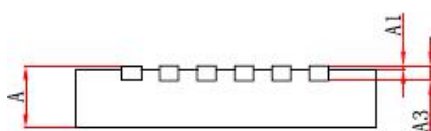
9.2. QFN24



Top View



Bottom View



Side View

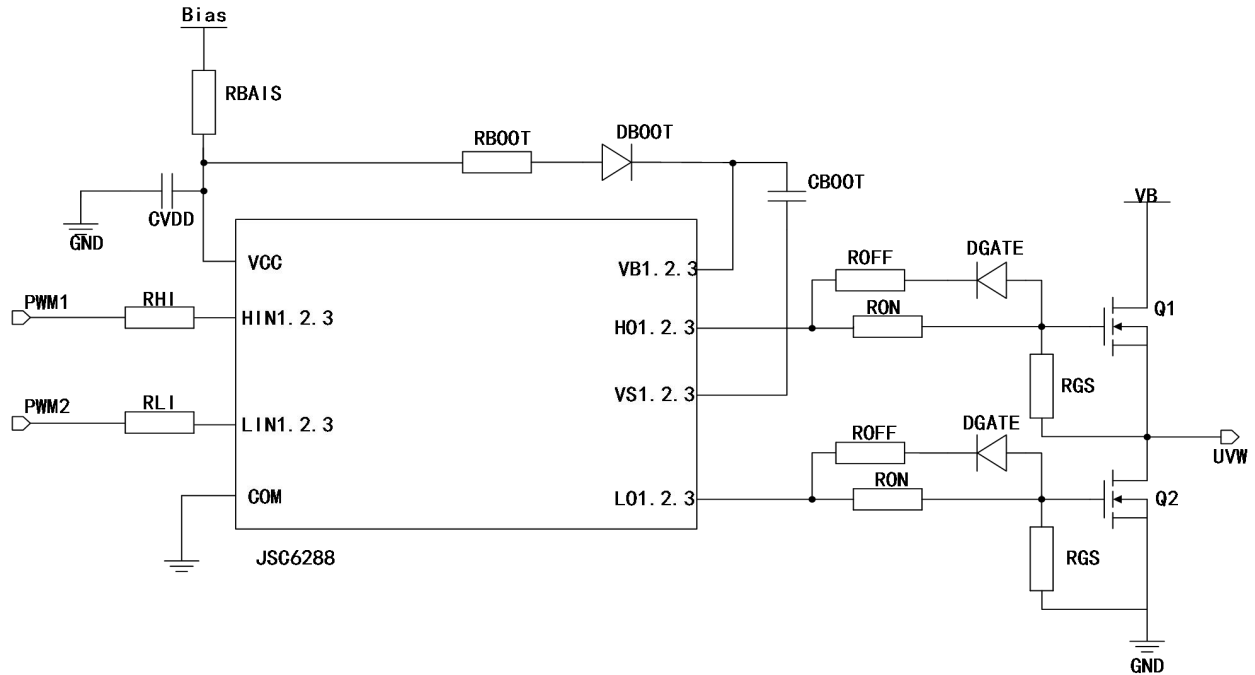
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.0031/0.0035
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
D1	2.600	2.800	0.102	0.110
E1	2.600	2.800	0.102	0.110
K	0.200MN		0.008MN	
B	0.200	0.300	0.008	0.012
E	0.500TYP		0.020TYP	
L	0.324	0.476	0.013	0.019

10. Software Description

Program the control software to meet the actual operating conditions.

11. Application Development Board

The example diagram is a 24 V BLDC motor drive circuit, and the driving MOS transistor should be as large as possible. Meet the demand of output large current.



Revision History

Date	Revision	Description	Author
2026.1.14	V1.0		

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