

1. 特性

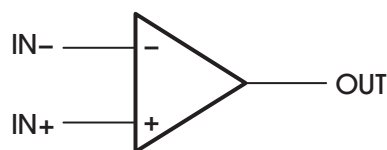
- 宽供电范围：1.7 V 到 5.5V
- -40°C 至+125°C 工作温度
- 无交越失真
- 低电源电流
 - OPL321: 70μA (Typ)
 - OPL358: 140μA (Typ)
 - OPL324: 250μA (Typ)
- 输入输出轨至轨
- ESD 保护超过
 - 3000V 人体模型
 - 1000V 带电器件模型

2. 应用

- 台式电脑
- HVAC：供暖、通风和空调
- 电机控制：交流感应
- 上网本
- 便携式媒体播放器
- 电源：电信 DC/DC 模块：数字
- 专业混音器
- 冰箱
- 洗衣机：高端和低端

3. 说明

OPL321、OPL358 和 OPL324 器件是具有轨至轨输入和输出的单路、双路和四路低压(1.7V 至 5.5V)运算放大器。这些器件对于需要低电压运行、节省空间和低成本的应用来说是最具成本效益的解决方案。这些放大器专为低电压(1.7V 至 5V)操作，可用于各种应用。有关订购信息，请参见 Table 1。



Simplified Schematic

Table 1 lists the order information.

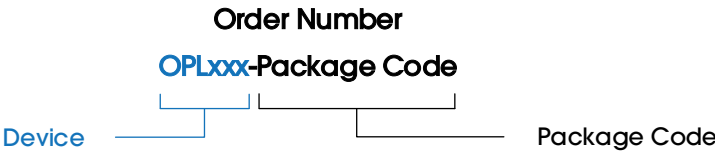
Table 1. Order Information

ORDER NUMBER ⁽¹⁾	CH (#)	PACKAGE	MARK	I _Q PER CH (TYP) (μA)	GBW (kHz)	SLEW RATE (TYP) (V/μs)	NOISE NV/√Hz (kHz)	OPERATING TEMP (°C)	PACKAGE OPTION	MSL
OPL321ASOT235 ⁽²⁾	1	SOT23-5		70	1300	0.7	40	−40-125		
OPL321ASC70 ⁽²⁾	1	SC70		70	1300	0.7	40	−40-125		
OPL358ASOIC8	2	SOIC-8	OPL358 XXXXXX ⁽³⁾	70	1300	0.7	40	−40-125	T/R-4000	2
OPL358AMSOP8	2	MSOP-8	OPL358 XXXXXX ⁽³⁾	70	1300	0.7	40	−40-125	T/R-4000	2
OPL358ATSSOP8 ⁽²⁾	2	TSSOP-8		70	1300	0.7	40	−40-125		
OPL324ASOIC14	4	SOIC-14	OPL324 XXXXXX ⁽³⁾	63	1300	0.7	40	−40-125	T/R-2500	2
OPL324ATSSOP14	4	TSSOP-14	OPL324 XXXXXX ⁽³⁾	63	1300	0.7	40	−40-125	T/R-4000	2

Devices can be ordered via the following two ways:

- Place orders directly on our website (www.analogysemi.com), or;
- Contact our sales team by mailing to sales@analogysemi.com.

Note 1:



Note 2: Available in the future.

Note 3: "XXXXXX": For internal use.

4. PIN CONFIGURATION AND FUNCTIONS

4.1 SOT23-5 AND SC70 PACKAGES

Figure 1 illustrates the pin configuration of the SOT23-5 and SC70 packages.

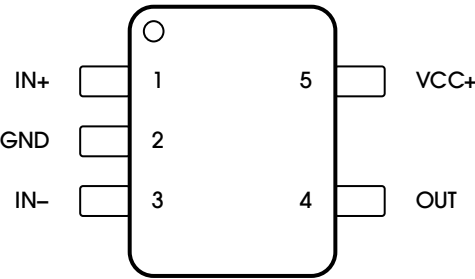


Figure 1. Pin Configuration (SOT23-5 and SC70 Packages)

Table 2 lists the pin functions of the SOT23-5 and SC70 packages.

Table 2. Pin Functions (SOT23-5 and SC70 Packages)

POSITION	NAME	TYPE	DESCRIPTION
1	IN+	Input	Noninverting input
2	GND	Power	Negative supply
3	IN-	Input	Inverting input
4	OUT	Output	Output
5	VCC+	Power	Positive supply

4.2 SOIC-8, MSOP-8, AND TSSOP-8 PACKAGES

Figure 2 illustrates the pin configuration of the SOIC-8, MSOP-8, and TSSOP-8 packages.

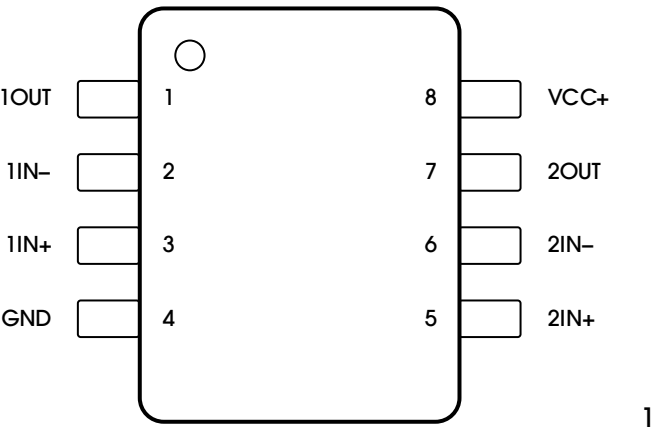


Figure 2. Pin Configuration (SOIC-8, MSOP-8, and TSSOP-8 Packages)

Table 3 lists the pin functions of the SOIC-8, MSOP-8, and TSSOP-8 packages.

Table 3. Pin Functions (SOIC-8, MSOP-8, and TSSOP-8 Packages)

POSITION	NAME	TYPE	DESCRIPTION
1	1OUT	Output	Output
2	1IN-	Input	Inverting input
3	1IN+	Input	Noninverting input
4	GND	Power	Negative supply
5	2IN+	Input	Noninverting input
6	2IN-	Input	Inverting input
7	2OUT	Output	Output
8	VCC+	Power	Positive supply

4.3 SOIC-14 AND TSSOP-14 PACKAGES

Figure 3 illustrates the pin configuration of the SOIC-14 and TSSOP-14 packages.

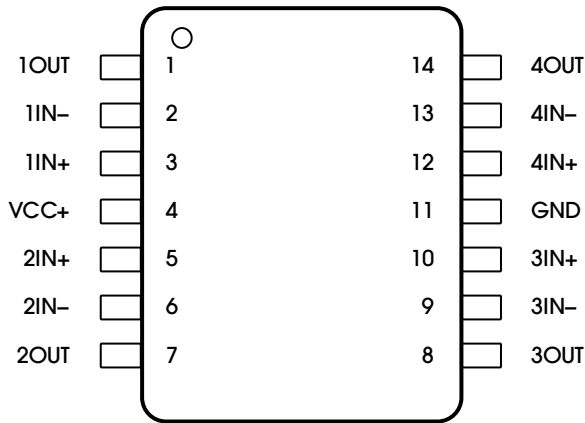


Figure 3. Pin Configuration (SOIC-14 and TSSOP-14 Packages)

Table 4 lists the pin functions of the SOIC-14 and TSSOP-14 packages.

Table 4. Pin Functions (SOIC-14 and TSSOP-14 Packages)

POSITION	NAME	TYPE	DESCRIPTION
1	1OUT	Output	Output
2	1IN-	Input	Inverting input
3	1IN+	Input	Noninverting input
4	VCC+	Power	Positive supply
5	2IN+	Input	Noninverting input
6	2IN-	Input	Inverting input
7	2OUT	Output	Output
8	3OUT	Output	Output
9	3IN-	Input	Inverting input
10	3IN+	Input	Noninverting input
11	GND	Power	Negative supply
12	4IN+	Input	Noninverting input
13	4IN-	Input	Inverting input
14	4OUT	Output	Output

5. SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Table 5 lists the absolute maximum ratings of the OPL321/OPL358/OPL324.

Table 5. Absolute Maximum Ratings

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
Voltage	Supply, $V_{CC}^{(2)}$		5.5	V
	Differential input voltage, $V_{ID}^{(3)}$		± 5.5	V
	Input voltage range (either input), V_I	-0.2	5.7	V
Duration of output short circuit (one amplifier) to ground, at or below $T_A = 25^\circ\text{C}$, $V_{CC} \leq 5.5\text{V}^{(4)}$		Unlimited		
Temperature	Operating, T_A	-40	125	$^\circ\text{C}$
	Junction, T_J		150	$^\circ\text{C}$
	Storage, T_{stg}	-65	150	$^\circ\text{C}$

Note 1: Stresses beyond those listed under Table 5 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 7. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 2: All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.

Note 3: Differential voltages are at $IN+$ with respect to $IN-$.

Note 4: Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

5.2 ESD RATINGS

Table 6 lists the ESD ratings of the OPL321/OPL358/OPL324.

Table 6. ESD Ratings

PARAMETER	SYMBOL	DESCRIPTION	VALUE	UNITS
Electrostatic Discharge	$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 3000	V
		Charged-device model (CDM), per JEDEC JS-002 ⁽²⁾	± 1000	

Note 1: The JEDEC document JEP155 indicates that 500V HBM allows safe manufacturing with a standard ESD control process.

Note 2: The JEDEC document JEP157 indicates that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 RECOMMENDED OPERATING CONDITIONS

Table 7 lists the recommended operating conditions for the OPL321/OPL358/OPL324.

Table 7. Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage (Single-Supply Operation)	V_{CC}	1.7		5.5	V
Operating Free-Air Temperature	T_A	-40		125	°C

5.4 THERMAL INFORMATION

Table 8 lists the thermal information for the OPL321/OPL358/OPL324.

Table 8. Thermal Information

PARAMETER	SYMBOL	SOIC-8	MSOP-8	SOIC-14	TSSOP-14	UNITS
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	123.8	175.2	108.0	127.3	°C/W
Junction-to-Board Thermal Resistance	$R_{\theta JB}$	74.9	124.0	68.7	94.3	°C/W
Junction-to-Top Characterization Parameter	ψ_{JT}	19.1	19.2	24.7	14.7	°C/W
Junction-to-Board Characterization Parameter	ψ_{JB}	73.6	117.9	67.3	88.7	°C/W
Junction-to-Case (Top) Thermal Resistance	$R_{\theta JC(top)}$	64.5	83.7	68	64.7	°C/W

5.5 ELECTRICAL CHARACTERISTICS

5.5.1 $V_{CC+} = 2.1V$

Table 9 lists the electrical characteristics of OPL321/OPL358/OPL324. $V_{CC+} = 2.1V$, $V_{CM} = V_{OUT} = 1/2 V_{CC+}$, $R_L = 2k\Omega$ to $1/2 V_{CC+}$. At $T_A = 25^\circ C$, unless otherwise noted.

Table 9. Electrical Characteristics ($V_{CC+} = 2.1V$)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$		± 0.5		mV
		$V_{CM} = 0V$, $T_A = -40^\circ C$ to $+125^\circ C$			4 ⁽¹⁾	mV
Average Temperature Coefficient of Input Offset Voltage	α_{VIO}			± 1.5		$\mu V/^\circ C$
Input Bias Current	I_{IB}			0.01		nA
Input Offset Current	I_{IO}			0.02		nA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0V$ to $1.4V$	64	90		dB
		$V_{CM} = 0V$ to $V_{CC+} + 0.05$	50	75		dB
Supply-Voltage Rejection Ratio	k_{SVR}	$V_{CC} = 1.7V$ to $5.5V$, $V_{CM} = 0V$	80	104		dB
Output Swing	V_O	$R_L = 10k\Omega$ to $1.35V$, high level	$V_{CC} - 20$	$V_{CC} - 6$		mV
		$R_L = 10k\Omega$ to $1.35V$, low level		5	20	mV
Supply Current	I_{CC}	OPL321		80	170	μA
		OPL321, $T_A = -40^\circ C$ to $+125^\circ C$			200	μA
		OPL358 (dual)		130	180	μA
		OPL358 (dual), $T_A = -40^\circ C$ to $+125^\circ C$			220 ⁽¹⁾	μA
		OPL324 (quad)		250	340	μA
		OPL324 (quad), $T_A = -40^\circ C$ to $+125^\circ C$			420 ⁽¹⁾	μA
Unity-Gain Bandwidth	B_1	$C_L = 200pF$		1.3		MHz
Phase Margin	Φ_m			60		deg
Gain Margin	G_m			10		dB
Open Loop Gain	A_{OL}	$R_L = 10k\Omega$, $V_{OUT} = 300mV$ to $V_{CC+} - 300mV$		5	30	$\mu V/V$
		$R_L = 2k\Omega$, $V_{OUT} = 300mV$ to $V_{CC+} - 300mV$		8	36	$\mu V/V$
Equivalent Input Noise Voltage	V_n	$f = 1kHz$		40		$nV/\sqrt{Hz}$

Note: Specified by characterization. Not production tested.

5.5.2 $V_{CC+} = 5V$

Table 10 lists the electrical characteristics of OPL321/OPL358/OPL324. $V_{CC+} = 5V$, $V_{CM} = V_{OUT} = 1/2 V_{CC+}$, $R_L = 2k\Omega$ to $1/2 V_{CC+}$. At $T_A = 25^\circ C$, unless otherwise noted.

Table 10. Electrical Characteristics ($V_{CC+} = 5V$)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$		± 0.5		mV
		$V_{CM} = 0V$, $T_A = -40^\circ C$ to $+125^\circ C$			4 ⁽¹⁾	mV
Average Temperature Coefficient of Input Offset Voltage	α_{VIO}	$T_A = 25^\circ C$		± 1.5		$\mu V/^\circ C$
Input Bias Current	I_{IB}	$T_A = 25^\circ C$		0.01		nA
Input Offset Current	I_{IO}	$T_A = 25^\circ C$		0.02		nA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0V$ to $3.6V$, $T_A = 25^\circ C$	77	105		dB
		$V_{CM} = 0V$ to $5.05V$, $T_A = 25^\circ C$	57	82		dB
Output Swing	V_O	High level, $T_A = 25^\circ C$	$V_{CC} - 50$	$V_{CC} - 30$		mV
		High level, $T_A = -40^\circ C$ to $+125^\circ C$	$V_{CC} - 50^{(1)}$			mV
		$T_A = 25^\circ C$, low level		25	40	mV
		$T_A = -40^\circ C$ to $+125^\circ C$, low level			50 ⁽¹⁾	mV
		$R_L = 10k\Omega$ to $2.5V$, high level, $T_A = 25^\circ C$	$V_{CC} - 20$	$V_{CC} - 6$		mV
		$R_L = 10k\Omega$ to $2.5V$, high level, $T_A = -40^\circ C$ to $+125^\circ C$	$V_{CC} - 20^{(1)}$			mV
		$R_L = 10k\Omega$ to $2.5V$, $T_A = 25^\circ C$, low level		5	20	mV
		$R_L = 10k\Omega$ to $2.5V$, $T_A = -40^\circ C$ to $+125^\circ C$, low level			20 ⁽¹⁾	mV
Output Short-Circuit Current	I_{OS}	Sourcing, $V_O = 0V$, $T_A = 25^\circ C$	50 ⁽¹⁾	56		mA
		Sinking, $V_O = 5V$, $T_A = 25^\circ C$	50 ⁽¹⁾	61		
Supply Current	I_{CC}	OPL321, $T_A = 25^\circ C$		130	250	μA
		OPL321, $T_A = -40^\circ C$ to $+125^\circ C$			350	μA
		OPL358 (dual), $T_A = 25^\circ C$		140	180	μA
		OPL358 (dual), $T_A = -40^\circ C$ to $+125^\circ C$			220 ⁽¹⁾	μA
		OPL324 (quad), $T_A = 25^\circ C$		260	360	μA
		OPL324 (quad), $T_A = -40^\circ C$ to $+125^\circ C$			445 ⁽¹⁾	μA
Unity-Gain Bandwidth	B_1	$C_L = 200pF$, $T_A = 25^\circ C$		1.3		MHz
Phase Margin	Φ_m	$T_A = 25^\circ C$		60		deg
Gain Margin	G_m	$T_A = 25^\circ C$		10		dB
Crosstalk		OPL358, OPL324		120		dB
Open Loop Gain	A_{OL}	$R_L = 10k\Omega$, $V_{OUT} = 300mV$ to $V_{CC+} - 300mV$		1	5.5	$\mu V/V$
		$R_L = 2k\Omega$, $V_{OUT} = 300mV$ to $V_{CC+} - 300mV$		2	6.7	$\mu V/V$
Equivalent Input Noise Voltage	V_n	$f = 1kHz$, $T_A = 25^\circ C$		40		$nV/\sqrt{Hz}$
Slew Rate	SR	$T_A = 25^\circ C$		0.7		$V/\mu s$

Note: Specified by characterization. Not production tested.

6. TYPICAL CHARACTERISTICS

$V_{CC+} = 5V$, $V_{CM} = V_{OUT} = 1/2 V_{CC+}$, $R_L = 2k\Omega$ to $1/2 V_{CC+}$. At $T_A = 25^\circ C$, unless otherwise noted.

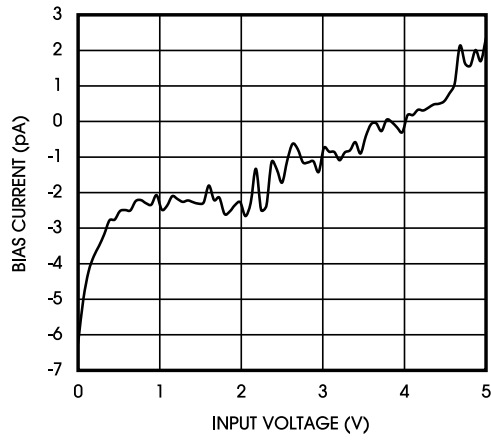


Figure 4. Input Bias Current vs. V_{CM}

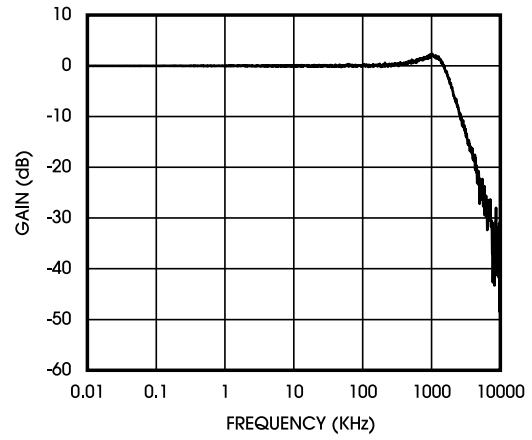


Figure 5. Bandwidth

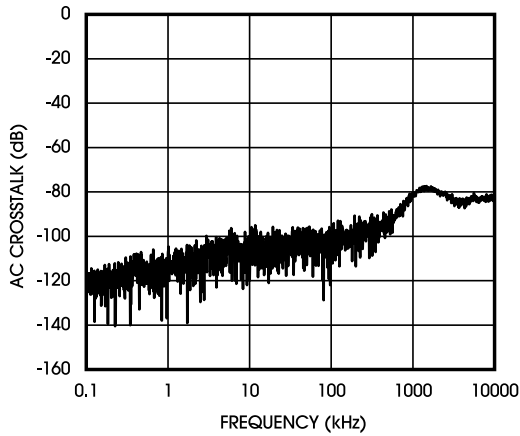


Figure 6. AC Crosstalk

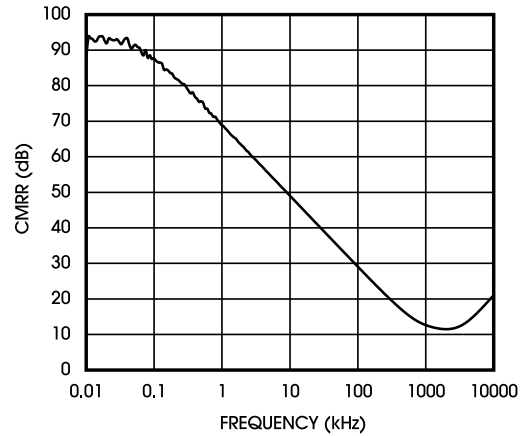


Figure 7. CMRR

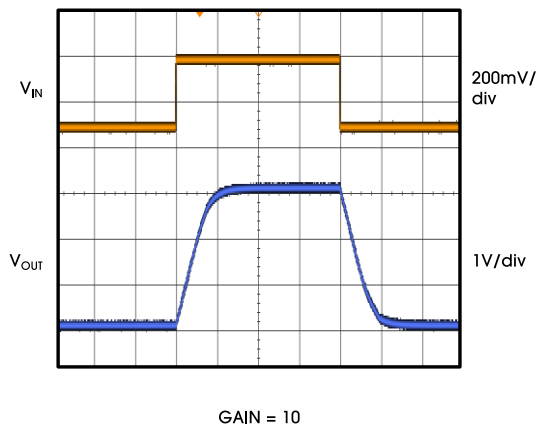


Figure 8. Step Response ($G = 10$)

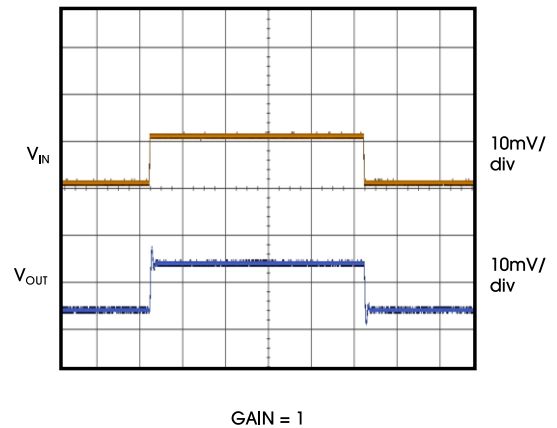


Figure 9. Step Response ($G = 1$)

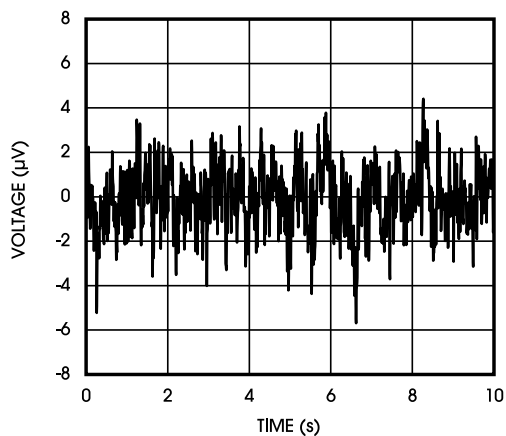


Figure 10. Integrated Noise

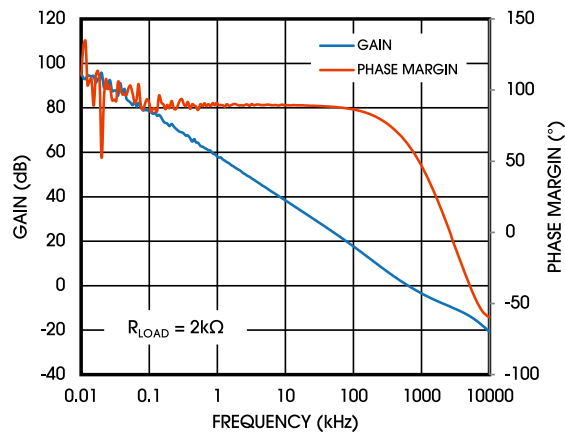


Figure 11. Phase Margin ($R_{LOAD} = 2k\Omega$)

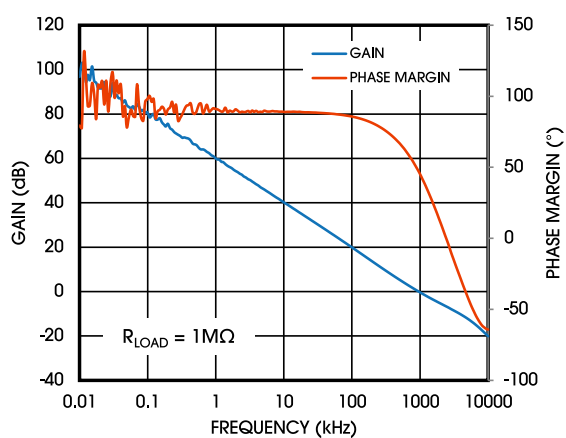


Figure 12. Phase Margin ($R_{LOAD} = 1M\Omega$)

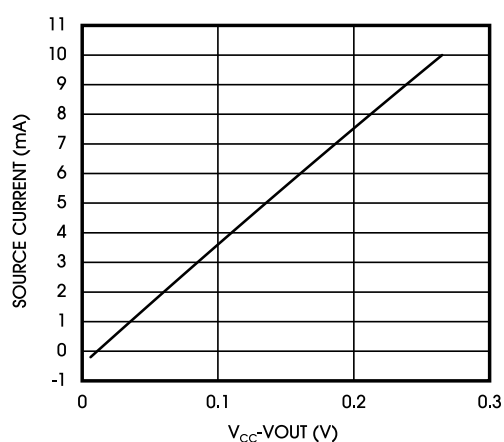


Figure 13. Output Source Current

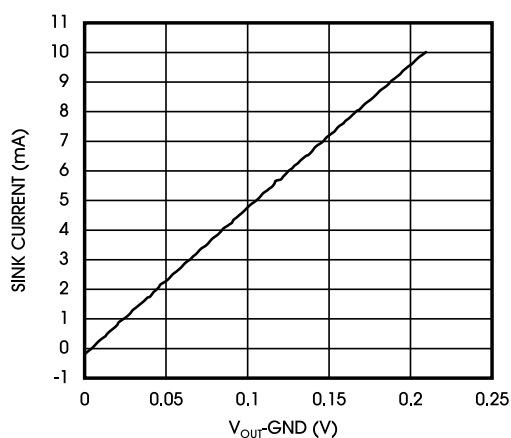


Figure 14. Output Sink Current

7. 详细说明

7.1 概述

OPL321、OPL358 和 OPL324 器件是具有轨至轨输出摆幅的单路、双路和四路低压(1.7V 至 5.5V)运算放大器。

OPL321、OPL358 和 OPL324 器件是最具成本效益的解决方案，适用于需要低电压运行、节省空间和低成本的应用。这些放大器专为低电压(1.7V 至 5V)操作而设计。

OPL321 器件采用超小型封装，该封装节省了印刷电路板上的空间，并支持小型便携式电子设备的设计。它还允许设计人员将设备放置在更靠近信号源的位置，以减少噪声拾取并提高信号完整性。

7.2 特性描述

7.2.1 工作电压

OPL321、OPL358 和 OPL324 器件经过完全规范并确保可从 1.7V 至 5V。此外，许多规格适用于 -40°C 至 125°C。

7.2.2 单位增益带宽

单位增益带宽是具有单位增益的放大器可以在不使信号严重失真的情况下工作的最高频率。OPL321、OPL358、OPL324 器件具有 1.3MHz 单位增益带宽。

7.2.3 转换速率

转换速率是当输入发生变化时运算放大器可以改变其输出的速率。OPL321、OPL358、OPL324 器件的转换速率为 0.7V/μs。

7.3 器件功能模式

连接电源后，OPL321、OPL358、OPL324 器件上电。根据应用，这些器件中的每一个都可以作为单电源运算放大器或双电源放大器运行。

8. 电源供电推荐

OPL321、OPL358、OPL324 器件指定工作电压范围为 1.7V 至 5V；许多规格适用于 -40°C 至 125°C。TYPICAL CHARACTERISTICS 部分提供的参数可能会因工作电压或温度而出现显著变化。

将 0.1μF 旁路电容器放置在电源引脚附近，以减少噪声或高阻抗电源耦合的误差。有关旁路电容器放置的更多详细信息，请参阅 LAYOUT 部分。

警告：电源电压大于 5.5V 可能会永久损坏器件(请参阅 ABSOLUTE MAXIMUM RATINGS)。

9. 布局

9.1 布局指南

为了使器件获得最佳运行性能，请采用良好的 PCB 布局实践，包括：

- 噪声可以通过整个电路的电源引脚以及运算放大器传播到模拟电路中。旁路电容器用于通过提供模拟电路本地的低阻抗电源来降低耦合噪声。

在每个电源引脚和接地之间连接低 ESR、0.1μF 陶瓷旁路电容器，并尽可能靠近器件放置。从 V+ 到地的单个旁路电容器适用于单电源应用。

- 电路的模拟和数字部分单独接地是最简单、最有效的噪声抑制方法之一。多层 PCB 上的一层或多层通常专用于接地层。接地层有助于散发热量并减少 EMI 噪声拾取。确保数字地和模拟地在物理上分开，注意地电流的流动。
- 为了减少寄生耦合，输入走线应尽可能远离电源或输出走线。如果无法将它们分开，最好垂直穿过敏感走线，而不是与噪声走线平行。
- 将外部组件尽可能靠近器件放置。将 RF 和 RG 保持靠近反相输入可最大限度地减少寄生电容。
- 保持输入走线的长度尽可能短。永远记住，输入走线是电路中最敏感的部分。
- 考虑在关键走线周围设置驱动的低阻抗保护环。保护环可以显著减少附近不同电位走线的漏电流。

9.2 布局示例

请参考 EVM 或者咨询公司销售支持。

10. PACKAGE INFORMATION

The OPL321/OPL358/OPL324 is available in the SOT23-5, SC70, SOIC-8, MSOP-8, TSSOP-8, SOIC-14, and TSSOP-14 packages.

10.1 SOIC-8 PACKAGE

Figure 15 shows the SOIC-8 package view.

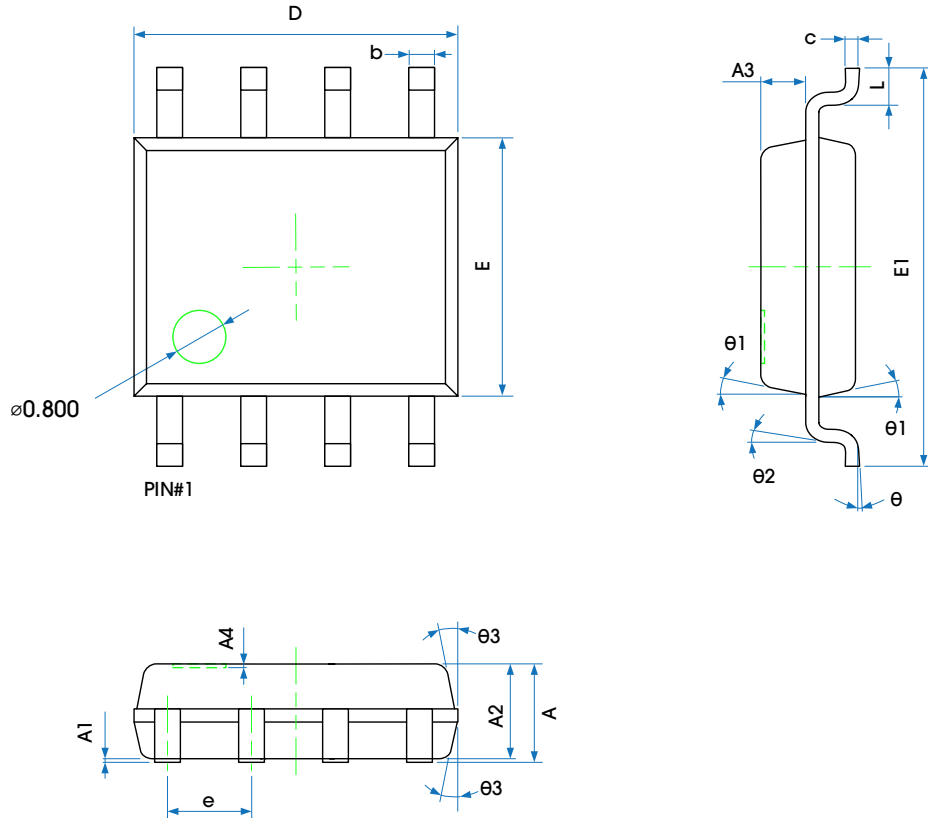


Figure 15. SOIC-8 Package View

Table 11 provides detailed information about the dimensions of the SOIC-8 package.

Table 11. Dimensions of the SOIC-8 Package

SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	1.300	1.500	1.700
A1	0.100	0.150	0.200
A2	1.350	1.420	1.550
A3	0.645	0.670	0.695
A4	0.020	—	0.050
b	0.330	0.400	0.510
c	0.170	0.203	0.250
D	4.800	4.900	5.000
E	3.800	3.900	4.000
E1	5.800	6.000	6.200
e	1.270BSC		
L	0.450	0.600	0.750
θ	0°	3°	8°
θ1	12° REF.		
θ2	5° REF.		
θ3	12° REF.		

10.2 MSOP-8 PACKAGE

Figure 16 shows the MSOP-8 package view.

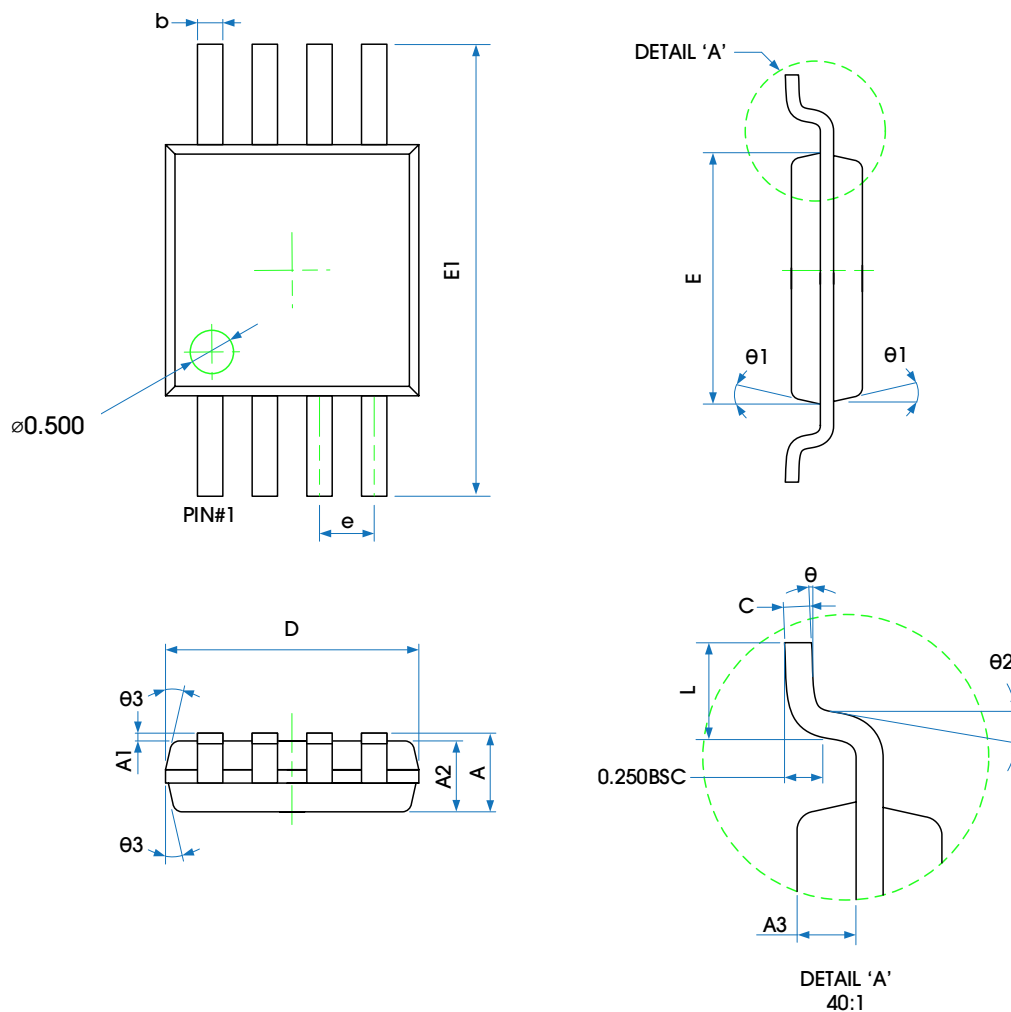


Figure 16. MSOP-8 Package View

Table 12 provides detailed information about the dimensions of the MSOP-8 package.

Table 12. Dimensions of the MSOP-8 Package

SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.820	0.930	1.100
A1	0.020	0.080	0.150
A2	0.750	0.850	0.950
A3	0.249	0.349	0.449
b	0.250	0.300	0.380
c	0.090	0.152	0.230
D	2.900	3.000	3.100
E	2.900	3.000	3.100
E1	4.750	4.900	5.050
e	0.650BSC		
L	0.400	0.600	0.800
θ	0°	3°	6°
θ1	12° REF.		
θ2	4° REF.		
θ3	12° REF.		

10.3 SOIC-14 PACKAGE

Figure 17 shows the SOIC-14 package view.

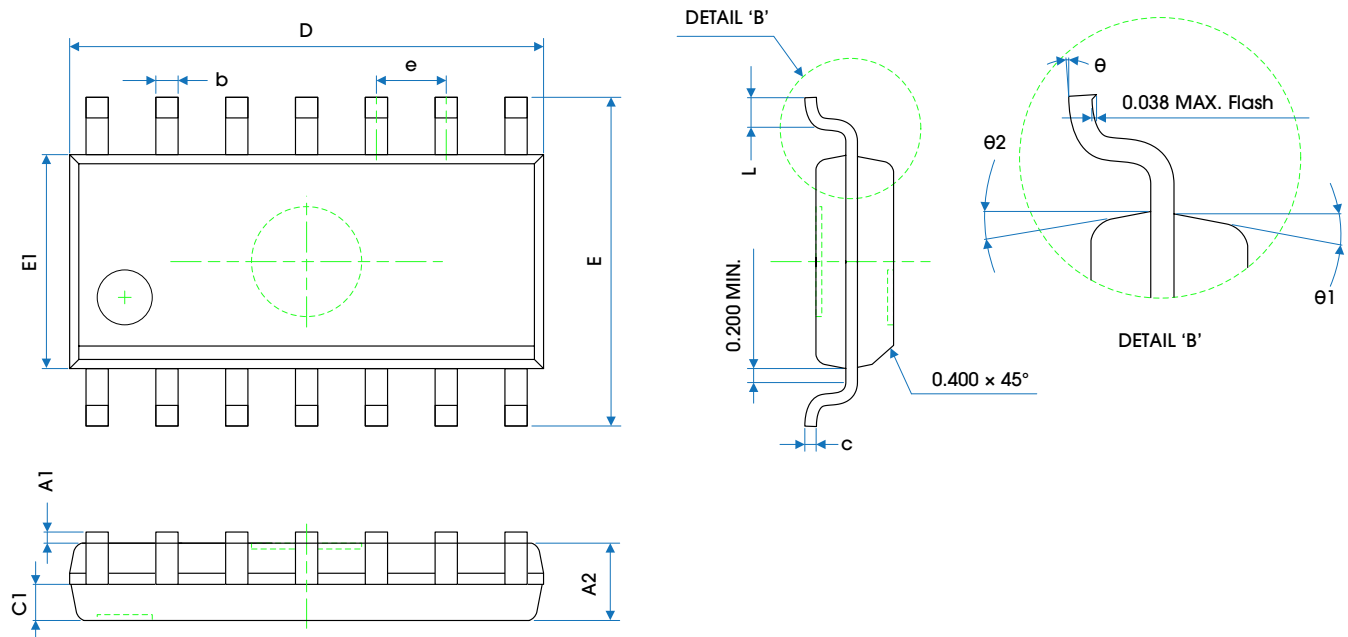


Figure 17. SOIC-14 Package View

Table 13 provides detailed information about the dimensions of the SOIC-14 package.

Table 13. Dimensions of the SOIC-14 Package

SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A1	0.050	0.200	0.250
A2	1.400	1.500	1.600
b	0.356	0.400	0.456
C1	0.600	0.670	0.700
c	0.193	0.203	0.213
D	8.550	8.650	8.750
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
e	1.270TYP.		
L	0.400	0.550	0.700
θ	0°	3°	8°
θ1	8°	11°	12°
θ2	8°	11°	12°

10.4 TSSOP-14 PACKAGE

Figure 18 shows the TSSOP-14 package view.

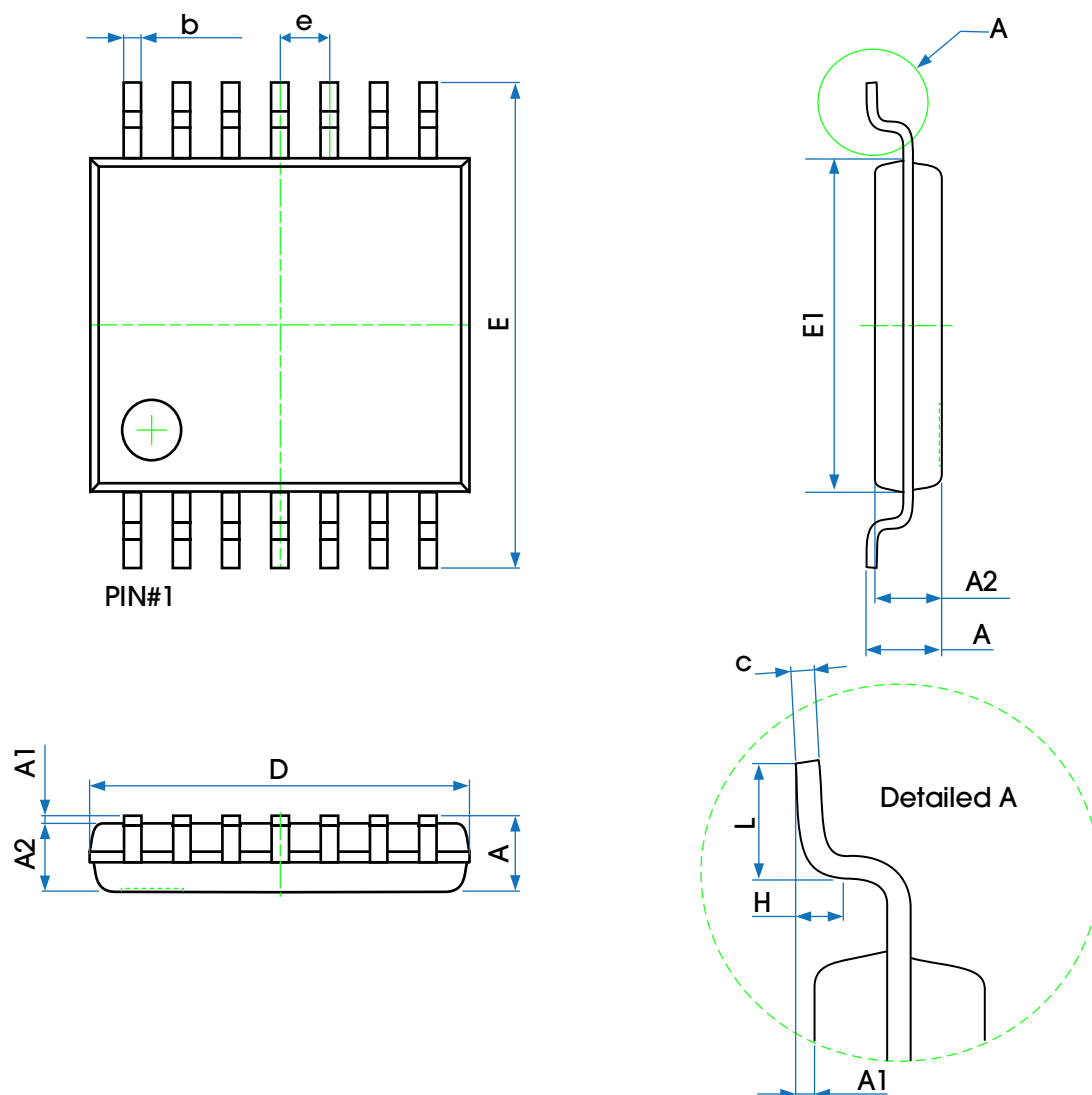


Figure 18. TSSOP-14 Package View

Table 14 provides detailed information about the dimensions of the TSSOP-14 package.

Table 14. Dimensions of the TSSOP-14 Package

SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	—	1.200	—	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.250	6.550	0.246	0.258
E1	4.300	4.500	0.169	0.177
e	0.650 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.250 (TYP)		0.010 (TYP)	
θ	1°	7°	1°	7°

11.1 SOIC-8 PACKAGE

The technical drawing illustrates the design of a sprocket cover tape. It includes three main views: a top view, a side view, and a detail view of the sprocket hole.

- Top View:** Shows a rectangular cover tape with a total width of 12.00 mm. It features a row of sprocket holes with a pitch of 8.0 ± 0.1 mm. The distance from the center of the first sprocket hole to the inner edge of the cover tape is 1.5^{+0.10}₋₀ mm. The distance from the center of the last sprocket hole to the inner edge is 1.5^{+0.25}₋₀ mm. The distance between the sprocket holes is 2 ± 0.05 mm. The distance from the sprocket hole to the sprocket is 4 ± 0.1 mm. The distance from the sprocket to the sprocket is 1.75 ± 0.1 mm. The distance from the sprocket to the sprocket is 5.5 ± 0.05 mm. The distance from the sprocket to the sprocket is 6.4 ± 0.1 mm. The distance from the sprocket to the sprocket is 12.0^{+0.30}_{-0.10} mm.
- Side View:** Shows the profile of the cover tape with a height of 2.10 ± 0.1 mm. The distance from the sprocket hole to the sprocket is 6.40 ± 0.10 mm.
- Detail View:** Shows a cross-section of the sprocket hole with a diameter of 5.40 ± 0.10 mm and a 5° chamfer.

Notes:

- Cover tape width: 9.3 ± 0.10.
- Cumulative tolerance of 10 sprocket hole pitch: ±0.20 (max).
- Camber: not to exceed 2mm in 250mm.
- Mold#: SOIC-8.
- All dimensions: mm.
- Direction of view:

Table 15 provides information about tape and reel.

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (mm)	CARTON SIZE (mm)
SOIC-8	13"	4000	1	8	32000	336*336*48	445*355*365

The diagram shows a pool table layout. At the top, four circles represent the 3-ball rack. Below them, two sets of pocket quadrants are shown. Each quadrant is a square divided into four smaller squares by dashed lines, labeled Q1 (top-left), Q2 (top-right), Q3 (bottom-left), and Q4 (bottom-right). A blue arrow points from the text 'Pin 1' to the Q1 quadrant of the left set.

Pin 1

Q1 Q2
Q3 Q4

Q1 Q2
Q3 Q4

* Q: Pocket quadrant

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11.2 MSOP-8 PACKAGE

Figure 21 illustrates the carrier tape.

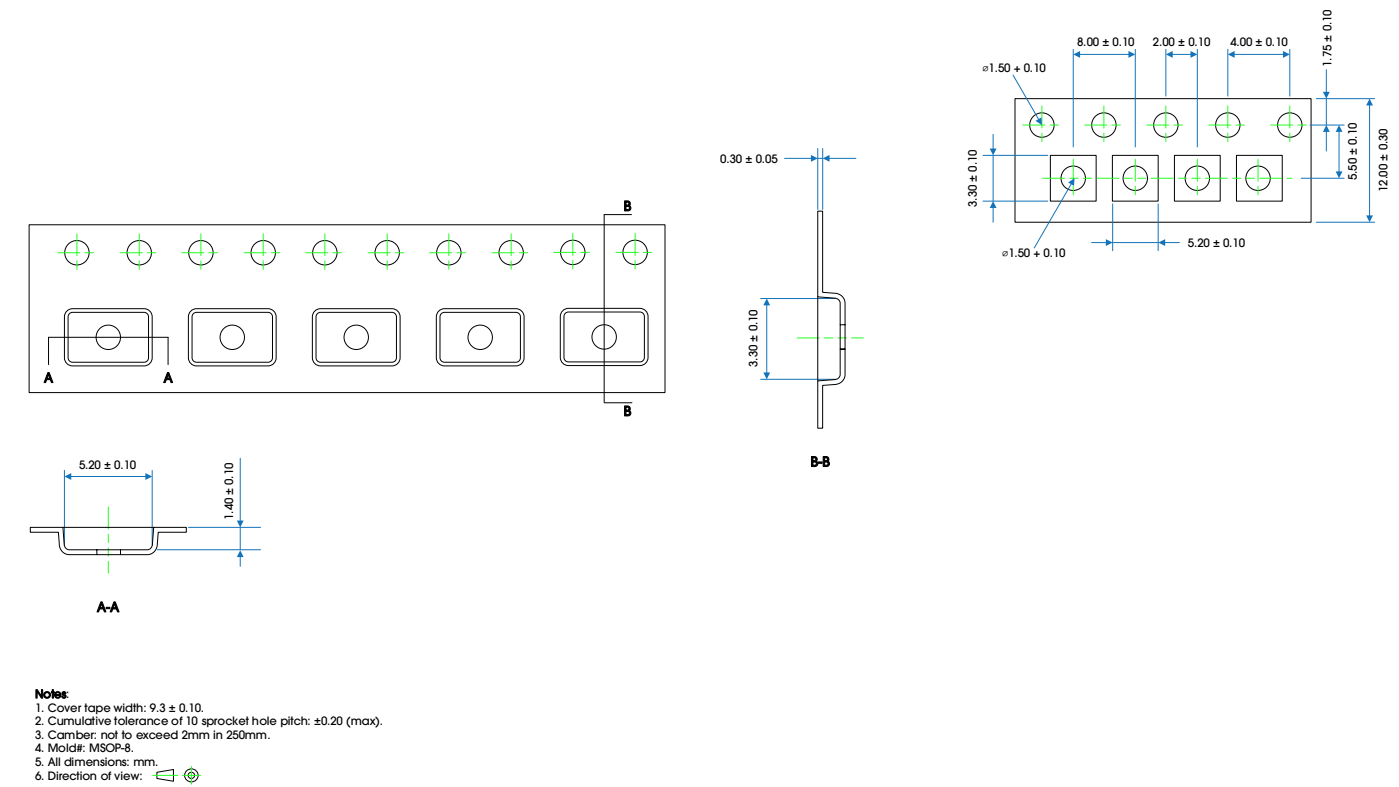


Figure 21. Carrier Tape Drawing

Table 16 provides information about tape and reel.

Table 16. Tape and Reel Information

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (mm)	CARTON SIZE (mm)
MSOP-8	13"	4000	1	8	32000	336*336*48	445*355*365

Figure 22 shows the product loading orientation—pin 1 is assigned at Q1.

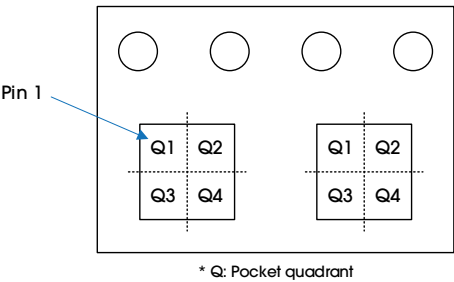
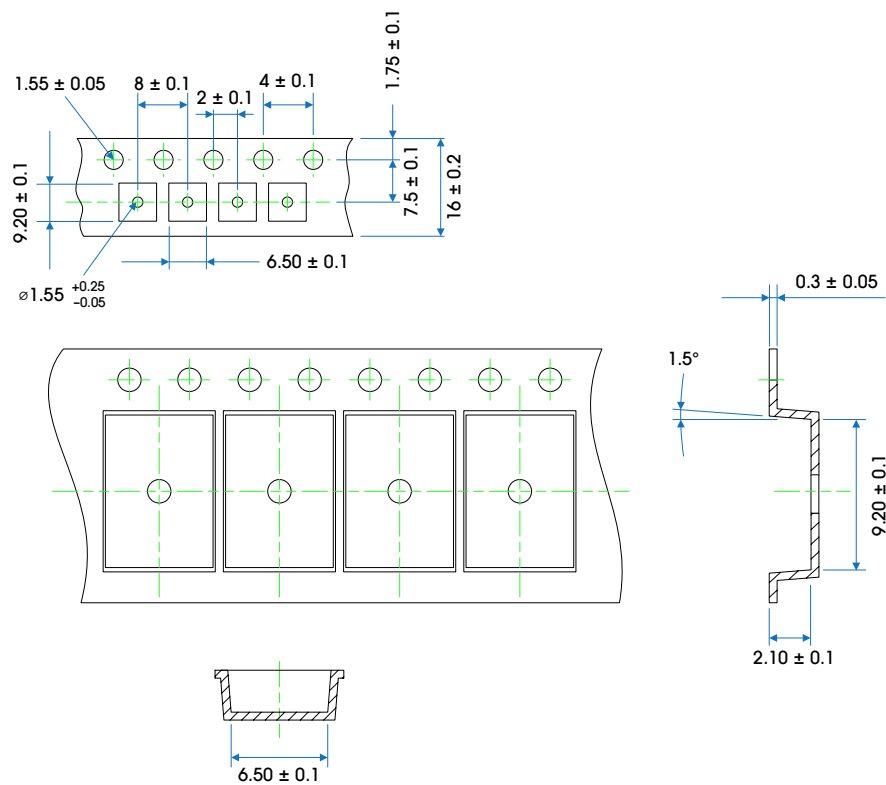


Figure 22. Product Loading Orientation

11.3 SOIC-14 PACKAGE

Figure 23 illustrates the carrier tape.



- Notes:**
- 1. Cover tape width: 13.5 ± 0.10.
 - 2. Cumulative tolerance of 10 sprocket hole pitch: ±0.20 (max).
 - 3. Camber: not to exceed 2mm in 250mm.
 - 4. Mold#: SOIC-14.
 - 5. All dimensions: mm.
 - 6. Direction of view:

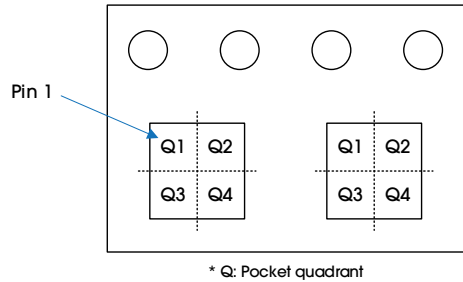
Figure 23. Carrier Tape Drawing

Table 17 provides information about tape and reel.

Table 17. Tape and Reel Information

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (mm)	CARTON SIZE (mm)
SOIC-14	13"	2500	1	8	20000	336*336*48	445*355*365

Figure 22 shows the product loading orientation—pin 1 is assigned at Q1.



* Q: Pocket quadrant

Figure 24. Product Loading Orientation

11.4 TSSOP-14 PACKAGE

Figure 25 illustrates the carrier tape.

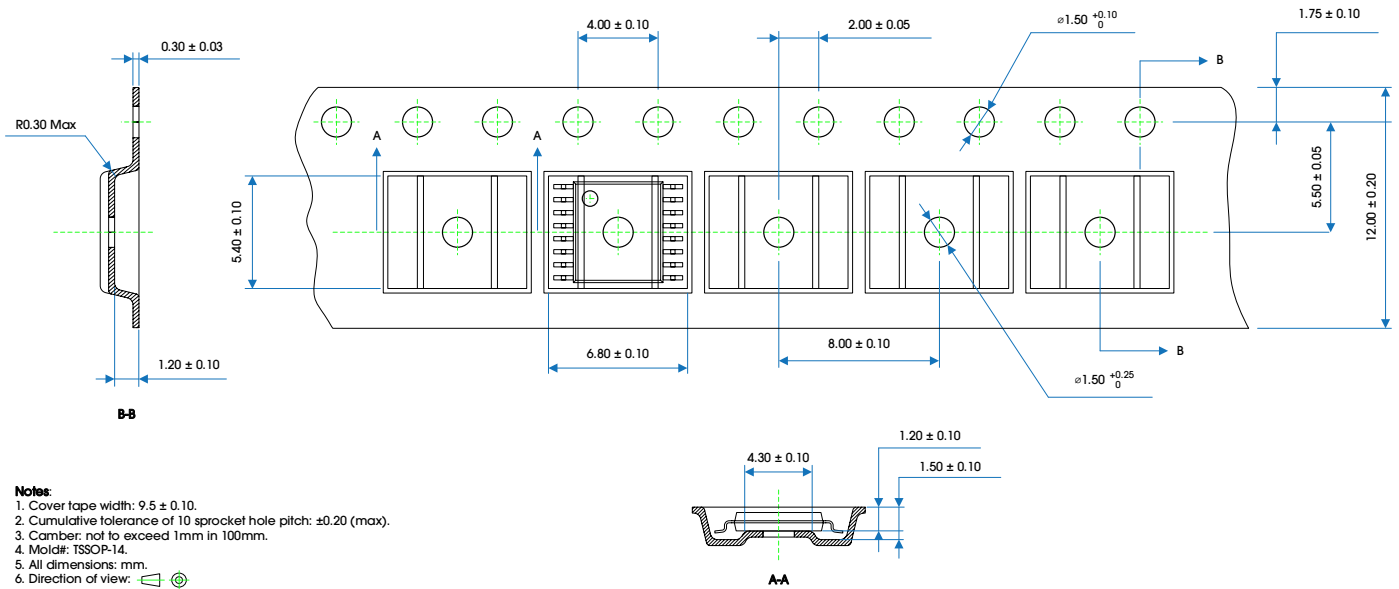


Figure 25. Carrier Tape Drawing

Table 18 provides information about tape and reel.

Table 18. Tape and Reel Information

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (mm)	CARTON SIZE (mm)
TSSOP-14	13"	4000	1	8	32000	358*340*50	430*380*390

Figure 26 shows the product loading orientation—pin 1 is assigned at Q1.

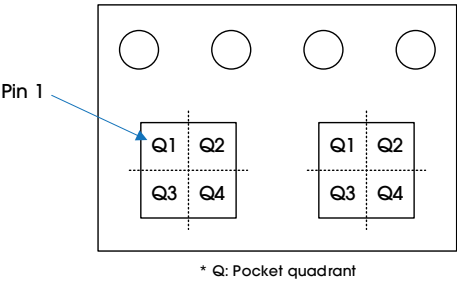


Figure 26. Product Loading Orientation

REVISION HISTORY

REVISION	DATE	DESCRIPTION
Rev A	05 August 2024	Rev A release.