

芯伯乐®
X I N B O L E

Product Specification

XBLW CD4013

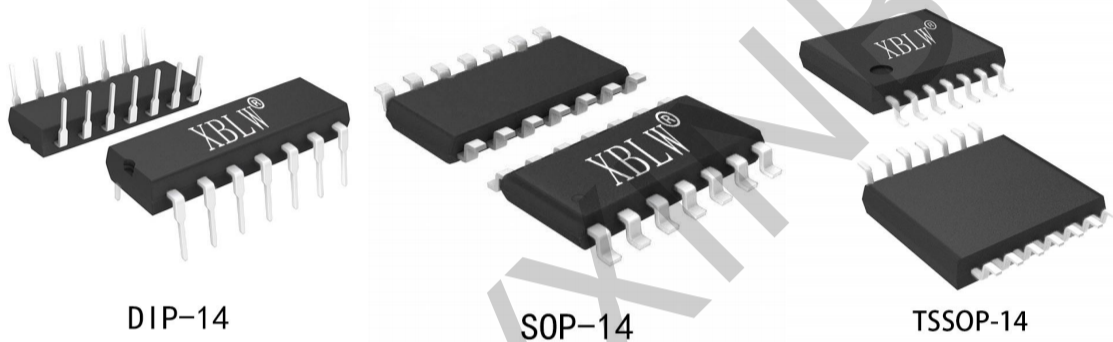
Dual D-Type Flip Flop

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Description

The CD4013 is a dual D-type flip-flop that features independent set-direct input (SD), clear-direct input (CD), clock input (CP) and outputs (Q, \bar{Q}). Data is accepted when CP is LOW and is transferred to the output on the positive -going edge of the clock. The active HIGH asynchronous CD and SD inputs are independent and override the D or CP inputs. The outputs are buffered for best system performance. The clock input's Schmitt-trigger action makes the circuit highly tolerant of slower clock rise and fall times. It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.



Feature

- Wide supply voltage range from 3V to 15V
- Fully static operation
- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Tolerant of slow clock rise and fall times
- Specified from -40°C to +85°C
- Packaging information: DIP14/SOP14/TSSOP14

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW CD4013BE	DIP-14	CD4013BE	Tube	1000Pcs/Box
XBLW CD4013BDTR	SOP-14	CD4013B	Tape	2500Pcs/Reel
XBLW CD4013BDTR	TSSOP-14	CD4013B	Tape	3000Pcs/Reel

Block Diagram And Pin Description

Block Diagram

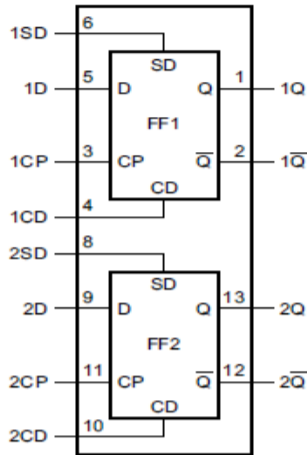


Figure 1. Functional diagram

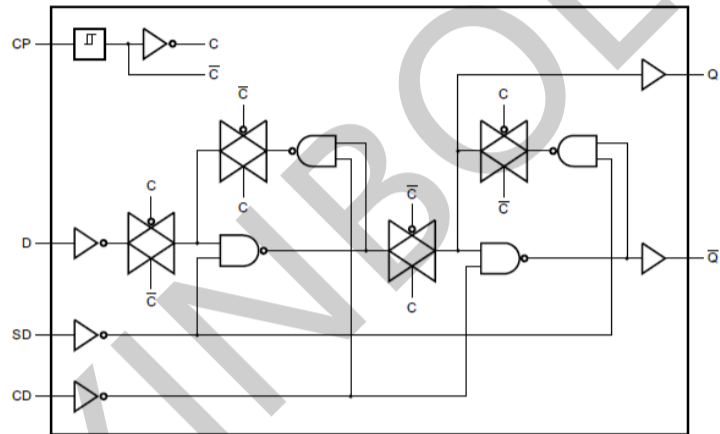
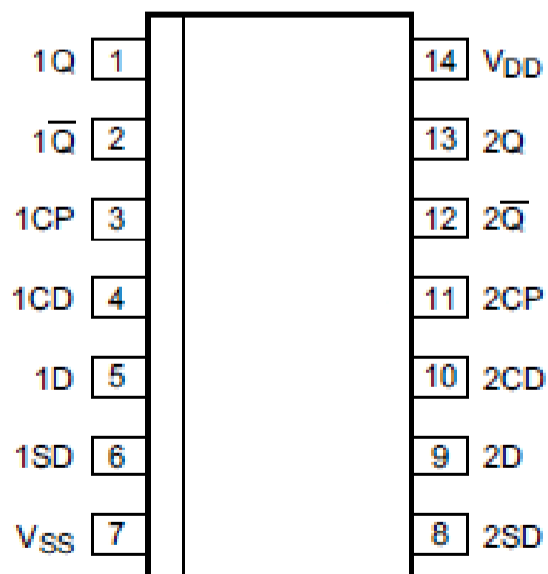


Figure 2. Logic diagram(one flip-flop)

Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	1Q	true output
2	1 \bar{Q}	complement output
3	1CP	clock input (LOW to HIGH edge-triggered)
4	1CD	asynchronous clear-direct input (active HIGH)
5	1D	data input
6	1SD	asynchronous set-direct input(active HIGH)
7	V _{SS}	ground (0V)
8	2SD	asynchronous set-direct input(active HIGH)
9	2D	data input
10	2CD	asynchronous clear-direct input (active HIGH)
11	2CP	clock input (LOW to HIGH edge-triggered)
12	2 \bar{Q}	complement output
13	2Q	true output
14	V _{DD}	supply voltage

Function Table

Input				Output	
nSD	nCD	nCP	nD	nQ	nQ
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H	H
L	L	↑	L	L	H
L	L	↑	H	H	L

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care; ↑=LOW-to-HIGH clock transition.

Electrical Parameter

Absolute Maximum Ratings (Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V _{DD}	-	-0.5	+18	V
DC input current	I _{IK}	any one input	-	±10	mA
input voltage	V _I	all inputs	-0.5	V _{DD} +0.5	V
storage temperature	T _{stg}	-	-65	+150	°C
total power dissipation	P _{tot}	-	-	500	mW
device dissipation	P	per output transistor	-	100	mW
Soldering temperature	T _L	10s	DIP	245	°C
			SOP	250	°C

Note:

[1] For DIP14 packages: above 70°C the value of P_{tot} derates linearly with 12mW/K.

[2] For SOP14 packages: above 70°C the value of P_{tot} derates linearly with 8mW/K.

[3] For (T)SSOP14 packages: above 60°C the value of P_{tot} derates linearly with 5.5mW/K.

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	-	15	V
ambient temperature	T_{amb}	in free air	-40	-	+85	°C
set-up time	t_{SU}	$V_{DD}=5V$	40	-	-	ns
		$V_{DD}=10V$	20	-	-	ns
		$V_{DD}=15V$	15	-	-	ns
clock pulse width	t_{wCL}	$V_{DD}=5V$	140	-	-	ns
		$V_{DD}=10V$	60	-	-	ns
		$V_{DD}=15V$	40	-	-	ns
clock input frequency	f_{CL}	$V_{DD}=5V$	3.5	7	-	MHz
		$V_{DD}=10V$	8	16	-	MHz
		$V_{DD}=15V$	12	24	-	MHz
clock rise and fall time	t_{rCL}, t_{fCL}	$V_{DD}=5V$	-	-	15	uS
		$V_{DD}=10V$	-	-	10	us
		$V_{DD}=15V$	-	-	5	uS
Set or reset pulse width	$t_{wS/R}$	$V_{DD}=5V$	180	-	-	ns
		$V_{DD}=10V$	80	-	-	ns
		$V_{DD}=15V$	50	-	-	ns

Note: If more than one unit is cascaded in a parallel clocked operation, t_{rCL} must be made less than or equal to the sum of the fixed propagation delay time at 15pF and the transition time of the output driving stage for the estimated capacitive load.

Electrical Characteristics

DC Characteristics 1 (Tamb=25°C, voltages are referenced to Vss (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions(V)			Tamb=25°C			Unit
		VO	VIN	VDD	Min.	Typ.	Max.	
supply current	IDD	-	0, 5	5	-	0.02	1	μA
		-	0, 10	10	-	0.02	2	μA
		-	0, 15	15	-	0.02	4	μA
LOW-level output current	IOL	0.4	0, 5	5	0.51	1	-	mA
		0.5	0, 10	10	1.3	2.6	-	mA
		1.5	0, 15	15	3.4	6.8	-	mA
HIGH-level output current	IOH	4.6	0, 5	5	-0.51	-1	-	mA
		2.5	0, 5	5	-1.6	-3.2	-	mA
		9.5	0, 10	10	-1.3	-2.6	-	mA
		13.5	0, 15	15	-3.4	-6.8	-	mA
LOW-level output voltage	VOL	-	0, 5	5	-	0	0.05	V
		-	0, 10	10	-	0	0.05	V
		-	0, 15	15	-	0	0.05	V
HIGH-level output voltage	VOH	-	0, 5	5	4.95	5	-	V
		-	0, 10	10	9.95	10	-	V
		-	0, 15	15	14.95	15	-	V
LOW-level input voltage	VIL	0.5, 4.5	-	5	-	-	1.5	V
		1, 9	-	10	-	-	3	V
		1.5, 13.5	-	15	-	-	4	V
HIGH-level input voltage	VIH	0.5, 4.5	-	5	3.5	-	-	V
		1, 9	-	10	7	-	-	V
		1.5, 13.5	-	15	11	-	-	V
input leakage current	II	-	0, 15	15	-	-	±1	μA

DC Characteristics 2

(Tamb=-40°C to +85°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions(V)			Tamb=-40°C		Tamb=+85°C		Unit
		VO	VIN	VDD	Min.	Max.	Min.	Max.	
supply current	IDD	-	0, 5	5	-	1	-	30	μA
		-	0, 10	10	-	2	-	60	μA
		-	0, 15	15	-	4	-	120	μA
LOW-level output current	IOL	0.4	0, 5	5	0.61	-	0.42	-	mA
		0.5	0, 10	10	1.5	-	1.1	-	mA
		1.5	0, 15	15	4	-	2.8	-	mA
HIGH-level output current	IOH	4.6	0, 5	5	-0.61	-	-0.42	-	mA
		2.5	0, 5	5	-1.8	-	-1.3	-	mA
		9.5	0, 10	10	-1.5	-	-1.1	-	mA
		13.5	0, 15	15	-4	-	-2.8	-	mA
LOW-level output voltage	VOL	-	0, 5	5	-	0.05	-	0.05	V
		-	0, 10	10	-	0.05	-	0.05	V
		-	0, 15	15	-	0.05	-	0.05	V
HIGH-level output voltage	VOH	-	0, 5	5	4.95	-	4.95	-	V
		-	0, 10	10	9.95	-	9.95	-	V
		-	0, 15	15	14.95	-	14.95	-	V
LOW-level input voltage	VIL	0.5, 4.5	-	5	-	1.5	-	1.5	V
		1, 9	-	10	-	3	-	3	V
		1.5, 13.5	-	15	-	4	-	4	V
HIGH-level input voltage	VIH	0.5, 4.5	-	5	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	V
		1.5, 13.5	-	15	11	-	11	-	V
input leakage current	II	-	0, 15	15	-	±1	-	±1	μA

AC Characteristics ($T_{amb}=25^{\circ}\text{C}$, $V_{SS}=0\text{V}$, $t_r, t_f=20\text{ns}$, $C_L=50\text{pF}$, $R_L=20\text{K}\Omega$, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
HIGH to LOW propagation delay	t_{PHL}	nCP to nQ, n \bar{Q} ; see Figure 4	$V_{DD}=5\text{V}$	-	150	300	ns
			$V_{DD}=10\text{V}$	-	65	130	ns
			$V_{DD}=15\text{V}$	-	45	90	ns
		nSD to n \bar{Q} or nCD to nQ	$V_{DD}=5\text{V}$	-	200	400	ns
			$V_{DD}=10\text{V}$	-	85	170	ns
			$V_{DD}=15\text{V}$	-	60	120	ns
LOW to HIGH propagation delay	t_{PLH}	nCP to nQ, n \bar{Q} ; see Figure 4	$V_{DD}=5\text{V}$	-	150	300	ns
			$V_{DD}=10\text{V}$	-	65	130	ns
			$V_{DD}=15\text{V}$	-	45	90	ns
		nSD to nQ or nCD to n \bar{Q}	$V_{DD}=5\text{V}$	-	150	300	ns
			$V_{DD}=10\text{V}$	-	65	130	ns
			$V_{DD}=15\text{V}$	-	45	90	ns
transition time	t_t	see Figure 4	$V_{DD}=5\text{V}$	-	100	200	ns
			$V_{DD}=10\text{V}$	-	50	100	ns
			$V_{DD}=15\text{V}$	-	40	80	ns
maximum clock frequency	$f_{clk(max)}$	see Figure 4	$V_{DD}=5\text{V}$	3.5	7	-	MHz
			$V_{DD}=10\text{V}$	8	16	-	MHz
			$V_{DD}=15\text{V}$	12	24	-	MHz
pulse width	t_w	nCP input LOW; see Figure 4	$V_{DD}=5\text{V}$	-	70	140	ns
			$V_{DD}=10\text{V}$	-	30	60	ns
			$V_{DD}=15\text{V}$	-	20	40	ns
		nSD input HIGH or nCD input HIGH; see Figure 5	$V_{DD}=5\text{V}$	-	90	180	ns
			$V_{DD}=10\text{V}$	-	40	80	ns
			$V_{DD}=15\text{V}$	-	25	50	ns
set-up time	t_{SU}	nD to nCP; see Figure 4	$V_{DD}=5\text{V}$	-	20	40	ns
			$V_{DD}=10\text{V}$	-	10	20	ns
			$V_{DD}=15\text{V}$	-	7	15	ns
hold time	t_h	nD to nCP; see Figure 4	$V_{DD}=5\text{V}$	-	2	5	ns
			$V_{DD}=10\text{V}$	-	2	5	ns
			$V_{DD}=15\text{V}$	-	2	5	ns
clock input rise or fall time	t_{rCL}, t_{fCL}	-	$V_{DD}=5\text{V}$	-	-	15	us
			$V_{DD}=10\text{V}$	-	-	10	us
			$V_{DD}=15\text{V}$	-	-	5	us
input capacitance	C_I	any input	-	5	7.5	pF	

 Note: t_t is the same as t_{LH} and t_{HL} .

Testing Circuit

AC Testing Circuit

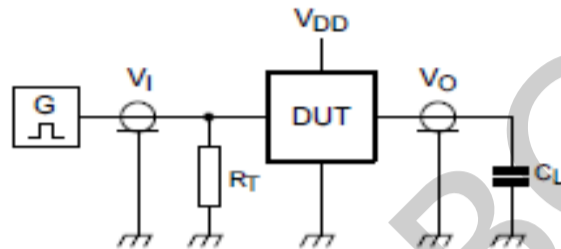


Figure 3. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

AC Testing Waveforms

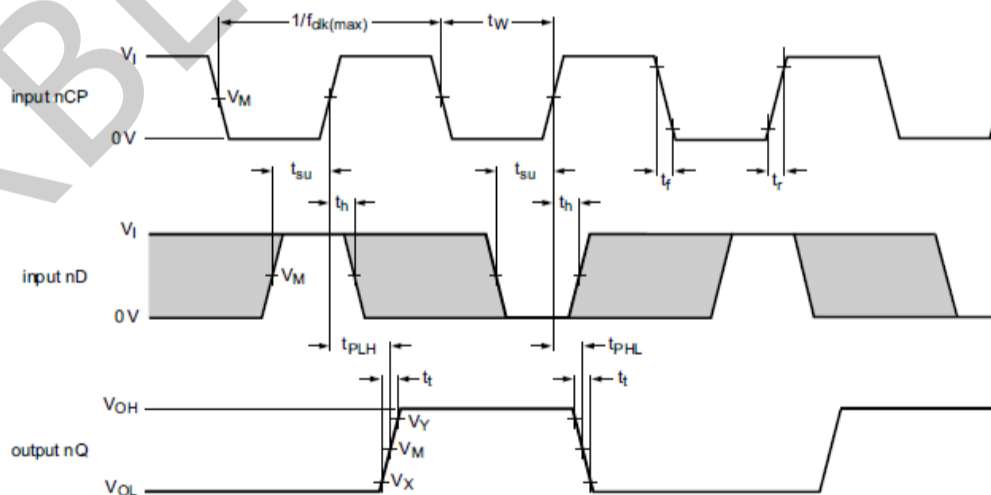


Figure 4. Set-up time, hold time, minimum clock pulse width, propagation delays and transition times

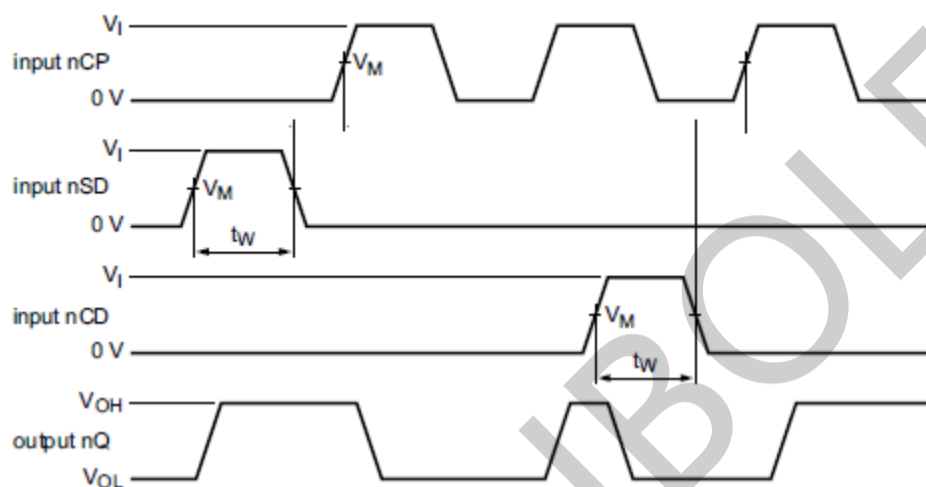


Figure 5. nSD, nCD pulse width

Measurement Points

Supply voltage	Input	Output		
V_{DD}	V_M	V_M	V_X	V_Y
5V to 15V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$	$0.1 \times V_{DD}$	$0.9 \times V_{DD}$

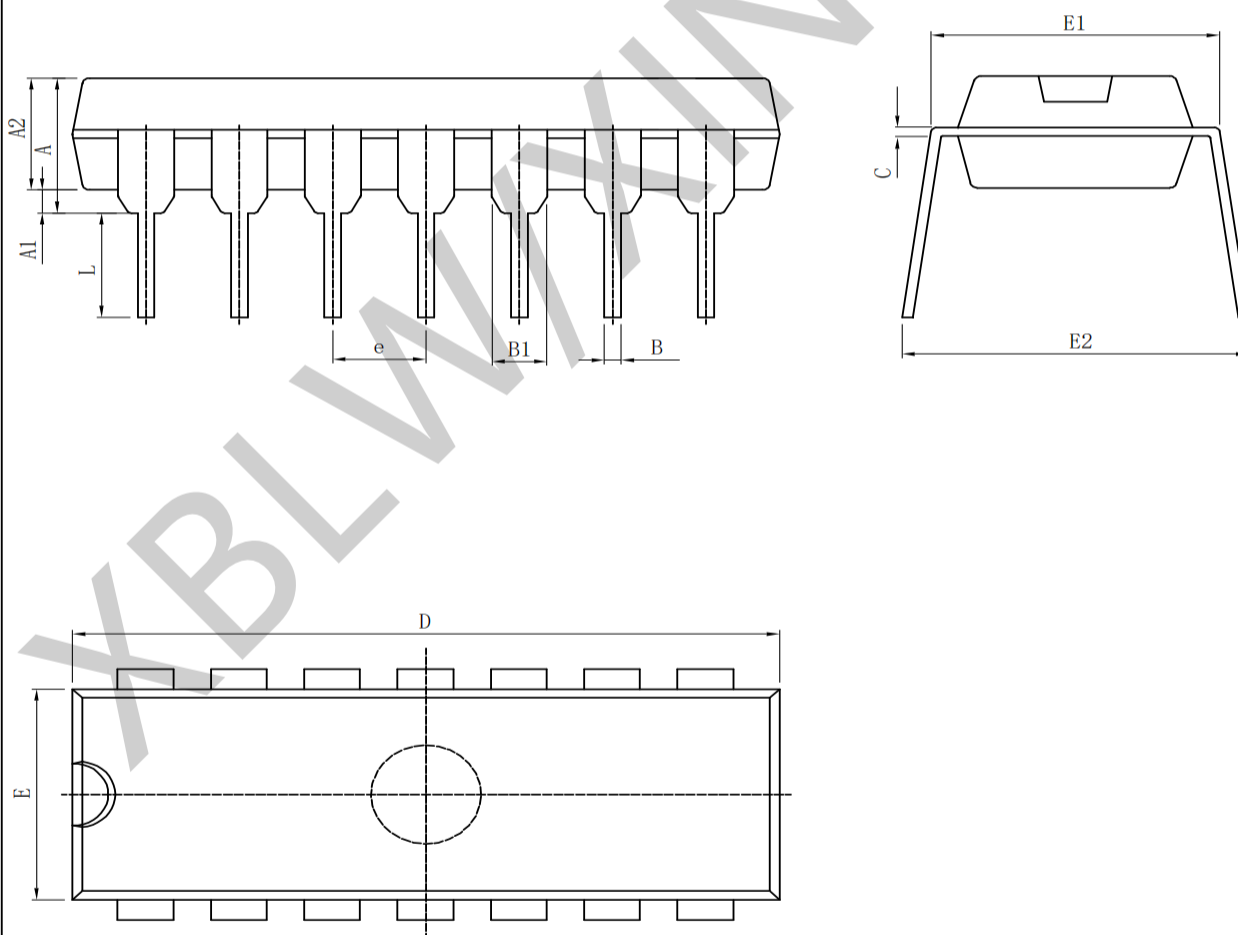
Test Data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5V to 15V	V_{SS} or V_{DD}	$\leq 20\text{ns}$	50pF

Package Information

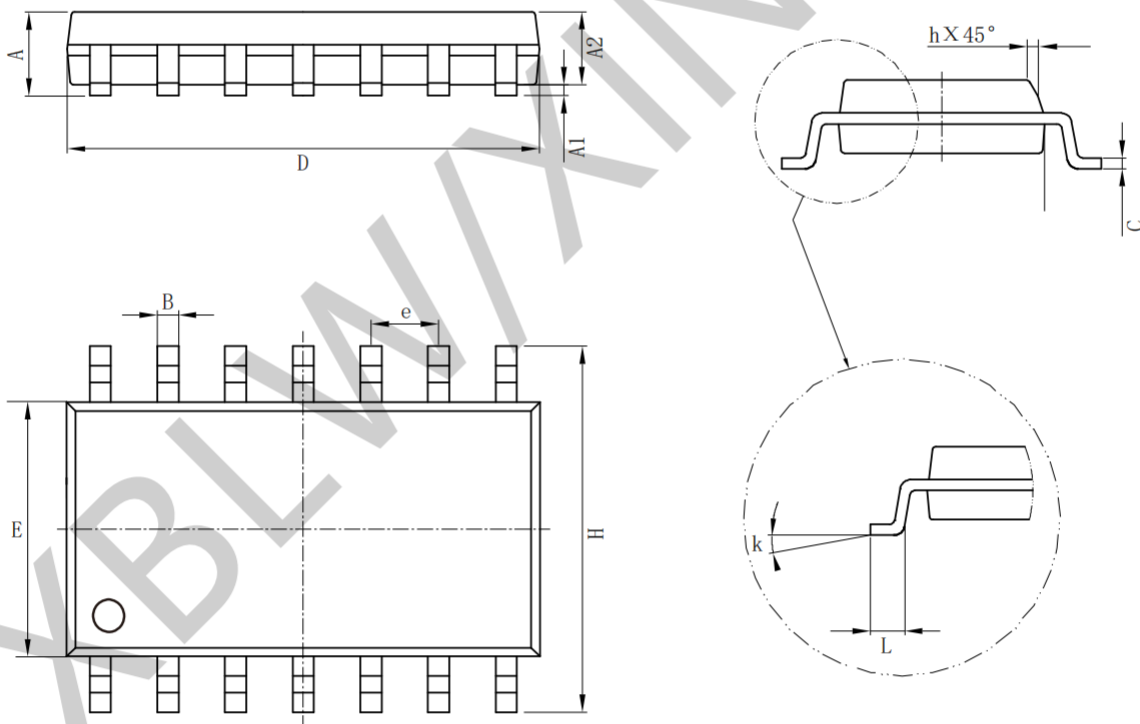
· DIP-14

Symbol	Size	Dimensions In Millimeters		Symbol	Size	Dimensions In Inches	
		Min (mm)	Max (mm)			Min (in)	Max (in)
A		3.710	4.310	A		0.146	0.170
A1		0.510		A1		0.020	
A2		3.200	3.600	A2		0.126	0.142
B		0.380	0.570	B		0.015	0.022
B1		1.524 (BSC)		B1		0.060 (BSC)	
C		0.204	0.360	C		0.008	0.014
D		18.800	19.200	D		0.740	0.756
E		6.200	6.600	E		0.244	0.260
E1		7.320	7.920	E1		0.288	0.312
e		2.540 (BSC)		e		0.100 (BSC)	
L		3.000	3.600	L		0.118	0.142
E2		8.400	9.000	E2		0.331	0.354



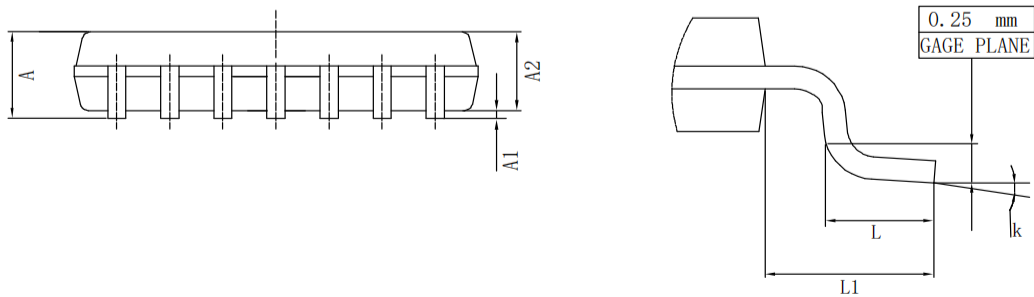
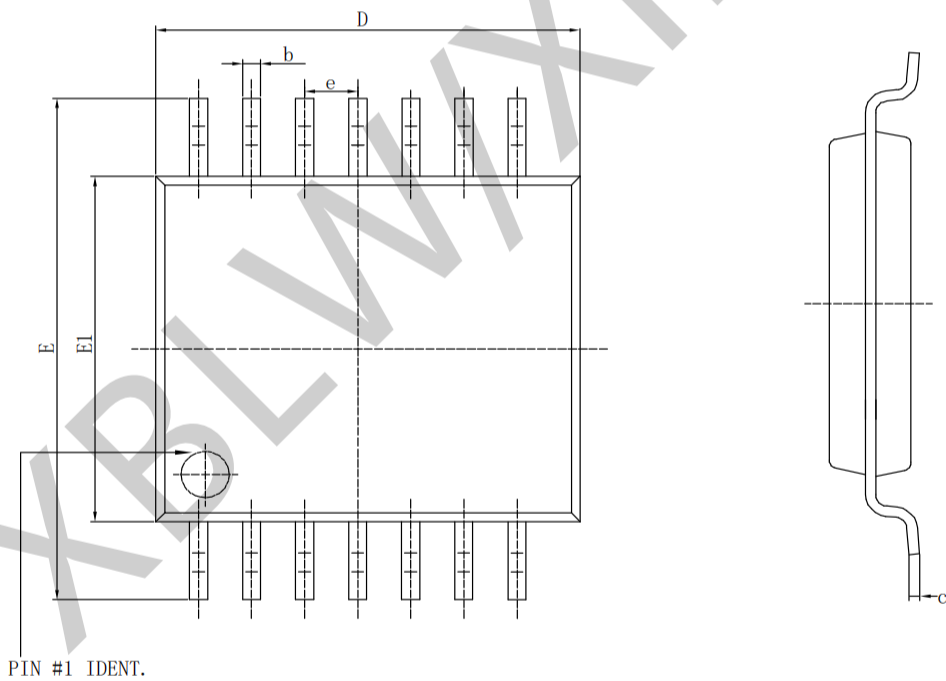
· SOP-14

Size Symbol	Dimensions In Millimeters		Size Symbol	Dimensions In Inches	
	Min (mm)	Max (mm)		Min (in)	Max (in)
A	1.350	1.750	A	0.050	0.068
A1	0.100	0.250	A1	0.004	0.009
A2	1.100	1.650	A2	0.040	0.060
B	0.330	0.510	B	0.010	0.020
C	0.190	0.250	C	0.007	0.009
D	8.550	8.750	D	0.330	0.340
E	3.800	4.000	E	0.150	0.150
e	1.27		e	0.05	
H	5.800	6.200	H	0.220	0.240
h	0.250	0.500	h	0.009	0.020
L	0.400	1.270	L	0.015	0.050
k	8° (max)		k	8° (max)	



· TSSOP-14

Size Symbol	Dimensions In Millimeters		Size Symbol	Dimensions In Inches	
	Min (mm)	Max (mm)		Min (in)	Max (in)
A		1.200	A		0.047
A1	0.050	0.150	A1	0.002	0.006
A2	0.800	1.050	A2	0.031	0.041
b	0.190	0.300	b	0.007	0.012
c	0.090	0.200	c	0.004	0.0089
D	4.900	5.100	D	0.193	0.201
E	6.200	6.600	E	0.244	0.260
E1	4.300	4.500	E1	0.169	0.176
e	0.65		e	0.0256	
L	0.450	0.750	L	0.018	0.030
L1	1.00		L1	0.039	
k	0°	8°	k	0°	8°



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