

1、 General Description

CS5755MT is a highly integrated and reliable 3-phase brushless DC motor driver circuit as a solution for low power motor driver, such as fan motors. It includes 6 fast-recovery MOSFETs, and 3 half-bridge HVICs for gate driving. The circuit which has under-voltage protection integrated can provide excellent protection and fail safe operation. Due to the each phase has an independent negative DC-link terminal, the current can be detected separately. CS5755MT provides a temperature sensing output port. In addition, an internal bootstrap diode is integrated to simplify the peripheral circuit.

Features

- 6 fast-recovery MOSFETs are built in
- HVIC for gate driving is built in
- Under-voltage protection is built in
- Bootstrap diodes are built in
- Fully compatible with 3.3V/5V/15V MCU interfaces, active high
- Temperature sensing function
- 3 divided negative DC-link terminals for inverter current sensing applications
- Optimized for low electromagnetic interference
- Isolation voltage rating of 1500Vrms for 1min
- Package: CS5755MTP: DIP-23H

CS5755MTO: SOP-23H

2、 Function Diagram and Pin Description

2. 1、 Function Diagram

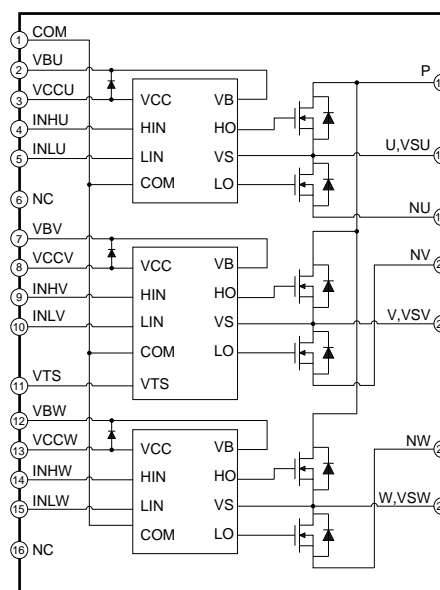


Figure1. Function Diagram

2. 2、 Function Description

This circuit is composed of 6 fast-recovery MOSFETs and 3 half-bridge HVICs for gate driving, as shown above. The block diagram and description of each half-bridge HVIC for gate driving are as follows.

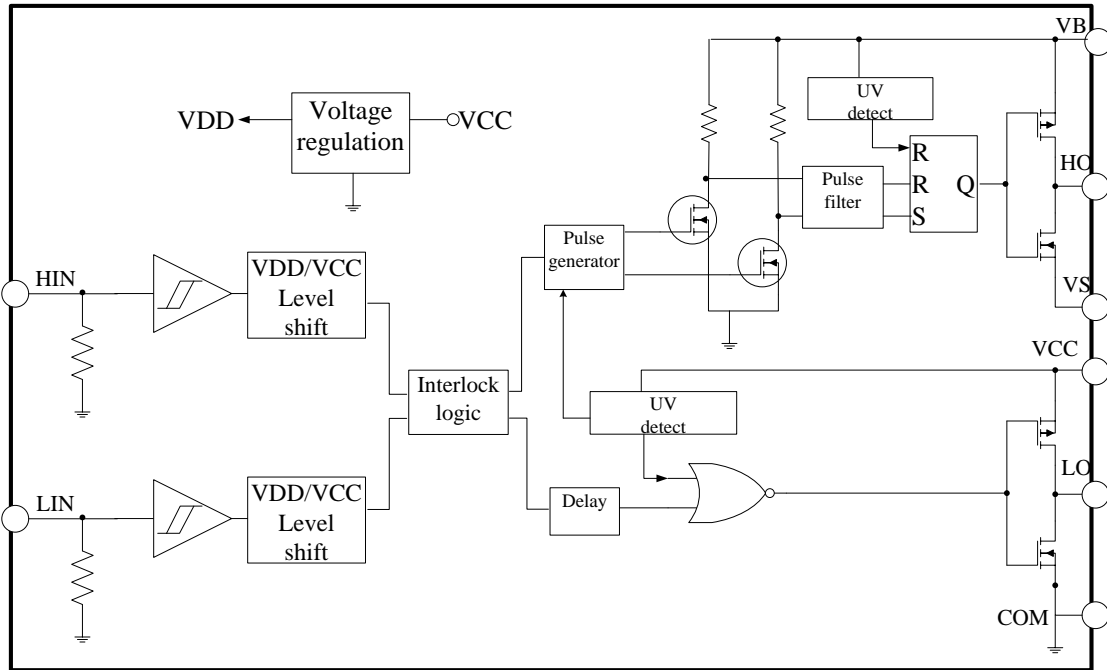


Figure2. Function Diagram of One HVIC

This HVIC for gate driving is mainly composed of Level shift, Interlock logic, Delay logic, Pulse generator, under-voltage protection, High and Low side drivers, etc.

The input signal LIN is input to the internal level shift through a Schmitt trigger, then gets through the delay circuit used for controlling the dead time, and finally arrives at the driver stage. The HIN input signal is also input to the internal level shift through a Schmitt trigger, then input into the pulse generator circuit, and outputs two fixed-frequency short pulses with fixed phase difference. Afterwards, the pulse level is converted to VB-VS signal by the level shifter, and then passes through the pulse filter module, inputs to the RS trigger with the output signal of the high-voltage channel under-voltage protection module together and finally outputs the high-voltage channel’s driving signal.

CS5755MT input/output control logic table is as follows:

INH	INL	Output	Note
0	0	Z	Both MOSFET Off
0	1	0	Low-side MOSFET On
1	0	VDC	High-side MOSFET On
1	1	Forbidden	Shoot-through
Open	Open	Z	Same as (0,0)

2. 3、 Pin Configuration

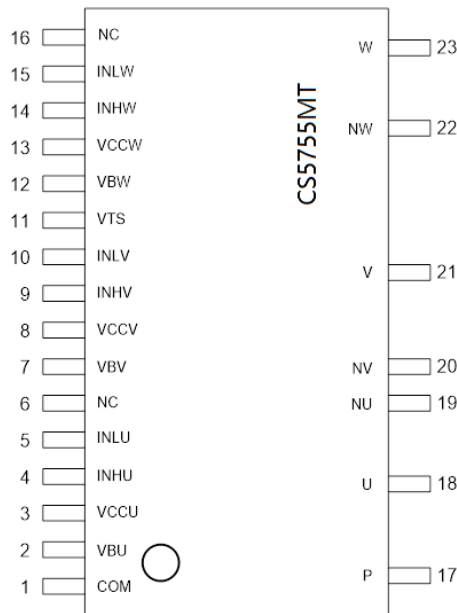


Figure3. Pin Configuration

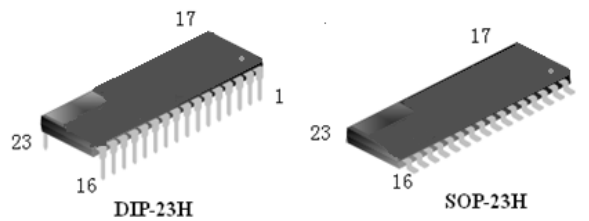


Figure4. Picture of Package

2. 4、 Pin Description

Pin	Symbol	Function	Attribute
1	COM	IC Common Supply Ground	I/O
2	VBU	Bias Voltage for U Phase High Side MOSFET Driving	I/O
3	VCCU	Bias Voltage for U Phase IC and Low Side MOSFET Driving	I/O
4	INHU	Signal Input for U Phase High-side	I
5	INLU	Signal Input for U Phase Low-side	I
6	NC	Empty Pin	-
7	VBV	Bias Voltage for V Phase High Side MOSFET Driving	I/O
8	VCCV	Bias Voltage for V Phase IC and Low Side MOSFET Driving	I/O
9	INHV	Signal Input for V Phase High-side	I
10	INLV	Signal Input for V Phase Low-side	I

To be continued

Continued

Pin	Symbol	Function	Attribute
11	VTS	Output for HVIC Temperature Sensing	-
12	VBW	Bias Voltage for W Phase High Side MOSFET Driving	I/O
13	VCCW	Bias Voltage for W Phase IC and Low Side MOSFET Driving	I/O
14	INHW	Signal Input for W Phase High-side	I
15	INLW	Signal Input for W Phase Low-side	I
16	NC	Empty Pin	-
17	P	Positive DC-link Input	I/O
18	U,VSU	Output for U Phase & Bias Voltage Ground for High Side MOSFET Driving	O
19	NU	Negative DC-link Input for U Phase	I/O
20	NV	Negative DC-link Input for V Phase	I/O
21	V,VSV	Output for V Phase & Bias Voltage Ground for High Side MOSFET Driving	O
22	NW	Negative DC-link Input for W Phase	I/O
23	W,VSW	Output for W Phase & Bias Voltage Ground for High Side MOSFET Driving	O

3、Electrical Characteristics

3.1、Absolute Maximum Ratings

Unless otherwise specified, $T_{amb}=25^{\circ}\text{C}$

Parameter	Symbol	Value	Unit
P-N Input Voltage	V_{PN}	500	V
Each MOSFET Drain Current, Continuous $T_C=25^{\circ}\text{C}$	I_{D25}	3.0	A
Each MOSFET Drain Current, Continuous $T_C=80^{\circ}\text{C}$	I_{D80}	2	A
Each MOSFET Drain Current, Peak $T_C=25^{\circ}\text{C}$, $PW<100\mu\text{s}$	I_{DP}	5.0	A
Maximum Power Dissipation $T_C=25^{\circ}\text{C}$	P_D	14.5	W
Control Supply Voltage	V_{CC}	20	V
High-side Control Voltage	V_{BS}	20	V
Input Signal Voltage	V_{IN}	$-0.3\sim V_{CC}+0.3$	V
Operating Junction Temperature	T_J	$-40\sim 150$	$^{\circ}\text{C}$
Shell Temperature Range $T_J\leq 150^{\circ}\text{C}$	T_C	$-40\sim 125$	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	$-50\sim 150$	$^{\circ}\text{C}$
Junction to Case Thermal Resistance	$R_{\theta JC}$	8.5	$^{\circ}\text{C}/\text{W}$
Isolation Voltage 60Hz, Sinusoidal, 1 Minute, Connection Pins to Heatsink	V_{ISO}	1500	V_{rms}

3. 2、 Recommended Operating Conditions

Unless otherwise specified, $T_{amb}= 25^{\circ}\text{C}$

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
P-N Input Voltage	V_{PN}	-	300	400	V
Control Supply Voltage	V_{CC}	13.5	15	16.5	V
High-side Control Voltage	V_{BS}	13.5	15	16.5	V
Input ON Threshold Voltage	$V_{IN(ON)}$	3.0	-	V_{CC}	V
Input OFF Threshold Voltage	$V_{IN(OFF)}$	0	-	0.8	V
Blanking Time for Preventing Arm-short	T_{DEAD}	1.0	-	-	μs
PWM Switching Frequency, $T_J \leq 150^{\circ}\text{C}$	f_{PWM}	-	15	20	kHz

3. 3、 Electrical Characteristics

3. 3. 1、 Inverter(Each MOSFET Unless Otherwise Specified)

Unless otherwise specified, $T_{amb}= 25^{\circ}\text{C}$, $V_{CC}= V_B= 15\text{V}$, $V_S= \text{COM}= 0$

Parameter	Symbol	Test Conditions	Value			Unit
			Min	Typ	Max	
Drain-source Breakdown Voltage	BV_{DSS}	$V_{IN}= 0\text{V}$ $I_D= 250\mu\text{A}(\text{Note1})$	500	-	-	V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_{JZ}$	$I_D= 250\mu\text{A}$ Referenced to 25°C	-	0.55	-	$\text{V}/^{\circ}\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{IN}= 0\text{V}$, $V_{DS}= 500\text{V}$	-	-	250	μA
Static Drain-source On-resistance	$R_{DS(ON)}$	$V_{CC}= V_{BS}= 15\text{V}$ $V_{IN}= 5\text{V}$, $I_D= 2.5\text{A}$	-	1.2	1.6	Ω
Drain-source Diode Forward Voltage	V_{SD}	$V_{CC}= V_{BS}= 15\text{V}$ $V_{IN}= 0\text{V}$, $I_D= -2.5\text{A}$	-	-	1.2	V
Switching Times	t_{ON}	$V_{PN}= 300\text{V}$	-	800	-	ns
	t_{OFF}	$V_{CC}= V_{BS}= 15\text{V}$	-	600	-	ns
	t_{RR}	$I_D= 0.5\text{A}$	-	80	-	ns
	E_{ON}	$V_{IN}= 0\text{V} \sim 5\text{V}$	-	70	-	μJ
	E_{OFF}	Inductive Load(Note2)	-	10	-	μJ

Note1: BV_{DSS} is the absolute voltage rating between drain and source terminal of each MOSFET. V_{PN} should be sufficiently less than this value considering the effect of the stray inductance so that V_{DS} should not exceed BV_{DSS} in any case;

Note2: t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. Listed values are measured at the laboratory test condition, and they can be different according to the field application due to the effect of different printed circuit boards and writings. Please see Figure 5 for switching time definition with the switching test circuit of Figure 6.

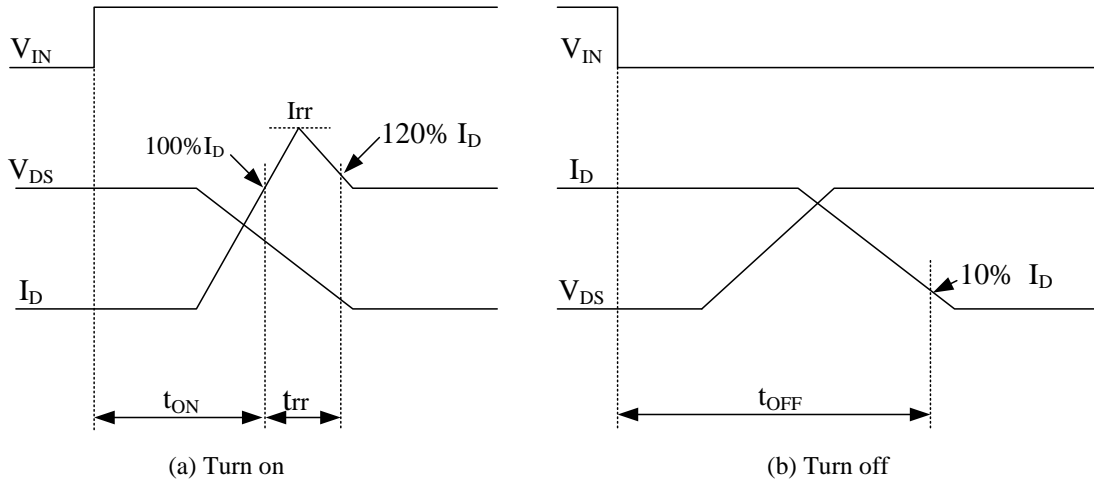


Figure5. Switching Time Definition

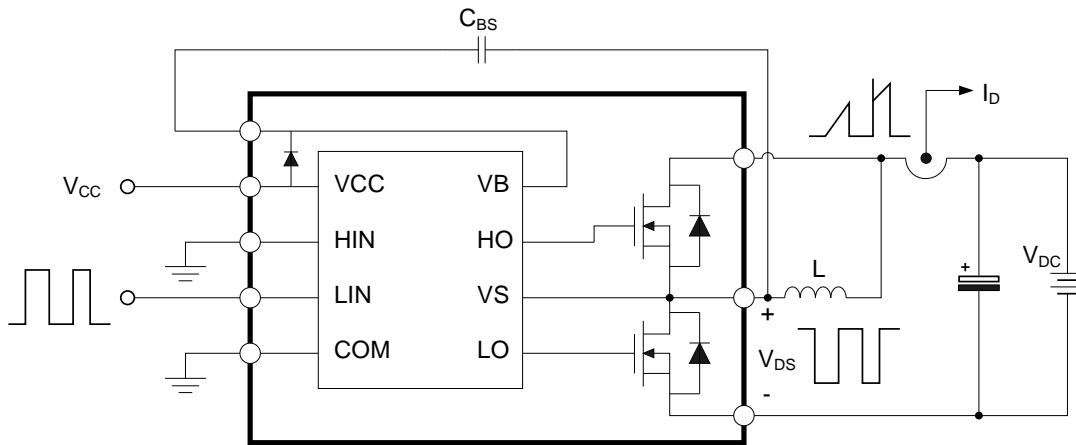


Figure6. Switching and RBSOA (Single-pulse) Test Circuit (Low-side)

3.3.2、Control Part(Each HVIC Unless Otherwise Specified)

Unless otherwise specified, $T_{amb} = 25^{\circ}\text{C}$, $V_{CC} = V_B = 15\text{V}$, $V_S = \text{COM} = 0$

Parameter	Symbol	Test Conditions	Value			Unit
			Min	Typ	Max	
Input ON Threshold Voltage	V_{IH}	$V_{CC} = 10\text{V} \sim 20\text{V}$	3	-	-	V
Input OFF Threshold Voltage	V_{IL}	$V_{CC} = 10\text{V} \sim 20\text{V}$	-	-	0.8	V
High-side Under-voltage Protection Detection Level	UV_{BSD}	-(Note3)	8.0	8.7	9.4	V
High-side Under-voltage Protection Reset Level	UV_{BSR}	-	8.6	9.4	9.9	V
Low-side Under-voltage Protection Detection Level	UV_{CCD}	-	8.3	9.1	9.7	V
Low-side Under-voltage Protection Reset Level	UV_{CCR}	-	8.8	9.5	10	V
Quiescent V_{BS} Current	I_{QBS}	$V_{BS} = 15\text{V}$ $V_{IN} = 0\text{V}$	-	-	100	μA
Quiescent V_{CC} Current	I_{QCC}	$V_{CC} = 15\text{V}$ $V_{IN} = 0\text{V}$	-	-	700	μA
Input Bias Current High Level	I_{IN+}	$V_{IN} = 5\text{V}$	-	10	20	μA
Input Bias Current Low Level	I_{IN-}	$V_{IN} = 0\text{V}$	-	-	2	μA
Temperature Sensing Voltage Output	V_{TS}	$V_{CC} = 15\text{V}$ $T = 25^{\circ}\text{C}$ (Note4)	600	790	980	mV

Note3: The timing diagram of the High-side and Low-side under-voltage protection function is shown in Figure 7 and Figure 8;

Note4: The temperature characteristic curve of the temperature sensing output voltage V_{TS} is shown in Figure 9.

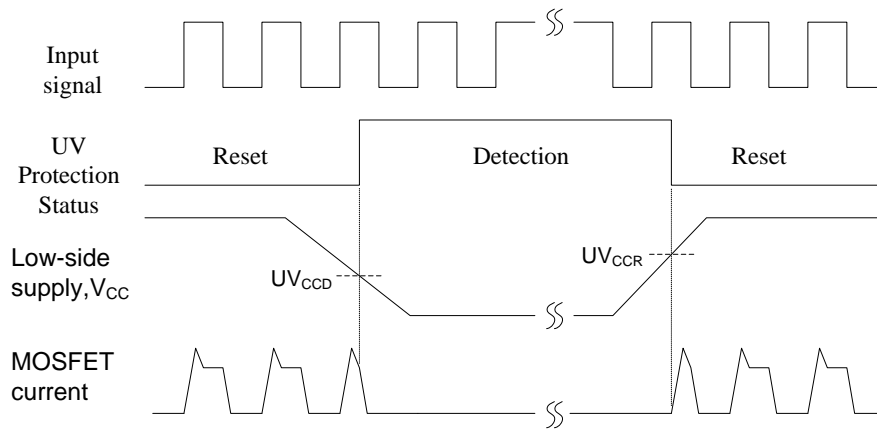


Figure7. Under-voltage Protection (Low-side)

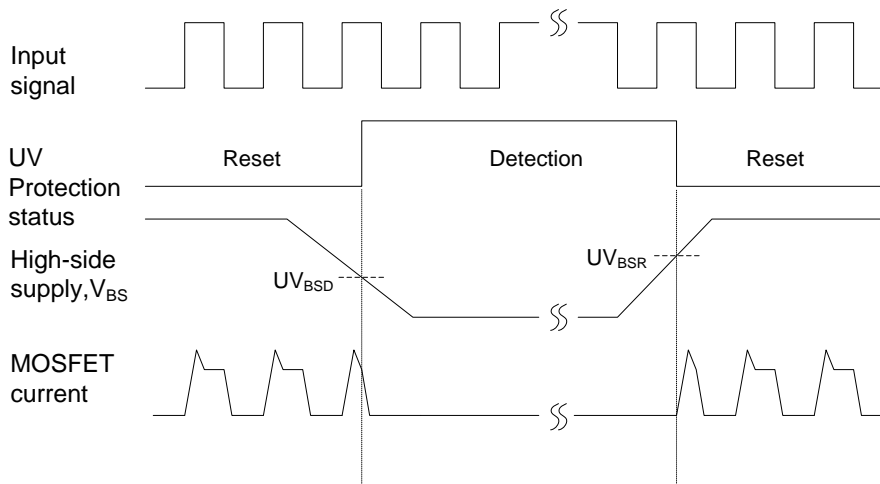


Figure8. Under-voltage Protection (High-side)

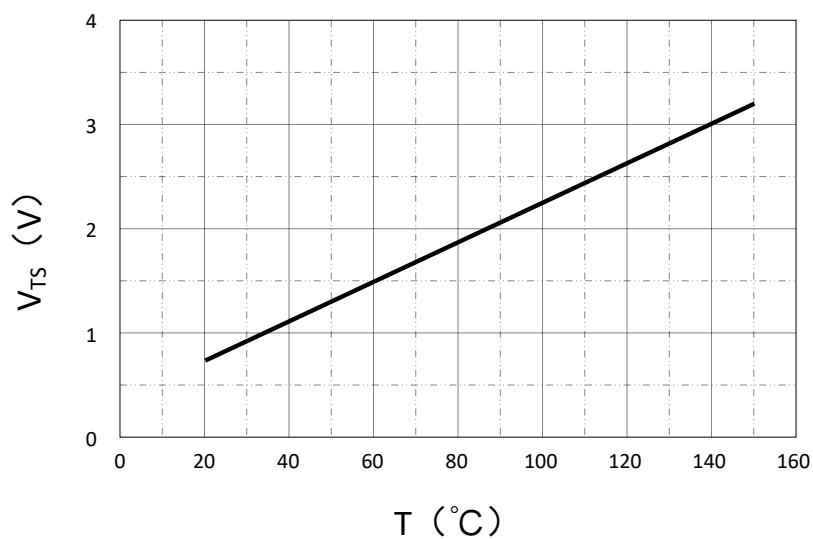


Figure9. Temperature Profile of V_{TS} (Typ)

3.3.3. Bootstrap Diode Part

Unless otherwise specified, $T_{amb} = 25^{\circ}\text{C}$, $V_{CC} = V_B = 15\text{V}$, $V_S = \text{COM} = 0$

Parameter	Symbol	Test Conditions	Value			Unit
			Min	Typ	Max	
Maximum Repeated Reverse Voltage	V_{RRM}	-	-	600	-	V
Forward Voltage	V_F	$I_F = 0.1\text{A}$, $T = 25^{\circ}\text{C}$	-	0.7	-	V
Forward Current	I_F	$T = 25^{\circ}\text{C}$	-	0.5	-	A
Forward Peak Current	I_{FP}	$T = 25^{\circ}\text{C}$ Duration $\leq 1\text{ms}$	-	-	-	A
Reverse recovery time	t_{RR}	$I_F = 0.1\text{A}$, $T = 25^{\circ}\text{C}$	-	50	-	ns
Resistance	R_{BOOT}	-	20	-	60	Ω

4. Typical Application Circuit and Information

4.1. Application Circuit

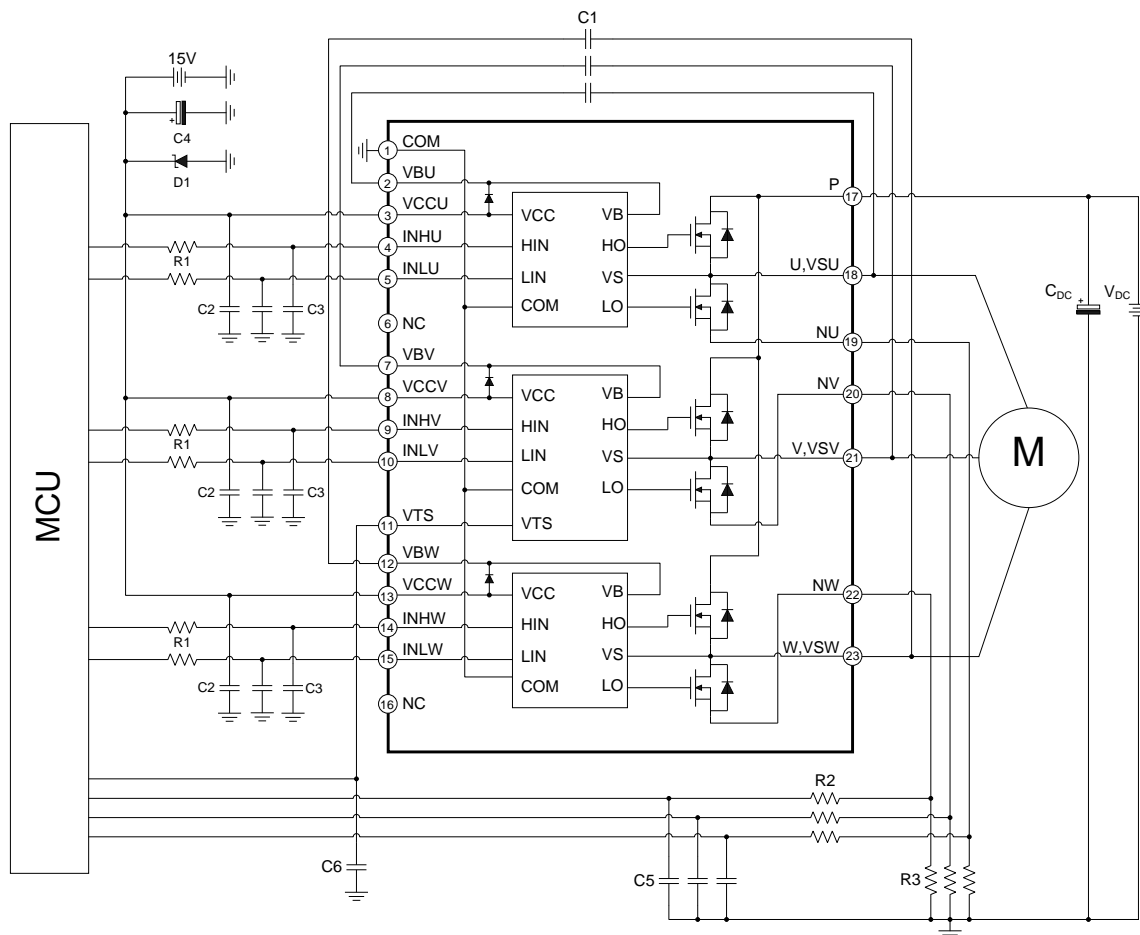


Figure10. Example of Application Circuit

4. 2、 Applications Information

(1) Keep the trace between the MCU and IPM as short as possible. If necessary, an RC filter circuit can be added to the input of gate to prevent improper input signal caused by surge noise, but the RC value must be selected carefully;

(2) INH and INL have internal pull-down resistors, additional pull-down resistors can be connected if necessary;

(3) A $1\mu\text{F}$ capacitor should be placed near each VCC pin that controls the HVIC and as close to the IPM as possible;

(4) In order to prevent the surge damage, a high-frequency non-inductive smooth capacitor is suggested to add between the P terminal of the IPM and the ground terminal of the resistor R3. The connecting line of capacitances should be as short as possible;

(5) It's best to add a filter capacitor at least 7 times the bootstrap capacitor at the VCC input;

(6) Suggest using high-frequency capacitor C1 (more than $2.2\mu\text{F}$) as bootstrap capacitance to absorb the high-frequency ripple;

(7) Connecting line between current-limiting resistor R3 and IPM should be as short as possible to avoid the line inductance causing surge voltage, which can break IPM down.

4. 3、 Design of Bootstrap Circuit

4. 3. 1、 Operating Principles of Bootstrap Circuit

The High-side circuit in HVIC is powered by the floating power supply V_{BS} , which is generated by bootstrap method, which is simple and economical. The bootstrap power supply consists of a built-in bootstrap diode and an external bootstrap capacitor C_{BS} .

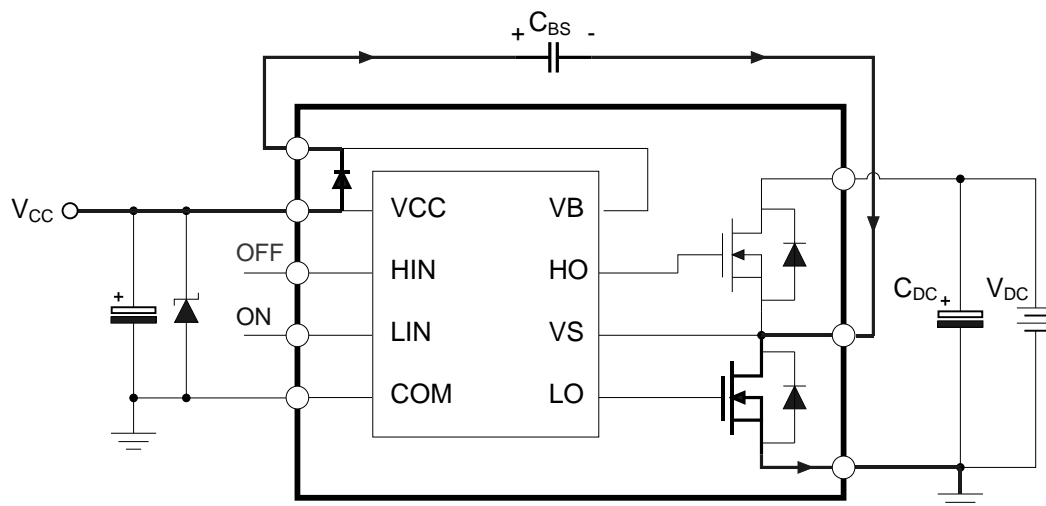


Figure11. Bootstrap Circuit and Current Path

The current path of bootstrap circuit is shown in Figure 11. When the low-side power MOSFET is turned on, the power supply VCC charges the bootstrap capacitor C_{BS} through the bootstrap diode. It takes time to charge the bootstrap capacitor thus limiting the duty cycle and on-time of the circuit operation. The low-side MOSFET should have sufficient on-time after the circuit is powered on.

The recommended working range of V_{BS} voltage is 13.5V~16.5V in order to have enough gate voltage to drive the high-side MOSFET. The under-voltage protection function of the power supply V_{BS} is designed in the HVIC to ensure that the high-side MOSFET will not be driven when the V_{BS} voltage is lower than the protection voltage to avoid the MOSFET operating in a high power consumption mode.

4.3.2、 Selection of Bootstrap Capacitor

The bootstrap capacitor can be calculated by the following formula:

$$C_{BS} = \frac{I_{LEAK} \times \Delta t}{\Delta V_{BS}}$$

Thereinto, Δt : maximum on-time of high-side MOSFET;

ΔV_{BS} : the allowable discharge voltage of C_{BS} (voltage ripple);

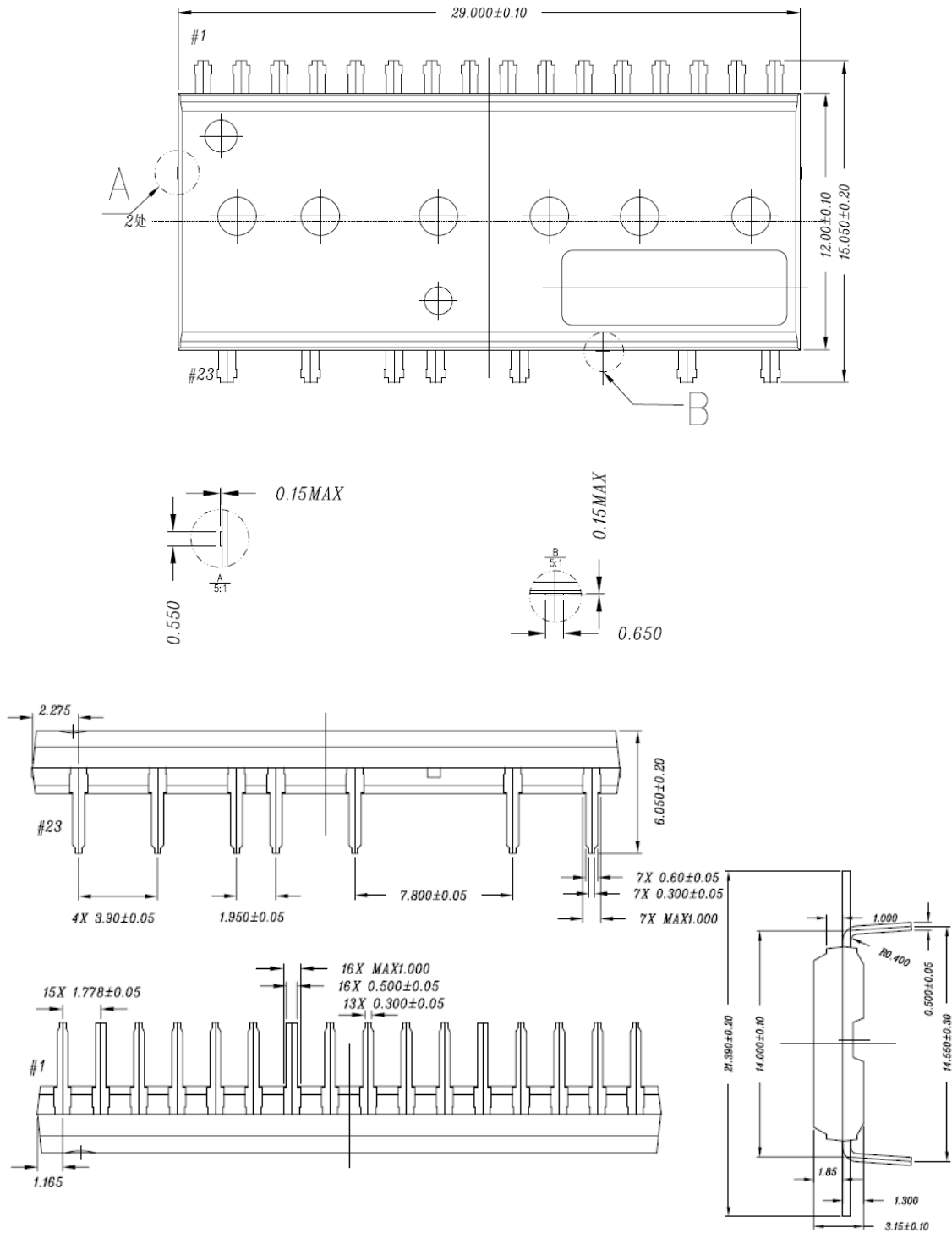
I_{LEAK}: maximum discharge current of C_{BS}, including:

- Quiescent current of the high-side circuit in HVIC
- Gate charge for turning the high-side MOSFET on
- Level shift charge required by level shifters in HVIC
- Leakage current of bootstrap diode
- Reverse recovery charge of bootstrap diode

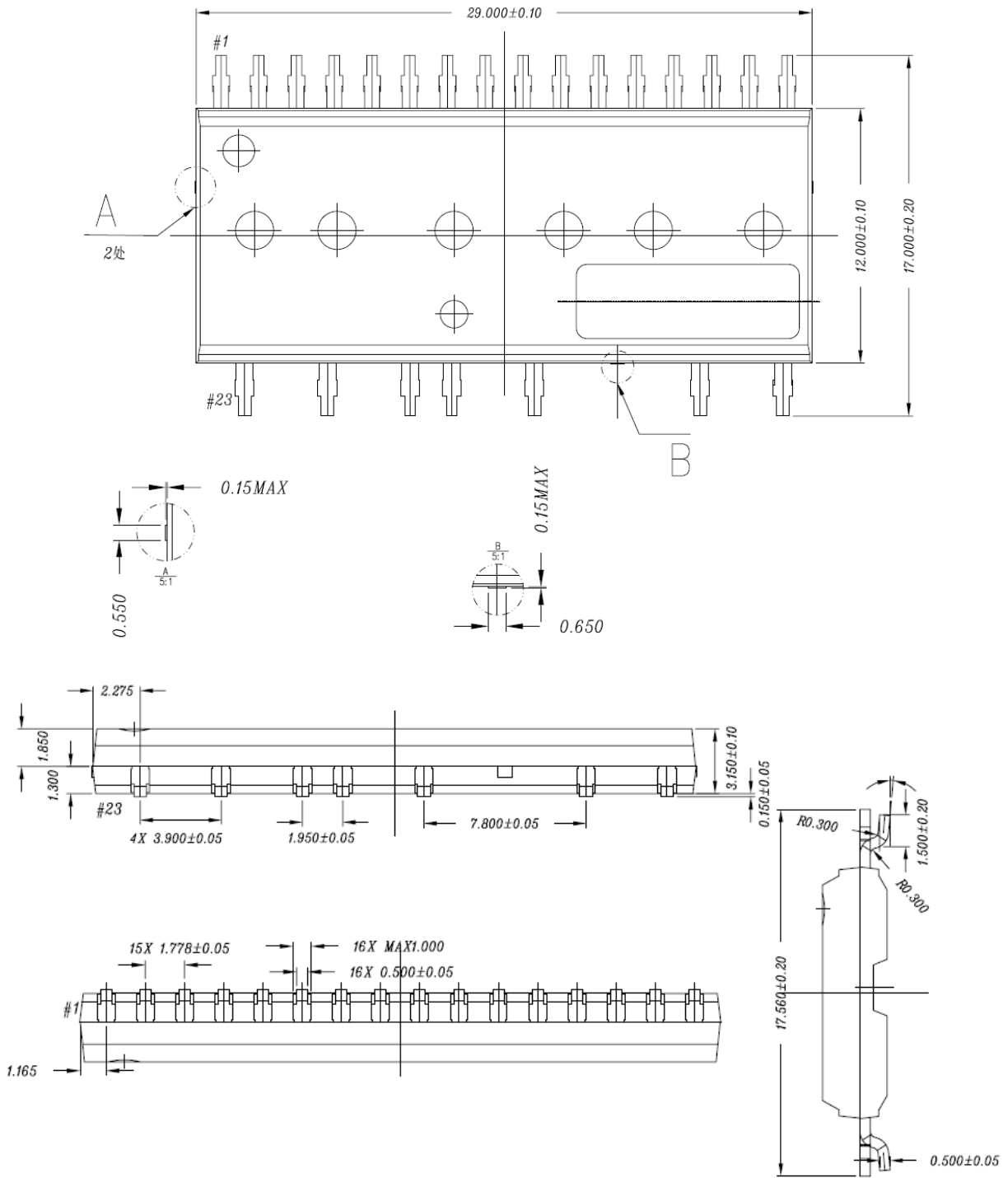
In actual use, the capacitor value is usually selected to be twice the calculated value to ensure reliability.

5、Package Dimensions (Unit: mm)

5.1、DIP23-H



5. 2、SOP23-H



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