

GENERAL DESCRIPTION

OB3636 is a flyback controller with high power factor, low THD and high constant voltage(CV) precision. It can achieve low system cost for an isolated application by primary side control in a single stage converter. It significantly simplifies the CV system design by eliminating the secondary side feedback components and the opto-coupler.

The proprietary CV control scheme is used and the system can achieve high power factor with constant on-time control scheme. Quasi-resonant (QR) operation and clamping frequency greatly improves the system efficiency. The advanced start-up technology is used to meet the start-up time requirement (<0.5s).

OB3636 offers comprehensive protection including open loop protection, short circuit protection, cycle-by-cycle current limiting, built-in leading edge blanking, VDD under voltage lockout (UVLO), etc.

OB3636 is offered in SOT23-6 package.

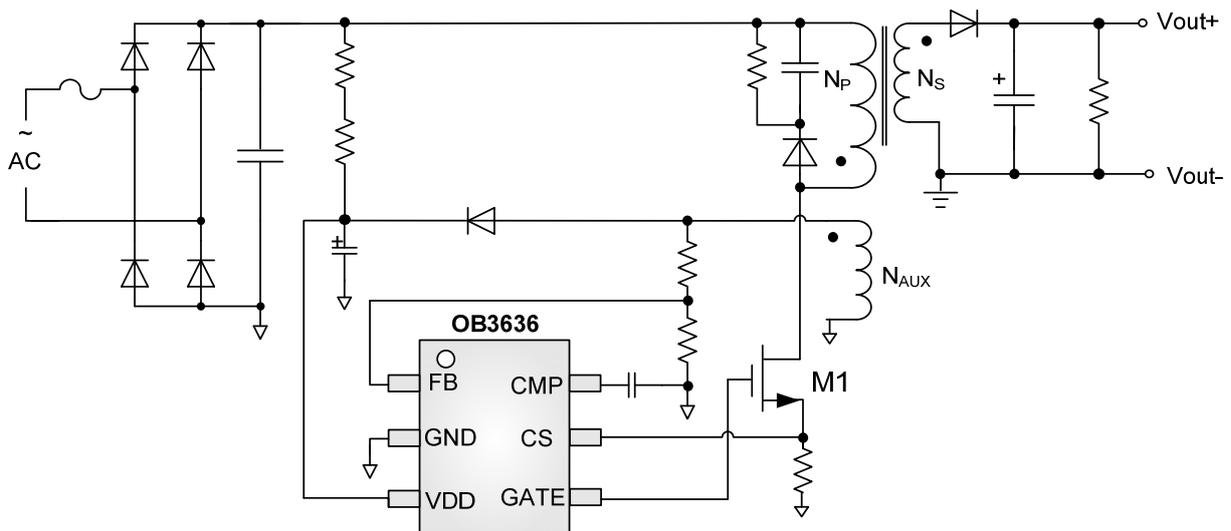
FEATURES

- High PF (>0.9)
- Low THD (<10%)
- High precision constant voltage regulation
- Fast start-up (<0.5s)
- Primary-side sensing and regulation without TL431 and opto-coupler
- Low system cost and high efficiency
- Quasi-resonant operation
- Short circuit protection
- Open loop protection
- Cycle-by-cycle current limiting
- Built-in leading edge blanking (LEB)
- VDD under voltage lockout with hysteresis
- VDD over voltage protection
- Over temperature protection (OTP)
- Audio Noise Free

APPLICATIONS

- LED lighting
- AC/DC adapters

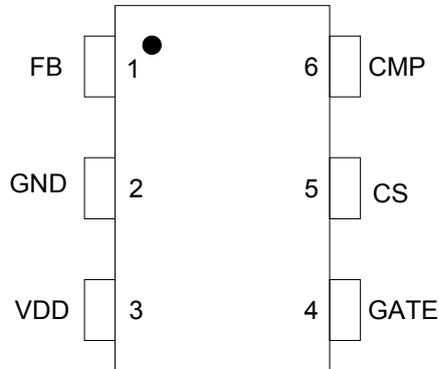
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The pin map is shown as below for SOT23-6.



Ordering Information

Part Number	Description
OB3636MP	SOT23-6, Halogen-free in T&R

Note: All Devices are offered in Halogen-free Package if not otherwise noted.

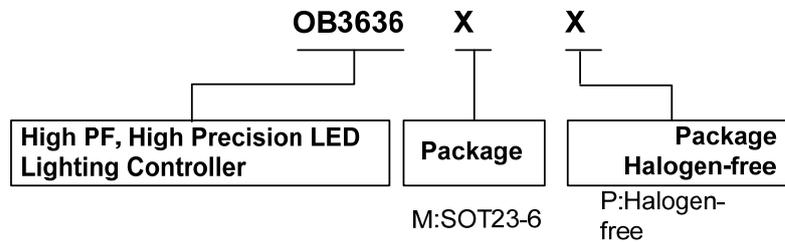
Package Dissipation Rating

Package	R θ JA (°C/W)
SOT23-6	200

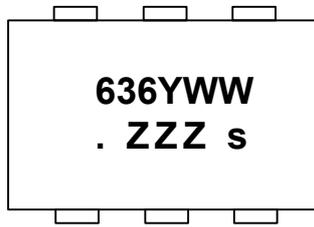
Absolute Maximum Ratings

Parameter	Value
VDD Voltage	-0.3 to 40V
GATE Voltage	-0.3 to 40V
CS Input Voltage	-0.3 to 7V
FB Input Voltage	-0.3 to 7V
CMP Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T _J	-40 to 150 °C
Operating Ambient Temperature T _A	-20 to 85 °C
Min/Max Storage Temperature T _{stg}	-55 to 150 °C
Lead Temperature (Soldering, 10secs)	260 °C

Note: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



Marking Information

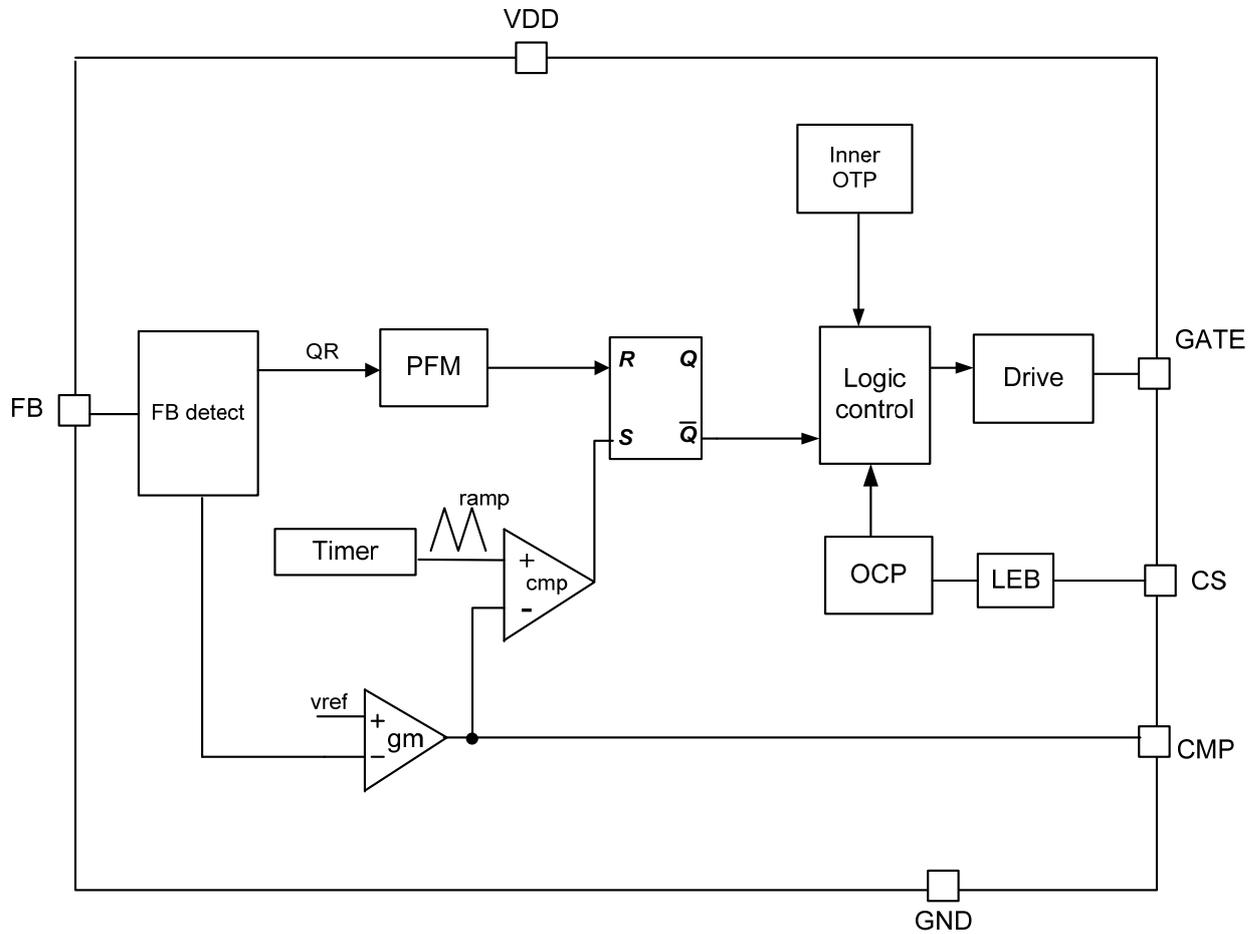


Y:Year Code
 WW:Week Code(01-52)
 ZZZ: Lot code
 s: Internal code

TERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1	FB	I	Voltage feedback from auxiliary winding. Connected to resistor divider from auxiliary winding reflecting output voltage.
2	GND	P	Power ground.
3	VDD	P	Power supply.
4	GATE	O	Gate driver output for power MOSFET.
5	CS	I	Current sense input pin.
6	CMP	O	Loop compensation pin. A capacitor is connected between CMP and GND.

BLOCK DIAGRAM

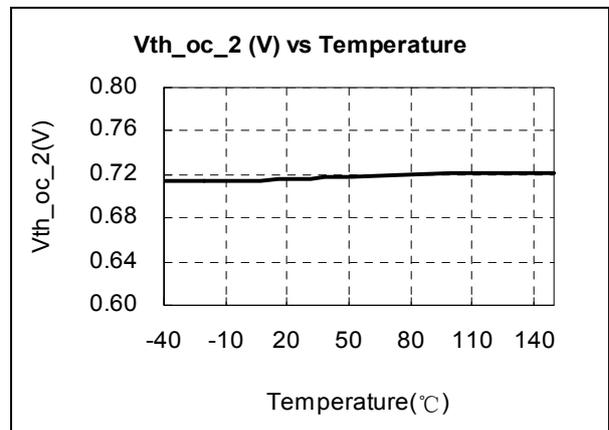
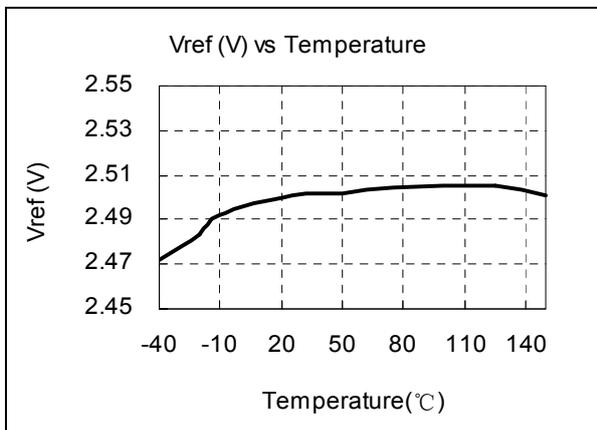
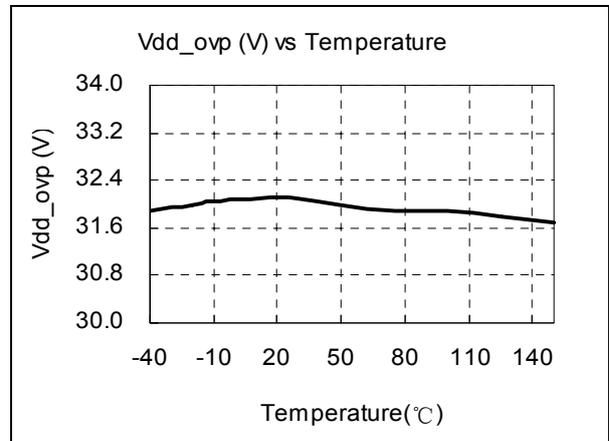
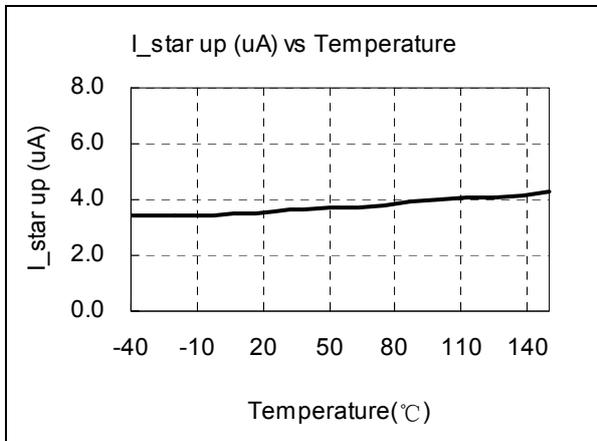
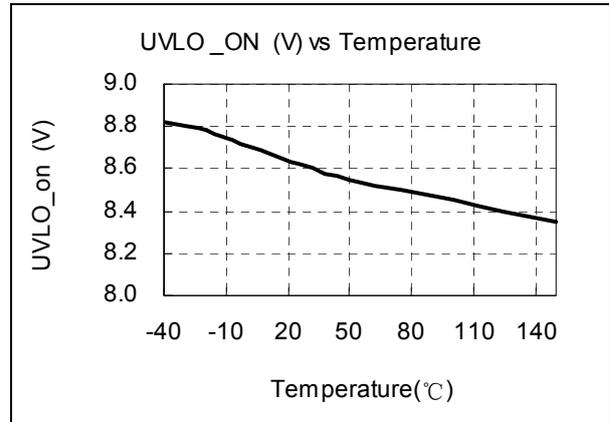
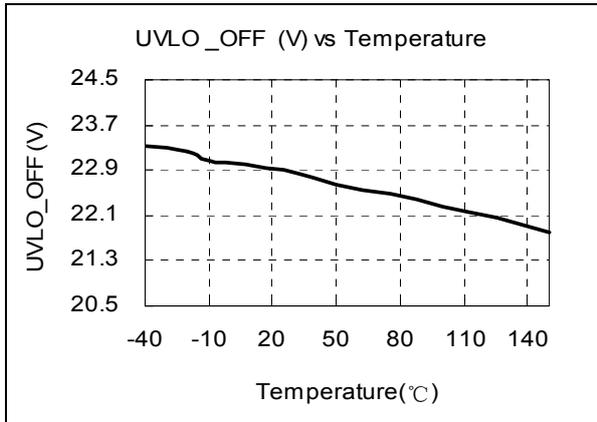


ELECTRICAL CHARACTERISTICS

(TA = 25°C, VDD=20V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage (VDD) Section						
I _{DD ST}	Standby Current	VDD=UVLO(OFF)-1V		3	7	uA
I _{OP}	Static Current	VDD=20V		850	1100	uA
UVLO(ON)	VDD Under Voltage Lockout Enter	VDD falling	7	8	9	V
UVLO(OFF)	VDD Under Voltage Lockout Exit	VDD rising	20	22.5	25	V
VDD_OVP	VDD Over Voltage Protection		29	32	35	V
FB Section						
V _{ovp}	Output over voltage protection		3	3.2	3.4	V
V _{th_fb_scp}	FB short protection			0.4		V
Gm amplifier section						
V _{ref}	Error Amplifier Reference Voltage		2.375	2.5	2.625	V
G _m	Error Amplifier Transconductance Gain			40		uS
V _{clamp_cmp}	CMP pin clamping voltage			0.8		V
CS Section						
TLEB	Leading Edge Blanking time			300		ns
V _{th_oc}	Over Current Threshold	T _{on} ≥10us		1.1		V
V _{th_oc_2}	Over Current Threshold	T _{on} =0us		0.7		V
QR Section						
F _{max}	Maximum Clamping Frequency			100		KHz
T _{off_max}	Maximum Off Time			70		us
T _{on_max}	Maximum On Time			20		us
F _{min}	Minimum frequency			500		Hz
OTP section						
OTP	Over Temperature Protection trigger threshold			150		°C
Gate Drive Output Section						
V _{ol}	Output Low Level				1	V
V _{oh}	Output High Level		6			V
V _{clamp}	Output Clamping Voltage			12		V
T _r	Rising Edge Time	CL=1nF		80		ns
T _f	Falling Edge Time	CL=1nF		30		ns

CHARACTERIZATION PLOTS



OPERATION DESCRIPTION

OB3636 is a cost effective PSR power switch optimized for high PFC and low THD constant voltage applications. It operates in primary side sensing and regulation, thus opto-coupler and TL431 are not required. Proprietary built-in constant on time control can achieve high power factor control meeting most application requirements.

Startup Current and Start up Control

The advanced start-up technology is used in OB3636 to meet the start-up time requirement (<0.5s). Low start-up current is designed in OB3636 so that VDD could be charged up above UVLO threshold with small charging current.

During the startup, the capacitor at CMP pin is pulled up quickly. OB3636 operates at open loop and over-current protection is set cycle-by-cycle until it senses the output voltage by FB pin up to about 2.4V. After that OB3636 operates in close loop, the transconductance of error amplifier is set to 40uS (typical).

Error Amplifier

Connected to a resistor divider from output line, the inverting input of the Error Amplifier (EA) is compared to an internal reference voltage(2.5V) to regulate the output voltage.

The EA output is internally connected to the CMP pin and externally connected for loop compensation. It is usually realized with a capacitor which connected between GND and EA output. The system loop bandwidth is set below 20 Hz to suppress the AC ripple of the line voltage.

Output voltage regulation

In order to achieve primary side constant voltage control, the output voltage is detected by the auxiliary winding voltage. During OFF time, the voltage across the auxiliary winding is:

$$V_A = (V_{OUT} + V_{DF}) \frac{N_A}{N_S}$$

N_A is the turns of auxiliary winding
 N_S is the turns of secondary winding
 V_{DF} is the forward voltage of the power diode

At the current zero-crossing point, V_{DF} is nearly zero, so V_{OUT} is proportional with V_A exactly. The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by:

$$V_{OUT} = \frac{V_{ref}}{\frac{N_A R_2}{N_S R_1 + R_2}}$$

V_{ref} is the internal voltage reference
 R_1 is resistance of the high side divider
 R_2 is resistance of the low side divider

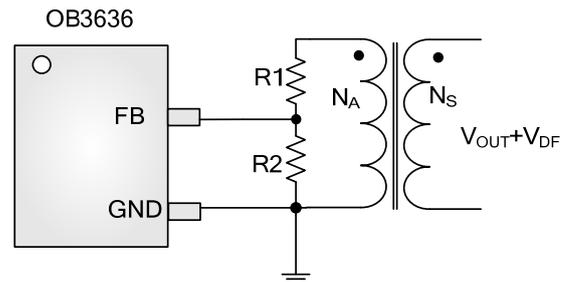


Figure.1 FB Section Circuit

PFC and THD

The duration of the turn on period t_{on} is generated by comparing an internal fixed saw-tooth wave with the voltage on the CMP pin. During steady state operation, the voltage on the CMP pin V_{cmp} is slowly varying due to a large external capacitor connected at the CMP pin, therefore the turn on time t_{on} is constant. In a fly-back topology, constant turn on time and quasi-resonant operation provide high power factor (PF) and low total harmonic distortion (THD).

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting (OCP) is offered in OB3636. The switching current is detected by a sense resistor connected between the CS pin and GND. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to snubber diode reverse recovery so that the external RC filter is no longer required. The current limit comparator is disabled at this blanking time and thus the external MOSFET cannot be turned off during this blanking time.

Quasi-Resonant Operation

OB3636 performs quasi-resonant detection through FB pin by monitoring the voltage activity on the primary windings in series with external resistors. When the stored energy of fly-back transformer is fully released to the output, the voltage at FB pin decreases. When FB pin voltage falls below 0V (typical), an internal FB comparator is triggered and a new PWM switching cycle is initiated following the FB triggering.

Short Circuit Protection

When output is short, the FB voltage is low. If the voltage at FB pin is lower than a threshold of approximately 0.4 V (typical), the threshold voltage of OCP is reduced to 0.4 V (typical). The power dissipation is greatly reduced in this way.

Open Circuit Protection

When the open circuit happens, the FB pin voltage is high. If the voltage at FB pin is higher than a threshold of approximately 3.2V (typical), the IC will shut down and enter power on startup sequence thereafter.

Gate Drive Output

The output stage is designed to ensure zero cross-conduction current. This minimizes heat dissipation, increase efficiency, and enhance reliability. The built-in 12V clamp at the gate output

protects the MOSFET gate from high voltage stress.

Over Temperature Protection

Over temperature protection is offered in OB3636. When temperature of the device rises over 150°C (typical), the IC will shut down. And the state will be kept until the device restarts.

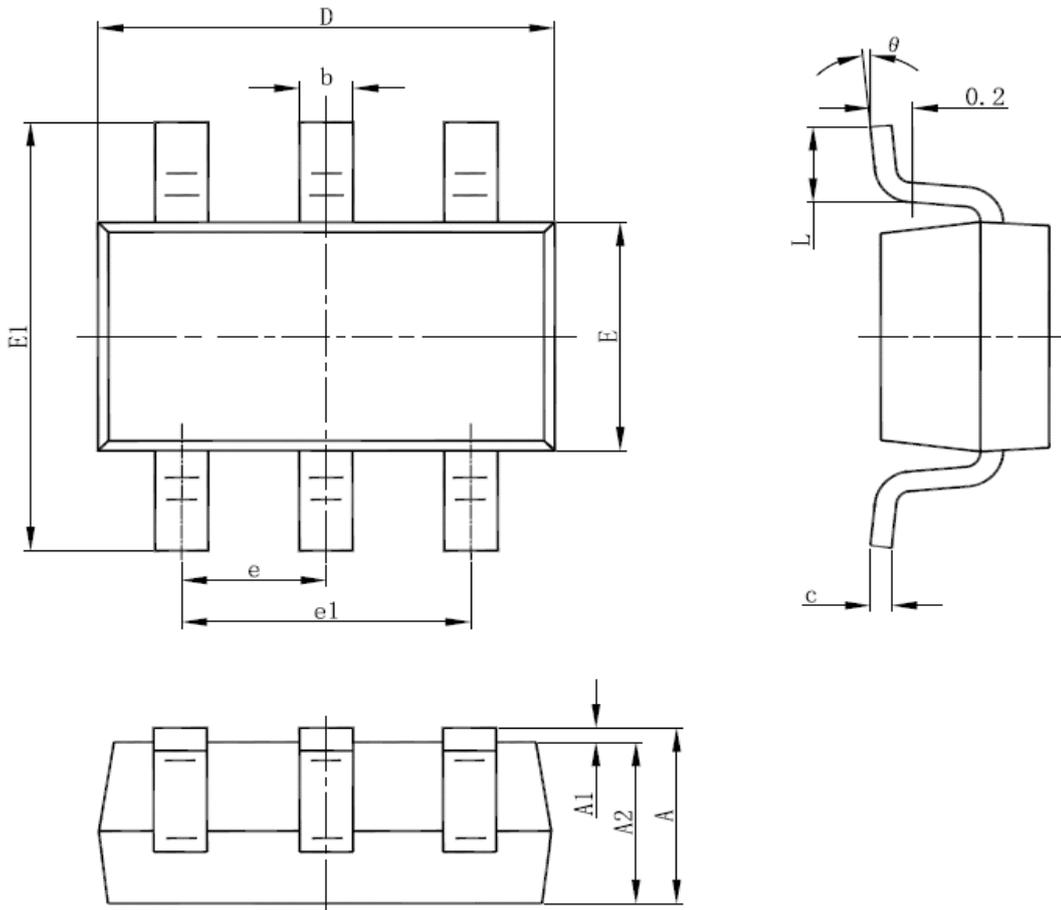
Protection Controls

OB3636 ensures good reliability design through its good protection coverage. Output dynamic and static over-voltage protection (OVP), VDD under voltage lockout (UVLO), VDD over-voltage protection (VDD OVP), cycle-by-cycle current limiting, Diode short protection and output gate clamp are standard features provided by OB3636.

PACKAGE MECHANICAL DATA

6-Pin Plastic SOT (SOT23-6)

SOT-23-6L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.450	0.039	0.057
A1	0.000	0.150	0.000	0.006
A2	0.900	1.300	0.035	0.051
b	0.300	0.500	0.012	0.020
c	0.080	0.220	0.003	0.009
D	2.800	3.020	0.110	0.119
E	1.500	1.726	0.059	0.068
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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