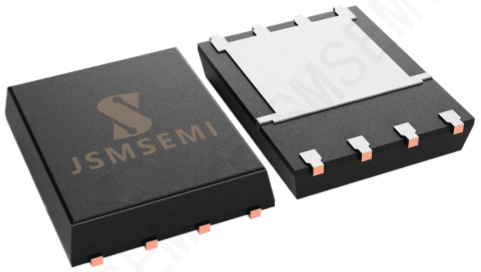
Product Summary

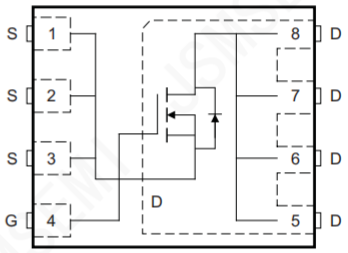
- V_{DS} 60V
- I_D 100A
- $R_{DS(ON)}$(at V_{GS}=10V) <3.4mΩ
- 100% EAS Tested
- 100% ∇V_{DS} Tested



General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Top View



Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor
- Motor drivers

■ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_C=25℃	I_D	100	A
	T_C =100℃		70	
Pulsed Drain Current [A]		I_{DM}	400	A
Avalanche energy [B]		EAS	340	mJ
Total Power Dissipation [C]	T_C=25℃	P_D	120	W
	T_C=100℃		50	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [D]	Steady-State	$R_{\theta JA}$	35		℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.85		

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship, Quantity	Green
BSC034N06NSATMA1-JSM	DFN5060-8L	023N06QGL	-55 to 150°C	1	T&R,5000	Rohs

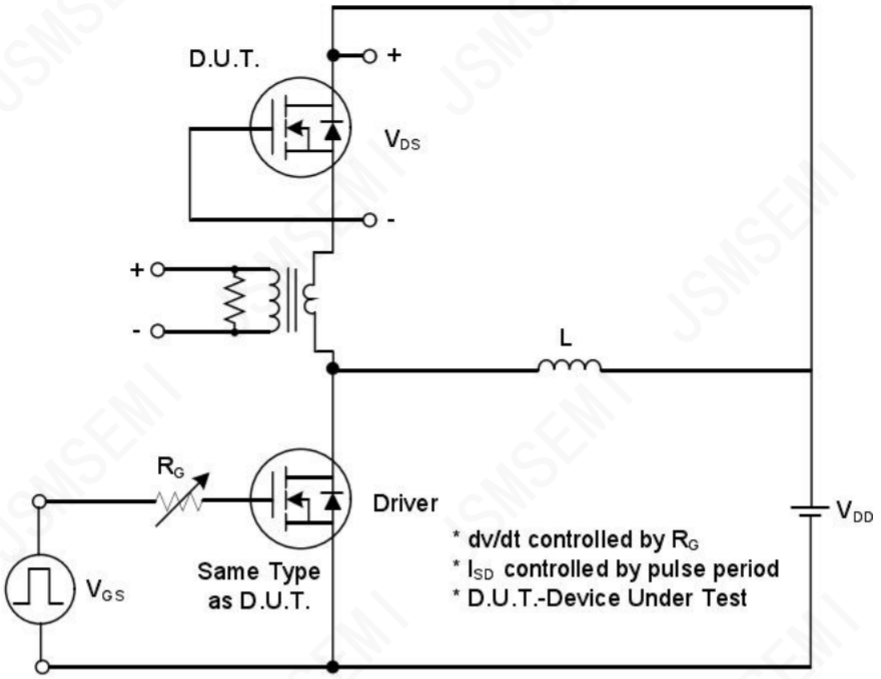
■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics (6)						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	-	-	1.0	μA
		T_J = 125°C	-	-	100	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
On Characteristics (6)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	1.3	1.7	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 20A	-	2.8	3.4	mΩ
Forward Transconductance	g_{fs}	V_{DS} = 5.0V, I_D = 20A	-	42	-	S
Diodes Forward Voltage	V_{SD}	I_S = 2.0A, V_{GS} = 0V	-	0.7	1.2	V
Dynamic Characteristics (7)						
Input Capacitance	C_{iss}	V_{DS} = 30V, V_{GS} = 0V, f = 1MHz	-	3183	-	pF
Output Capacitance	C_{oss}		-	914	-	pF
Reverse Transfer Capacitance	C_{rss}		-	9	-	pF
Gate Resistance	R_g	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz	-	1.8	-	Ω
Switching Characteristics (7)						
Turn-On DelayTime	$t_{d(on)}$	V_{GS} = 10V, V_{DS} = 30V I_D = 20A, R_{GEN} = 3.0Ω	-	8.5	-	ns
Rise Time	t_r		-	18	-	ns
Turn-Off DelayTime	$t_{d(off)}$		-	65	-	ns
Fall Time	t_f		-	28	-	ns
Gate Charge Characteristics (7)						
Total Gate Charge (V_{GS} = 10V)	Q_g	V_{DS} = 30V, I_D = 20A V_{GS} = 10V	-	94	-	nC
Total Gate Charge (V_{GS} = 6.0V)	Q_g		-	60	-	nC
Gate-Source Charge	Q_{gs}		-	25	-	nC
Gate-Drain Charge	Q_{gd}		-	23	-	nC
Gate Plateau Voltage	$V_{plateau}$		-	4.4	-	V
Drain-Source Diode Characteristics (7)						
Body Diode Reverse Recovery Time	t_{rr}	I_F = 20A, dI/dt = 100A/μs, T_J = 25°C	-	66	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	131	-	nC
Diode Forward Current	I_S	T_C = 25°C	-	-	100	A

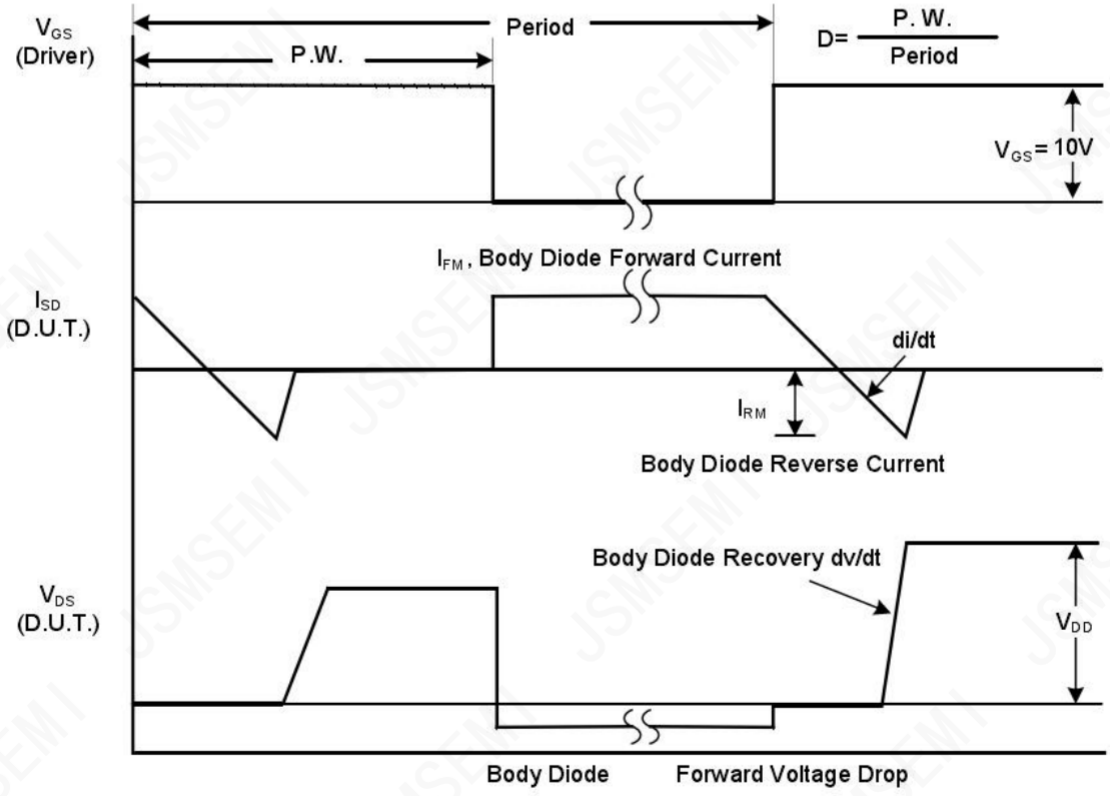
Notes:

1. This current is chip limited, which is calculated based on Rthjc.
2. This current is calculated on single pulse with 10μs Single Pulse.
3. Defined by design, not subject to production test, E_{AS} condition: T_J=25°C, V_{DD}=30V, V_{GS}=10V, L=1.0mH.
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to the exposed drain pad.
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.

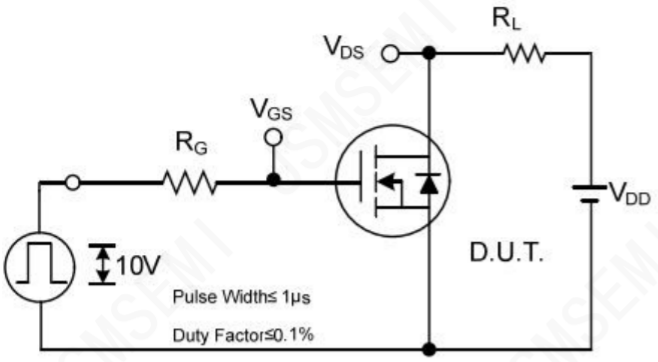
■ RATING AND CHARACTERISTIC CURVES



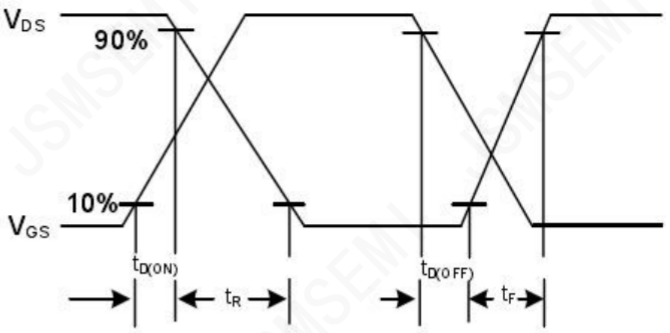
Peak Diode Recovery dv/dt Test Circuit



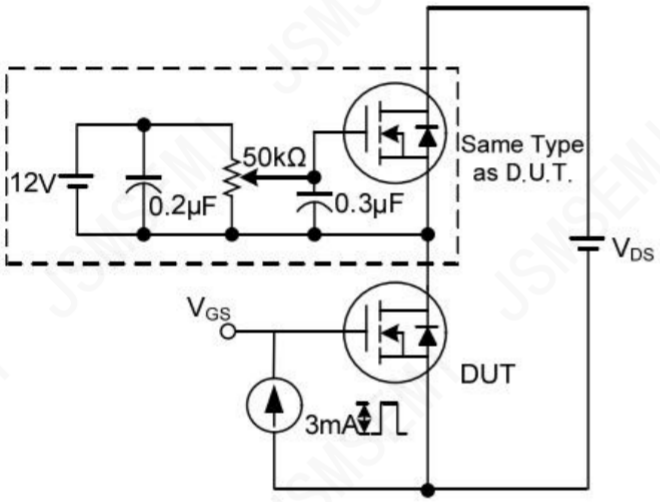
Peak Diode Recovery dv/dt Waveforms



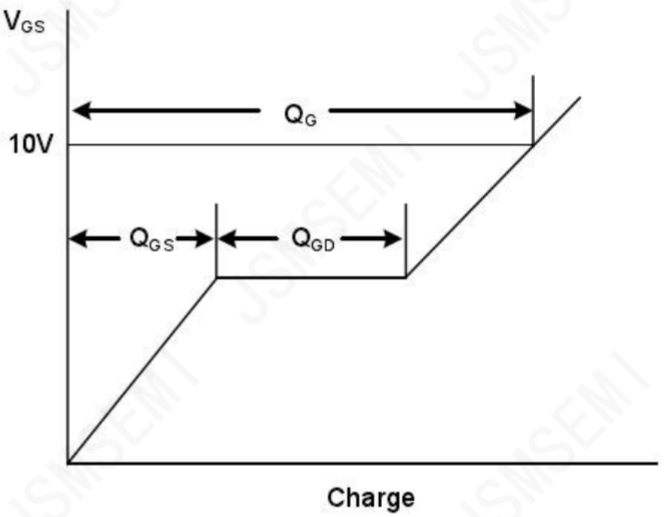
Switching Test Circuit



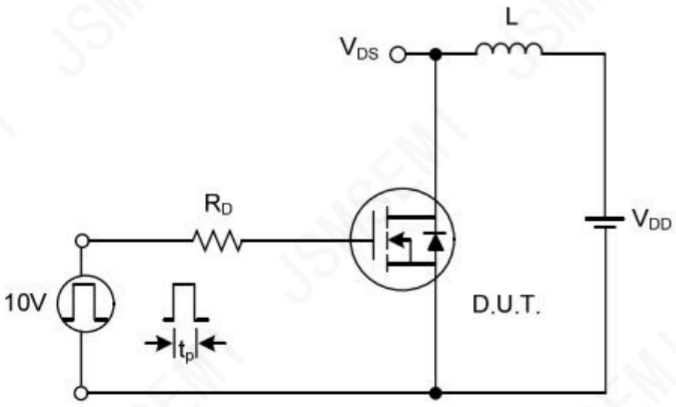
Switching Waveforms



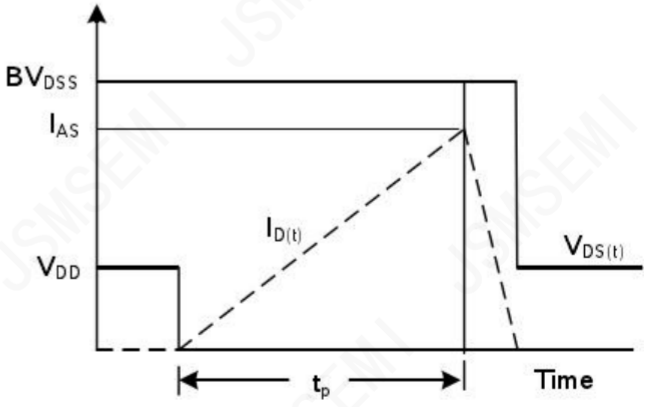
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

■Typical Electrical and Thermal Characteristics Diagrams

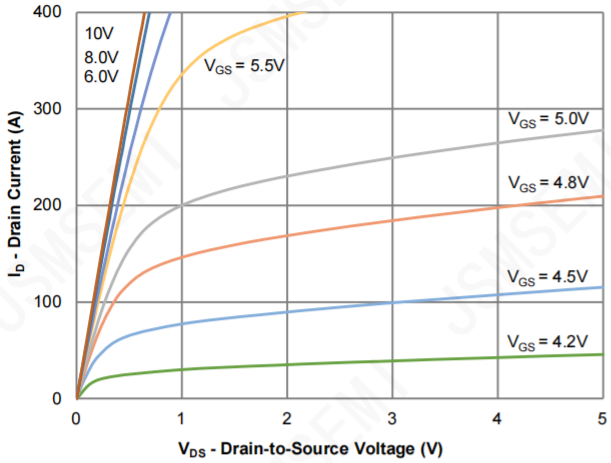


Figure 1: Output Characteristics

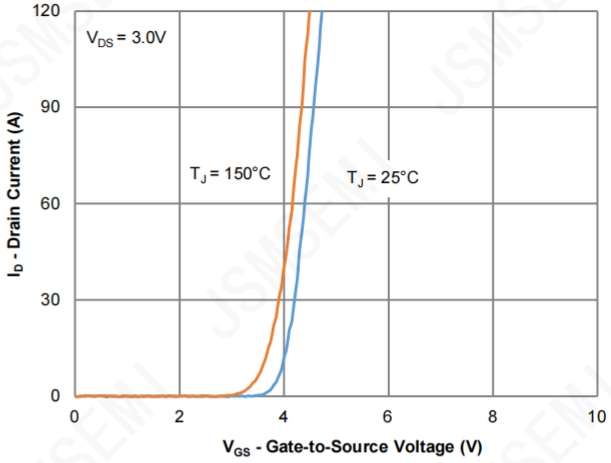


Figure 2: Transfer Characteristics

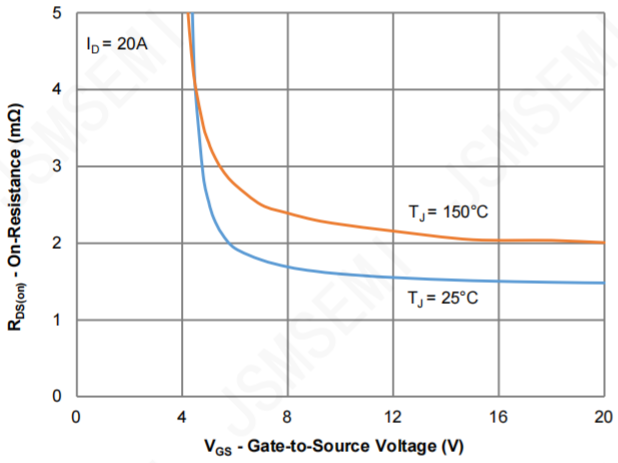


Figure 3: On-Resistance vs. Gate-Source Voltage

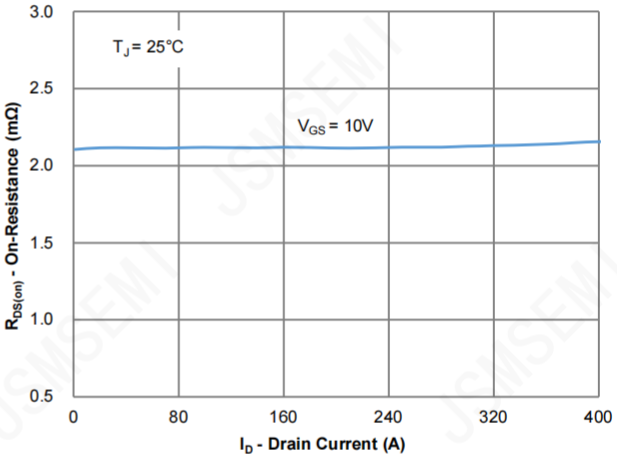


Figure 4: On-Resistance vs. Drain Current and Gate Voltage

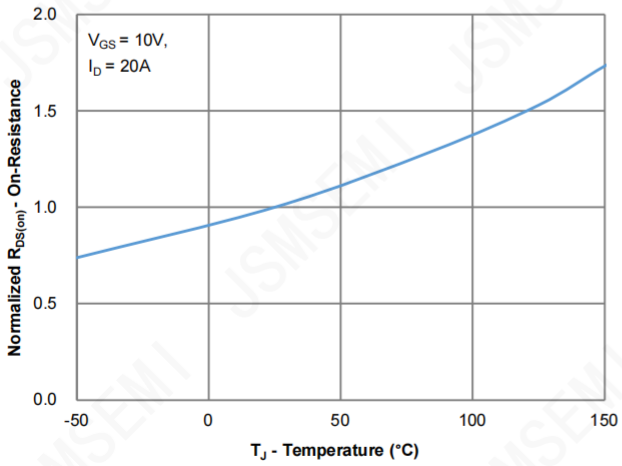


Figure 5: On-Resistance vs. Junction Temperature

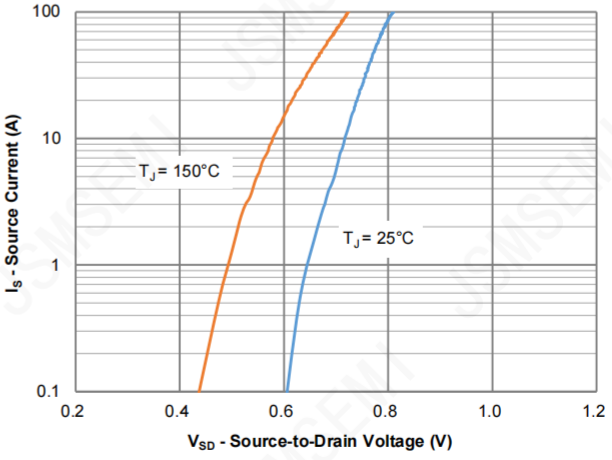


Figure 6: Source-Drain Diode Forward Voltage

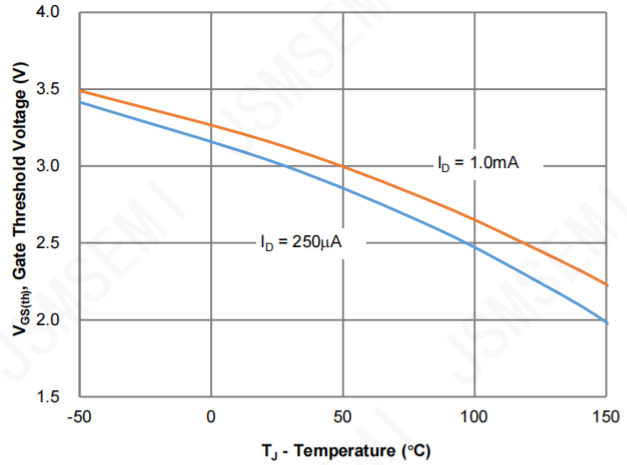


Figure 7: Gate Threshold Variation vs. Junction Temperature

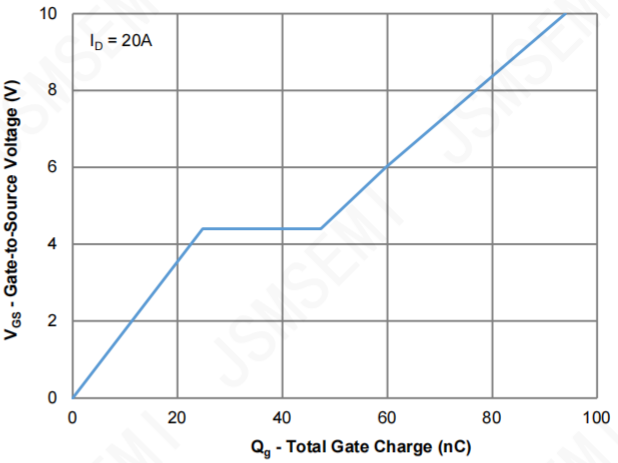


Figure 8: Gate Charge Characteristics

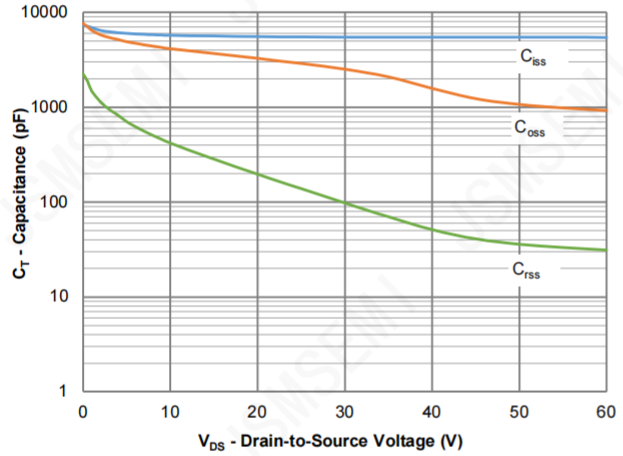


Figure 9: Capacitance Characteristics

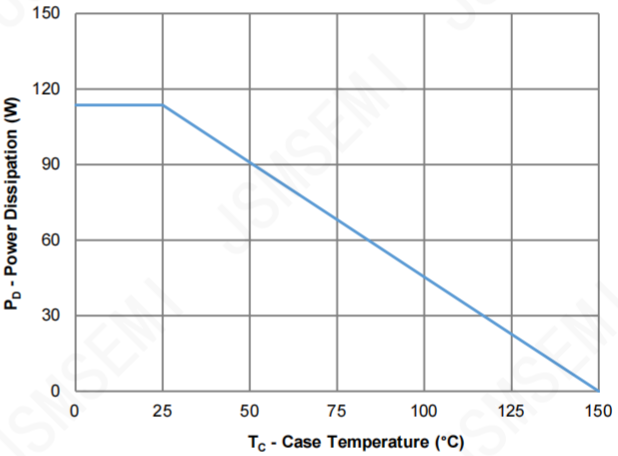


Figure 10: Power Derating

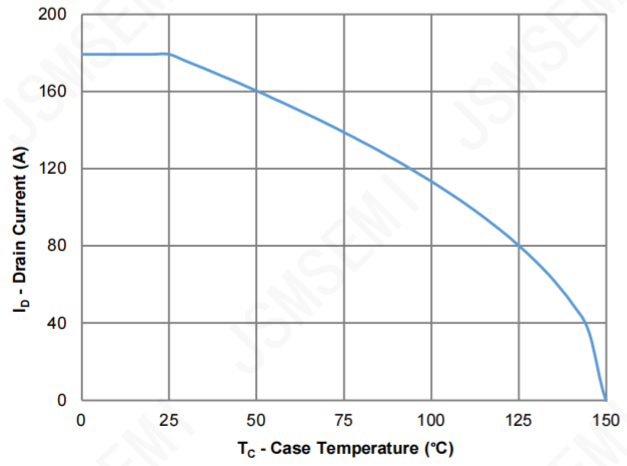


Figure 11: Current Derating

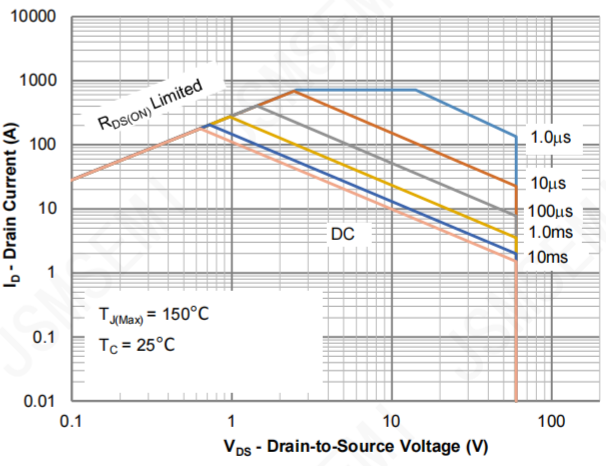


Figure 12: Safe Operating Area

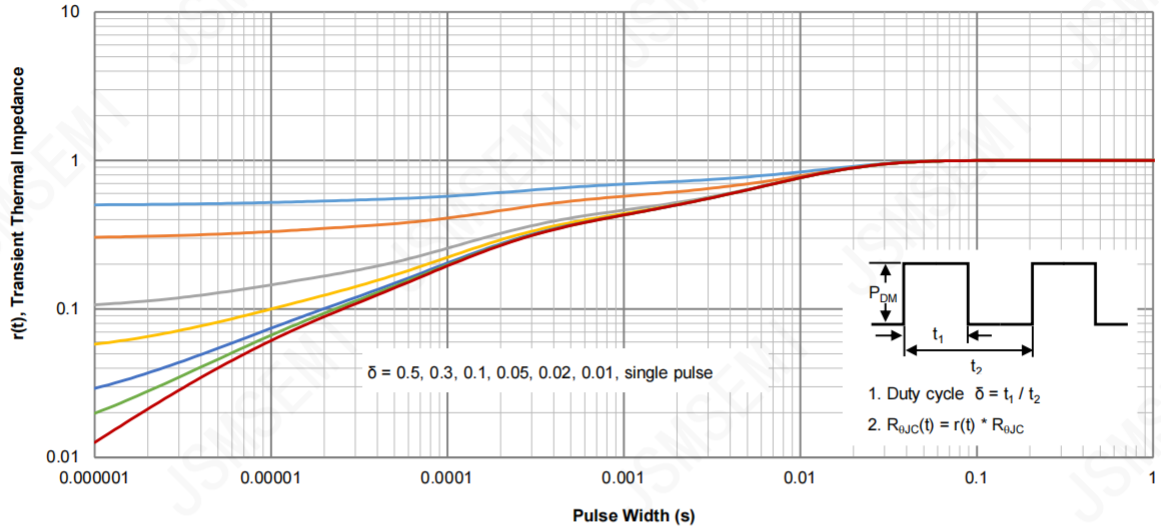
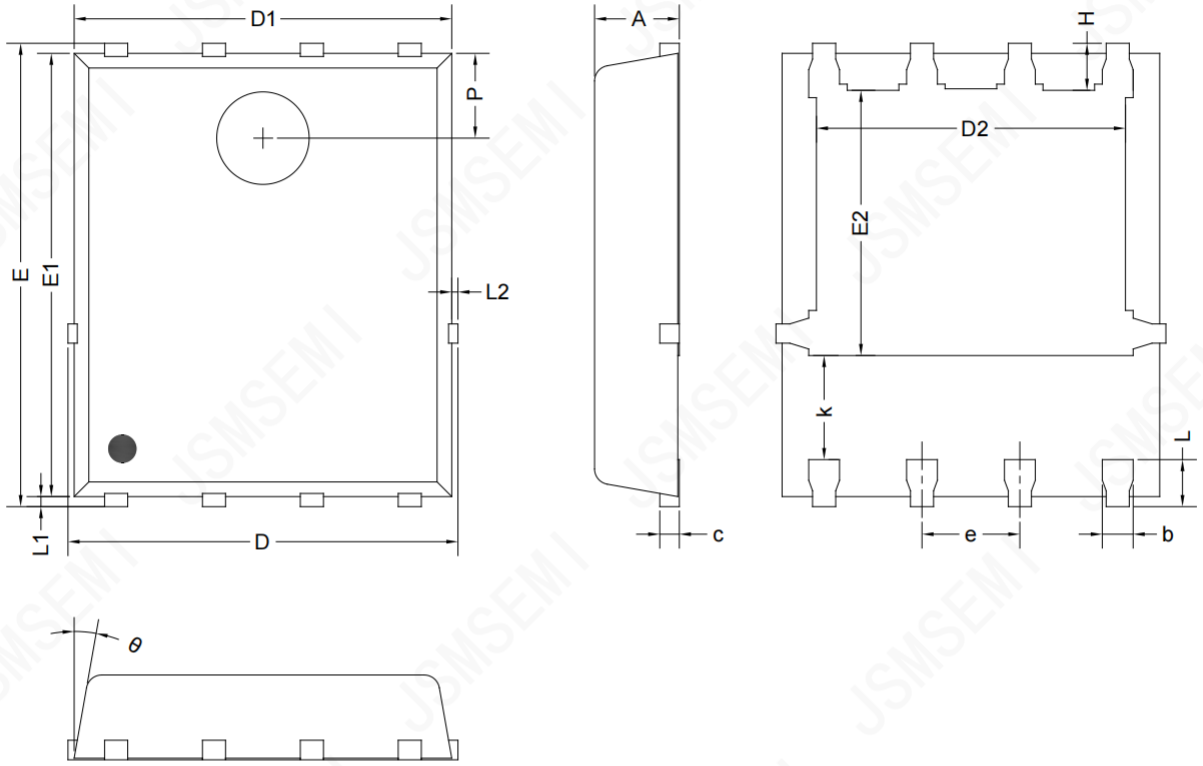


Figure 13: Normalized Maximum Transient Thermal Impedance

Package Information

DFN5060-8L



Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.000	1.100	1.200
b	0.350	0.400	0.450
c	0.210	0.250	0.340
D	4.800	-	5.100
D1	4.800	4.900	5.000
D2	3.910	4.010	4.110
E	5.900	6.000	6.100
E1	5.700	5.750	5.800
E2	3.340	3.440	3.540
e	1.270 BSC		
H	0.510	0.610	0.710
k	1.100	-	-
L	0.510	0.610	0.710
L1	0.060	0.130	0.200
L2	-	-	0.100
P	1.000	1.100	1.200
θ	8°	10°	12°

NOTE: This drawing is subject to change without notice.

Revision History

Rev.	Change	Date
V1.0	Initial version	6/27/2021

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