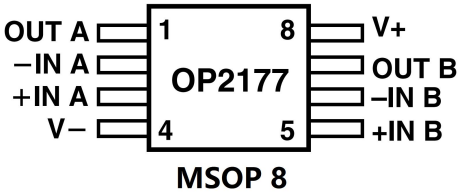
Features

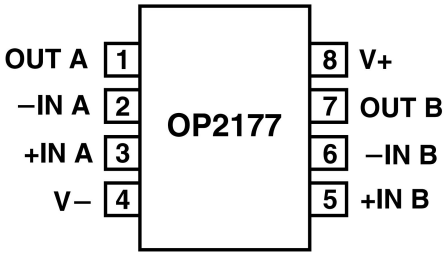
- Inputs Internally Protected Beyond Supply Voltage
- Very Low Offset Voltage Drift:0.7 uV/C Max
- Dual Supply Operation:±5V to ±15V
- Low Input Bias Current:2 nA Max
- Low Noise:8 nV/Hz
- Low Supply Current:400 LA/Amp



MSOP 8

Applications

- Instrumentation
- Sensors and Controls
- Precision Filters



SOIC 8

OP2177

Absolute Maximum Ratings*

Supply Voltage..... 36 V

Input Voltage .....VS– to VS+

Differential Input Voltage .....±Supply Voltage

Storage Temperature Range

R, RM, and RU Packages..... –65°C to +150°C

Operating Temperature Range

OP2177.....–40°C to +125°C

Junction Temperature Range

Packages..... –65°C to +150°C

Lead Temperature Range (Soldering, 10 sec) .....300°C

*Stresses above those listed under Absolute Maximum Ratings may cause perma-nent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating condi-tions for extended periods may affect device reliability.

Package Type	θJA	θJC	Unit
MSOP-8	190	44	℃/W
SOIC-8	158	44	℃/W

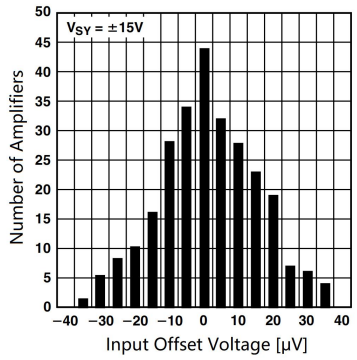
Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ*	Max	Unit
Input Characteristics						
Offset Voltage	V_{OS}	-40℃＜T_A＜125℃	-	25	100	μV
Input Bias Current	I_B	-40℃＜T_A＜125℃	-2	0.5	2	nA
Input Offset Current	I_{OS}	-40℃＜T_A＜125℃	-1	0.2	1	
Input Voltage Range		.	-3.5	-	3.5	V
Common-mode Rejection Ratio	CMRR	V_{CM}=-3.5V to 3.5V -40℃＜T_A＜125℃	120 118	126 125	-	dB
Large Signal Voltage Gain	A_{VO}	R_L=2kΩ，V_O=-3.5V to 3.5V	1000	2000	-	V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	-40℃＜T_A＜125℃	-	0.2	0.7	μV/℃
Output Characteristics						
Output Voltage High	V_{OH}	I_L=1mA，-40℃＜T_A＜125℃	4	4.1	-	V
Output Voltage Low	V_{OL}	I_L=1mA，-40℃＜T_A＜125℃	-	-4.1	-4	V
Output Current	I_{OUT}	$V_{DROPOUT}$	-	±10	-	mA
Power Supply						
Power Supply Rejection Ration	PSRR	V_S=±2.5V to ±15V -40℃＜T_A＜125℃	118 114	121 120	-	dB
Supply Current/Amplifier	I_{SY}	V_O=0V -40℃＜T_A＜125℃	-	400 500	500 600	μA
Dynamic Performance						
Slew Rate	S_R	R_L=2kΩ	-	0.7	-	V/μS
Gain Bandwidth Product	GBP		-	1.3	-	MHz
Noise Performance						
Voltage Noise	e_n p-p	0.1Hz to 10 Hz	-	0.4	-	μV p-p
Voltage Noise Density	e_n	f=1KHz	-	7.9	8.5	nV/√Hz
Current Noise Density	i_n	f=1KHz	-	0.2	-	nV/√Hz
Multiple Amplifiers Channel Separation	CS	DC f=100KHz	-	0.01 -120	-	μV/V dB

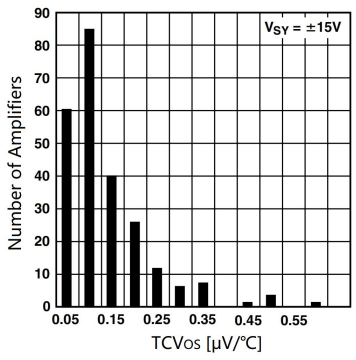
*Typical values cover all parts within one standard deviation of the average value. Average values, given in many competitors ' data sheets as "typical," give unrealistically low estimates for parameters that can have both positive and negative values.

Typical Characteristics

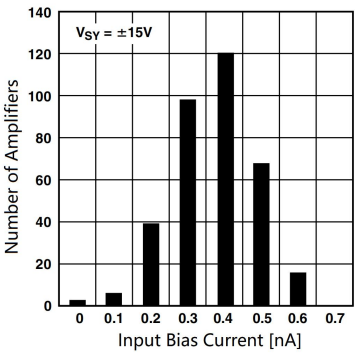
Input Offset Voltage Distribution



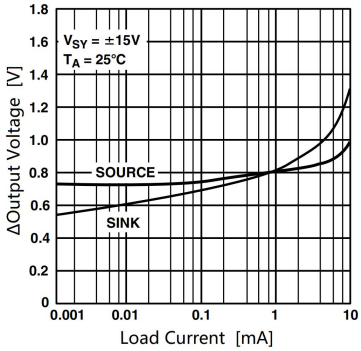
Input Offset Voltage Distribution



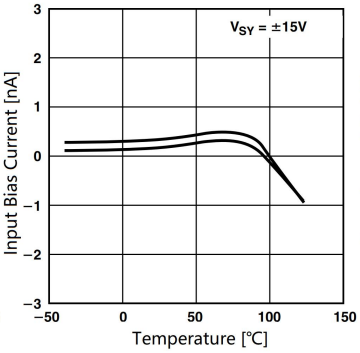
Input Offset Voltage Distribution



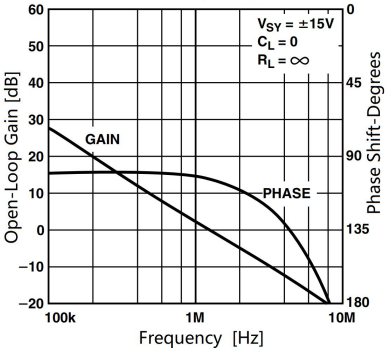
Output Voltage to Supply Rail vs. Load Current



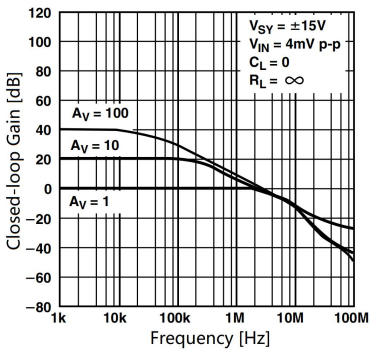
Input Bias Current vs. Temperature



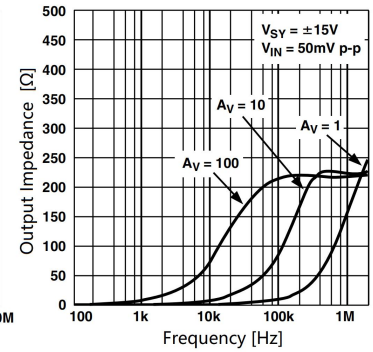
Open-loop Gain and Phase Shift vs. Frequency



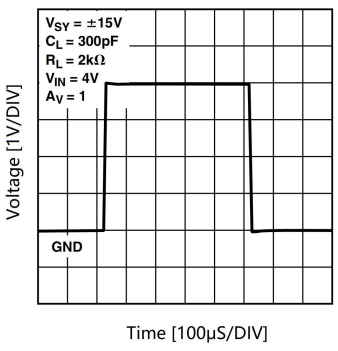
Closed-loop Gain vs. Frequency



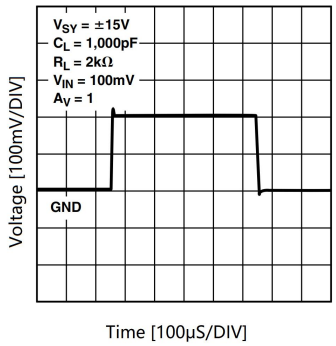
Output Inpedance vs. Frequency



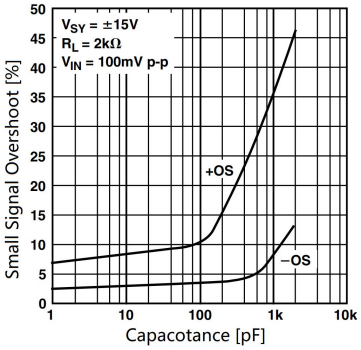
Large Signal Transient Response



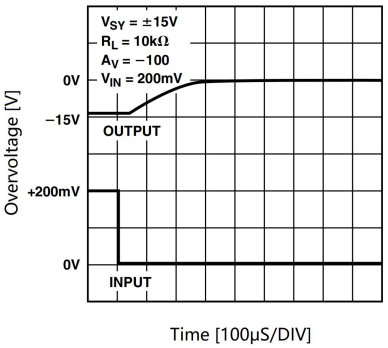
Small Signal Transient Response



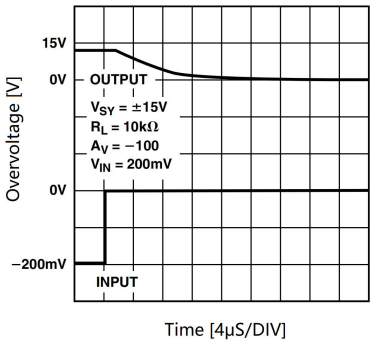
Small Signal Overshoot vs. Load Capacitance



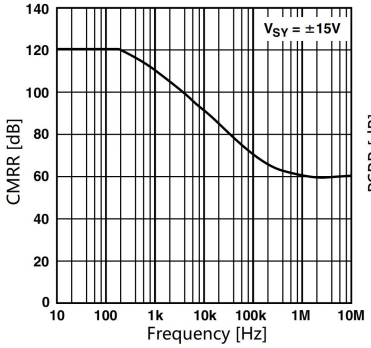
Positive Overvoltage Recovery



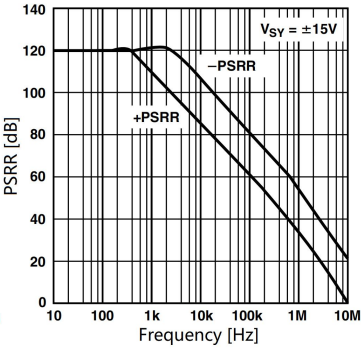
Negative Overvoltage Recovery



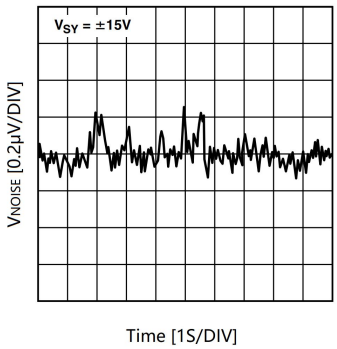
CMRR vs. Frequency



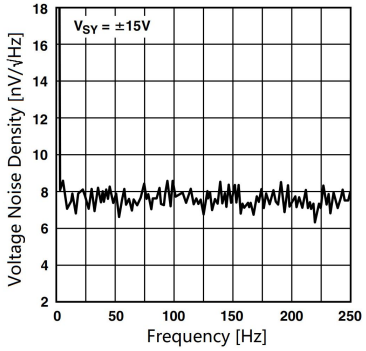
PSRR vs. Frequency



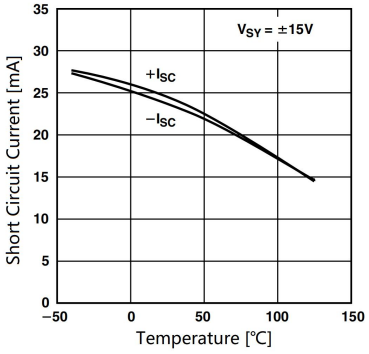
0.1Hz to 10Hz Input Voltage Noise



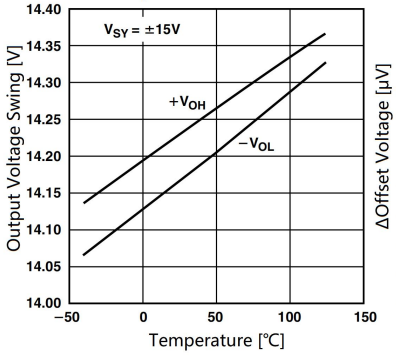
Voltage Noise Density



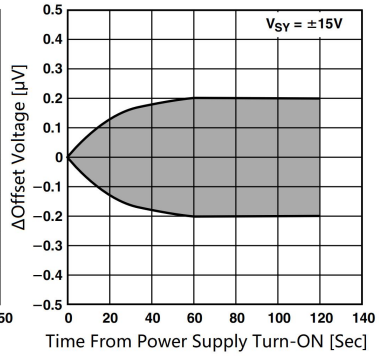
Short Circuit Current vs. Temperature



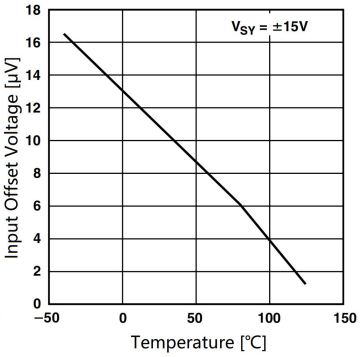
Output Voltage Swing vs. Temperature



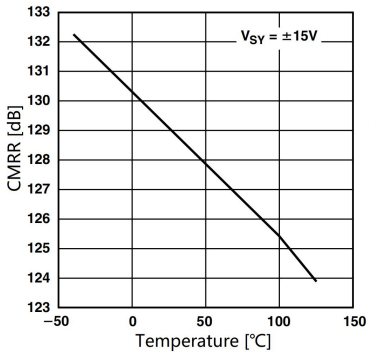
Warm-Up Drift



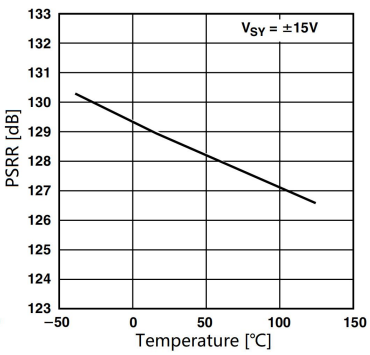
|Offset Voltage| vs. Temperature



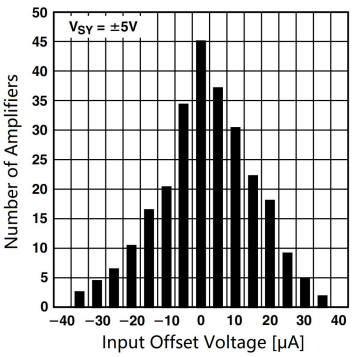
CMRR vs. Temperature



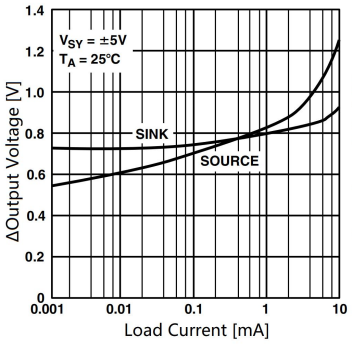
PSRR vs. Temperature



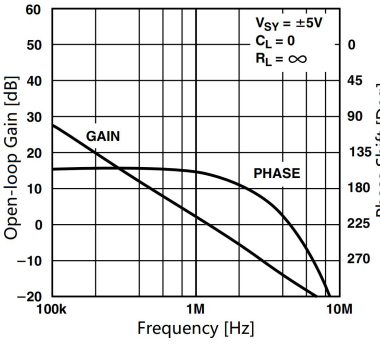
Input Offset Voltage Distribution



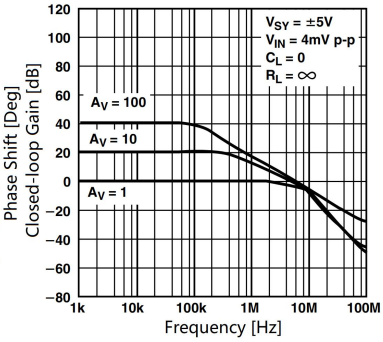
Output Voltage to Supply Rail vs. Load Current



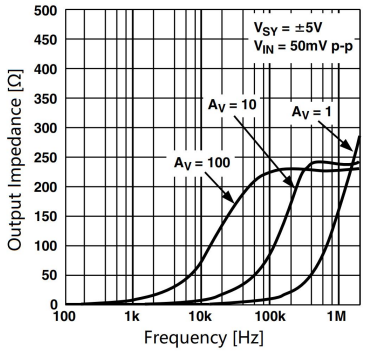
Open-loop Gain and Phase Shift vs. Frequency



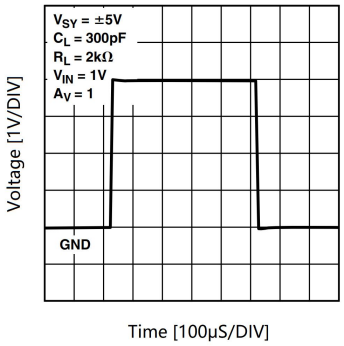
Closed-loop Gain vs. Frequency



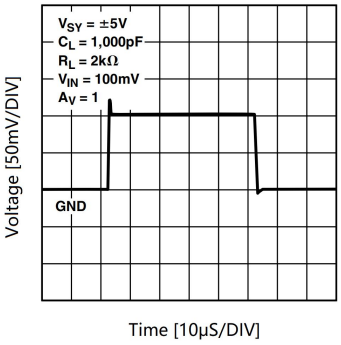
Output Impedance vs. Frequency



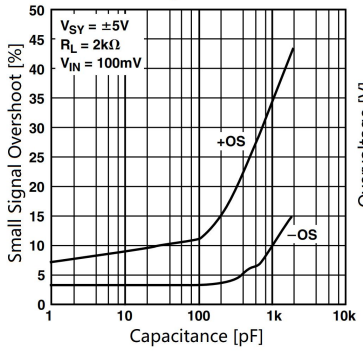
Large Signal Transient Response



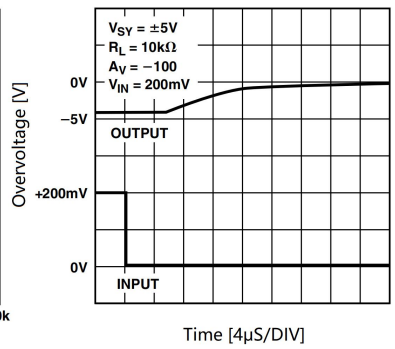
Small Signal Transient Response



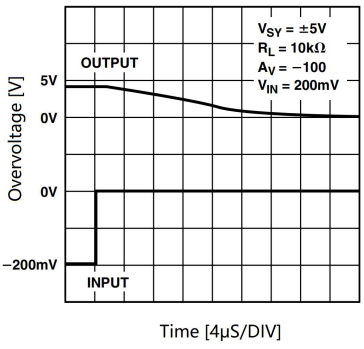
Small Signal Overshoot vs. Load Capacitance



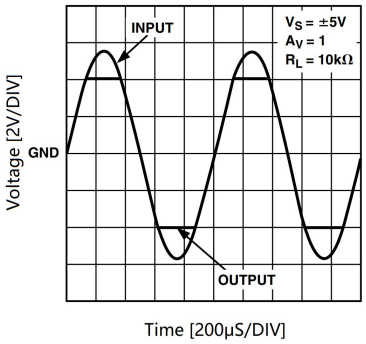
Positive Overvoltage Recovery



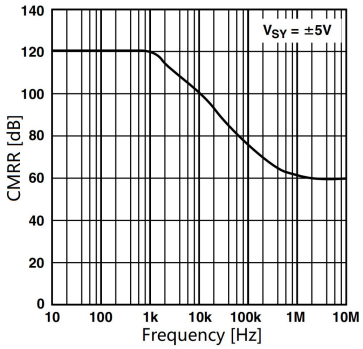
Negative Overvoltage Recovery



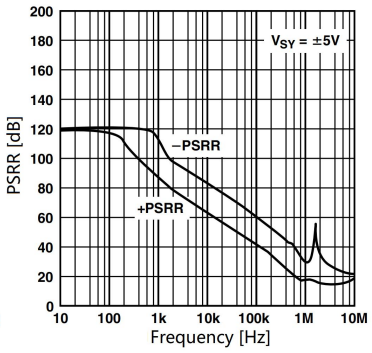
No Phase Reversal



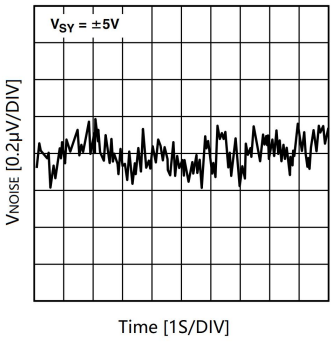
CMRR vs. Frequency



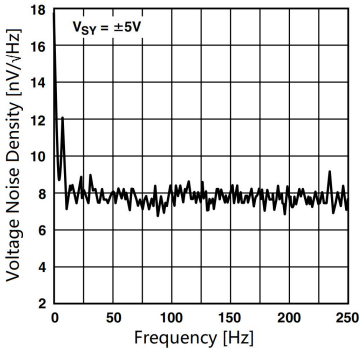
PSRR vs. Frequemcy



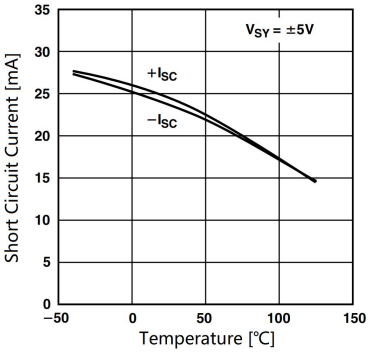
0.1 Hz to 10 Hz Input Voltage Noise



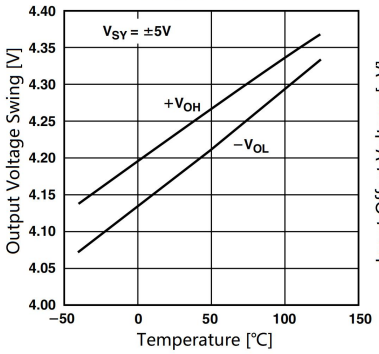
Voltage Noise Density



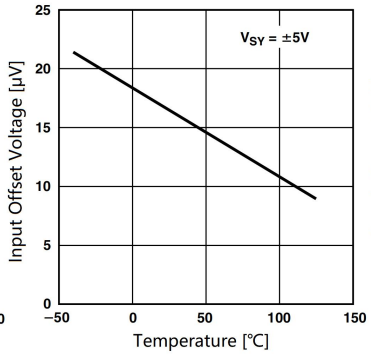
Short Circuit Current vs. Temperayure



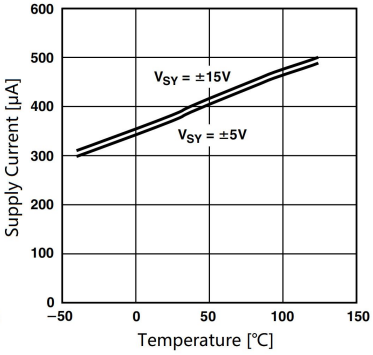
Output Voltage Swing vs. Temperature



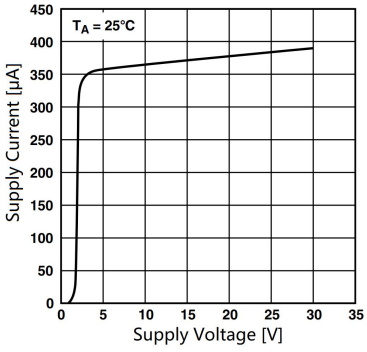
|Offset Voltage| vs. Temperature



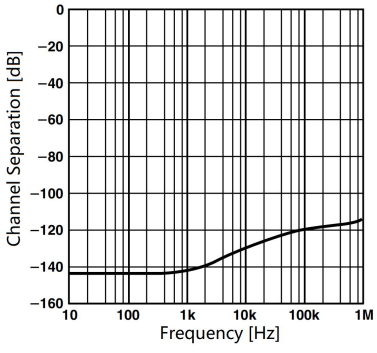
Supply Current vs. Temperature



Supply Current vs. Supply Voltage



Channel Separation vs. Frequency



Total Noise Including Source Resistors

The low input current noise and input bias current of the OP2177 make it useful for circuits with substantial input source resistance.Input offset voltage increases by less than 1 μV max per 500 Ω of source resistance.The total noise density of the OP2177 is:

$$e_{n,\,TOTAL} = \sqrt{e_n^{\,2} + \left(i_n R_S\right)^2 + 4kTR_S}$$

Where e_n is the input voltage noise density

$\mathbf{i}_n$ is the input current noise density

$\mathbf{R}_S$ is the source resistance at the noninverting terminal

k is Boltzman's constant (1.38 *10^{-23} J/K)

T is the ambient temperature in Kelvin (T = 273 + °C)

For R_S < 3.9 kΩ, $\mathbf{e}_n$ dominates and

$$e_{n,\,TOTAL} \approx e_n$$

The total equivalent rms noise over a specific bandwidth is expressed as:

$$E_n = \left(e_{n,\,TOTAL}\right)\sqrt{BW}$$

Where **BW** is the bandwidth in Hertz.

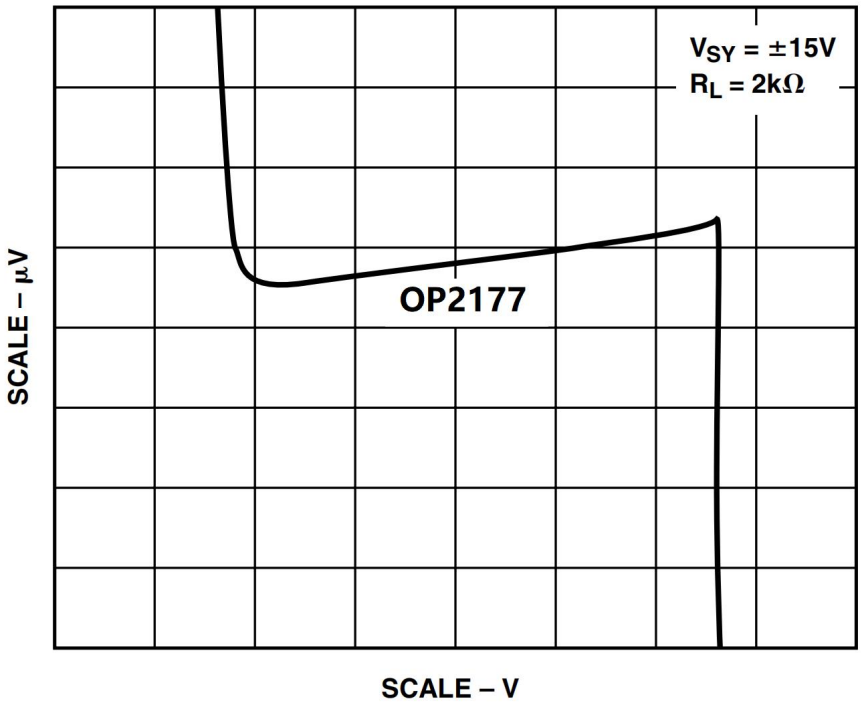
Note: The above analysis is valid for frequencies larger than 50 Hz. When considering lower frequencies, flicker noise (also known as 1/f noise) must be taken into account. For a reference on noise calculations refer to Band pass KRC or Sallen-Key Filter section

Gain Linearity

Gain linearity reduces errors in closed-loop configurations. The straighter the gain curve, the lower the maximum error over the input signal range will be. This is especially true for circuits with high closed-loop gains.The OP2177 has

excellent gain linearity even with heavy loads,shown in Figure 1.conditions with RL = 2 kΩ. The OP2177 (dual) has virtually no distortion at lower voltages.

Figure 1



Input Overvoltage Protection

When their input voltage exceeds the positive or negative supply voltage, most amplifiers require external resistors to protect them from damage.

The OP2177 has internal protective circuitry that allows voltages as high as 2.5 V beyond the supplies to be applied at the input of either terminal without any harmful effects.

Use an additional resistor in series with the inputs if the voltage will exceed the supplies by more than 2.5 V. The value of the resistor can be determined from the formula:

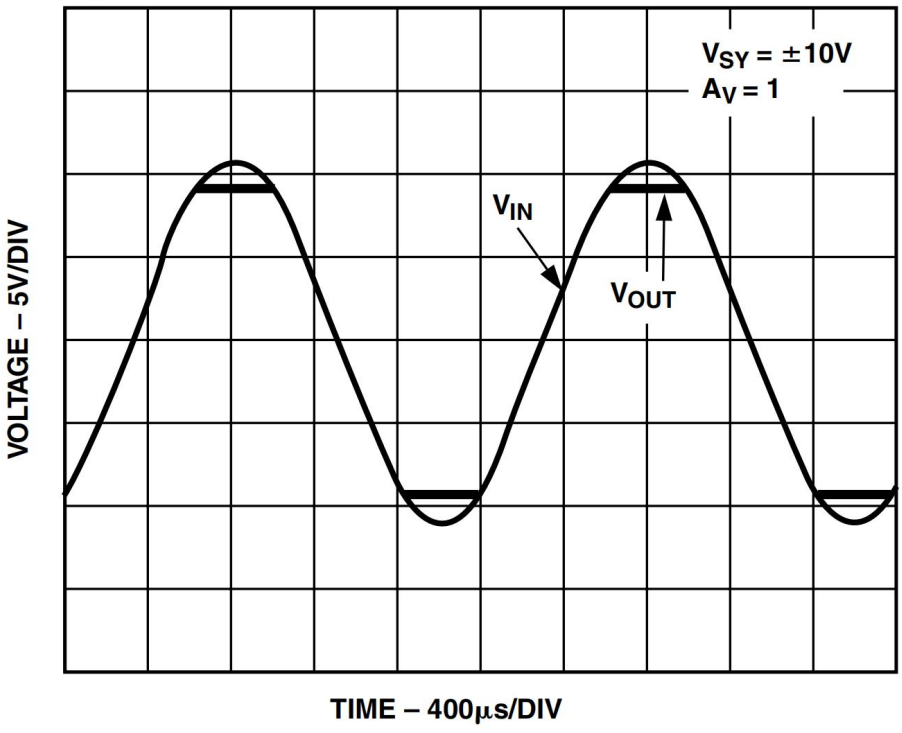
$$\frac{\left(V_{IN} - V_S\right)}{R_S + 500\ \Omega} \leq 5\ mA$$

With the OP2177's low input offset current of <1 nA max, placing a 5kΩ resistor in series with both inputs adds less than 5 μV to input offset voltage and has a negligible impact on the overall noise performance of the circuit.5kΩ will protect the inputs to more than 27 V beyond either supply.Refer to the THD + N section for additional information on noise versus source resistance.

Output Phase Reversal

Phase reversal is defined as a change of polarity in the amplifier transfer function. Many operational amplifiers exhibit phase reversal when the voltage applied to the input is greater than the maximum common-mode voltage. In some instances this can cause permanent damage to the amplifier. In feedback loops, it can result in system lockups or equipment damage. The OP2177 is immune to phase reversal problems even at input voltages beyond the supplies.

Figure 2



Settling Time

Settling time is defined as the time it takes an amplifier output to reach and remain within a percentage of its final value after application of an input pulse. It is especially important in measurement and control circuits where amplifiers buffer A/D inputs or DAC outputs.

To minimize settling time in amplifier circuits, use proper bypassing of power supplies and an appropriate choice of circuit components.Resistors should be metal film types as these have less stray capacitance and inductance than their wire-wound counterparts.Capacitors should be polystyrene or polycarbonate types to minimize dielectric absorption.

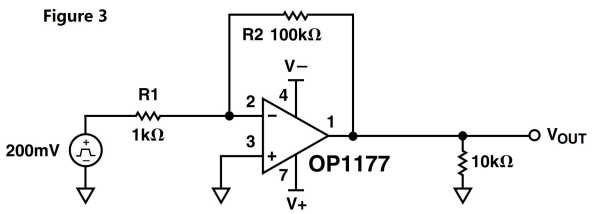
The leads from the power supply should be kept as short as possible to minimize capacitance and inductance. The OP2177 has a settling time of about 45 μs to 0.01% (1 mV) with a 10V step applied to the input in a noninverting unity gain.

Overload Recovery Time

Overload recovery is defined as the time it takes the output voltage of an amplifier to recover from a saturated condition to its linear response region. A common example is where the output voltage demanded by the circuit’ s transfer function lies beyond the maximum output voltage capability of the amplifier. A 10 V input applied to an amplifier in a closed-loop gain of 2 will demand an output voltage of 20 V. This is beyond the output voltage range of the OP2177 when operating at ±15 V supplies and will force the output into saturation.

Recovery time is important in many applications, particularly where the op amp must amplify small signals in the presence of large transient voltages.

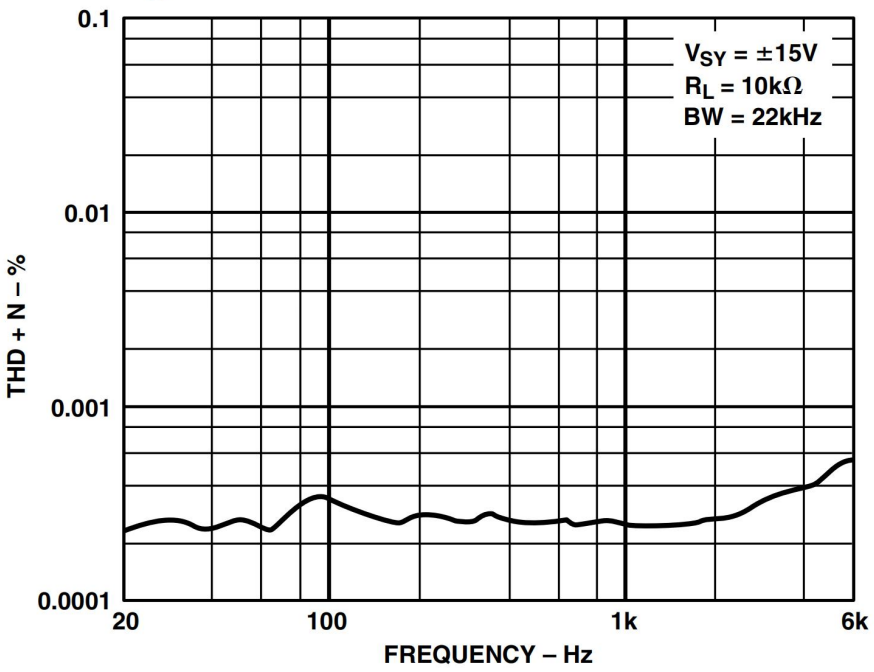
Figure 3



THD + Noise

The OP2177 has very low total harmonic distortion. This indicates excellent gain linearity and makes the OP2177 a great choice for high closed-loop gain precision circuits.Figure 4 shows that the OP2177 has approximately 0.00025% distortion in unity gain, the worst-case configuration for distortion.

Figure 4



Capacitive Load Drive

OP2177 is inherently stable at all gains and capable of driving large capacitive loads without oscillation. With no external compensation, the OP2177 will safely drive capacitive loads up to 1000 pF in any configuration. As with virtually any amplifier,driving larger capacitive loads in unity gain requires additional circuitry to assure stability.

In this case, a “snubber network” is used to prevent oscillation and reduce the amount of overshoot. A significant advantage of this method is that it does not reduce the output swing because the resistor RS is not inside the feedback loop.

Figure 5 is a scope photograph of the output of the OP2177 in response to a 400 mV pulse. The load capacitance is 2 nF. The circuit is configured in

positive unity gain, the worst-case condition for stability.

Placing an R-C network, as shown in Figure 6, parallel to the load capacitance CL will allow the amplifier to drive higher values of CL without causing oscillation or excessive overshoot.

There is no ringing and overshoot is reduced from 27% to 5%using the snubber network.

Optimum values for RS and CS are tabulated in Table I for several capacitive loads up to 200 nF. Values for other capacitive loads can be determined experimentally.

Figure 5

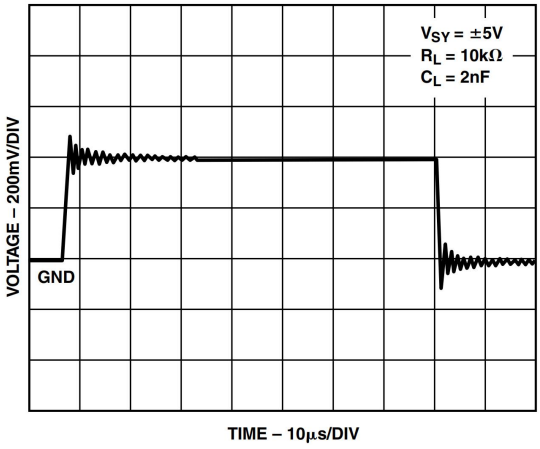


Figure 6

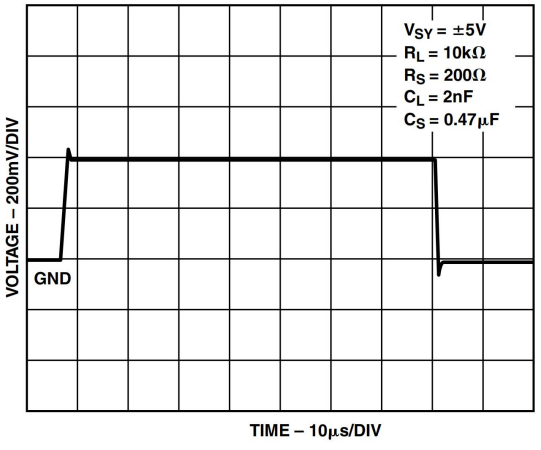
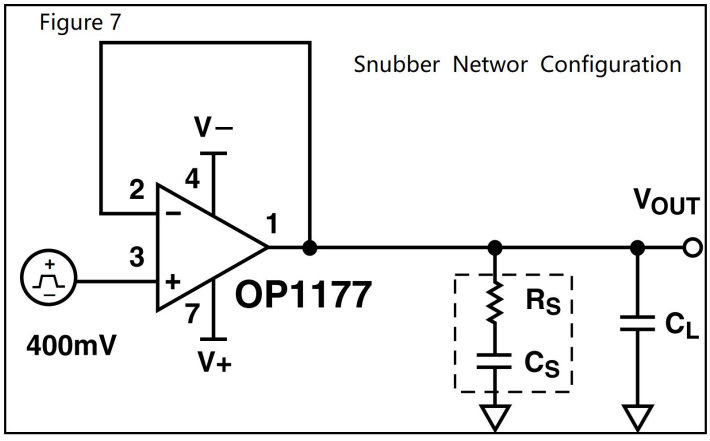


Table 1
Optimum Values for
Capacitive Loads

C_L (nF)	R_S (Ω)	C_S
10	20	0.33 µF
50	30	6.8 nF
200	200	0.47 µF

Figure 7



Caution: The snubber technique cannot recover the loss of bandwidth induced

by large capacitive loads.

Stray Input Capacitance Compensation

The effective input capacitance in an op amp circuit, Ct, consists of three components. These are: the internal differential capacitance between the input terminals, the internal common mode capacitance of each input to ground, and the external capacitance including parasitic capacitance. In the circuit of Figure 8, the closed-loop gain increases as the signal frequency increases.

The transfer function of the circuit is: indicating a zero at:

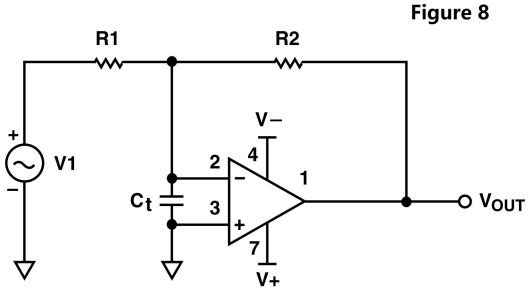
$$1+\frac{R2}{R1}\left(1+sC_tR1\right) \qquad s=\frac{R2+R1}{R2R1C_t}=\frac{1}{2\pi\left(R1//R2\right)C_t}$$

Depending on the value of R1 and R2, the cutoff frequency of the closed-loop gain may be well below the crossover frequency. In this case, the phase margin, Φm, can be severely degraded resulting in excessive ringing or even oscillation.

A simple way to overcome this problem is to insert a capacitor in the feedback path as shown in Figure 9.

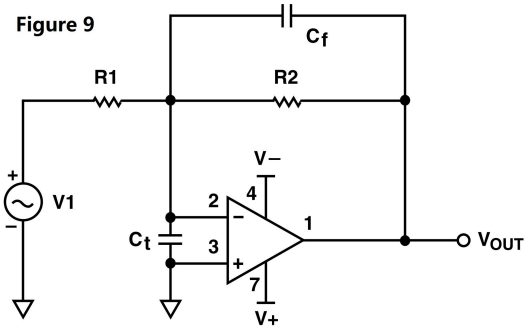
The resulting pole can be positioned to adjust the phase margin Setting Cf = (R1/R2)Ct, achieves a phase margin of 90°.

Figure 8



Stray Input Capacotance OP2177

Figure 9



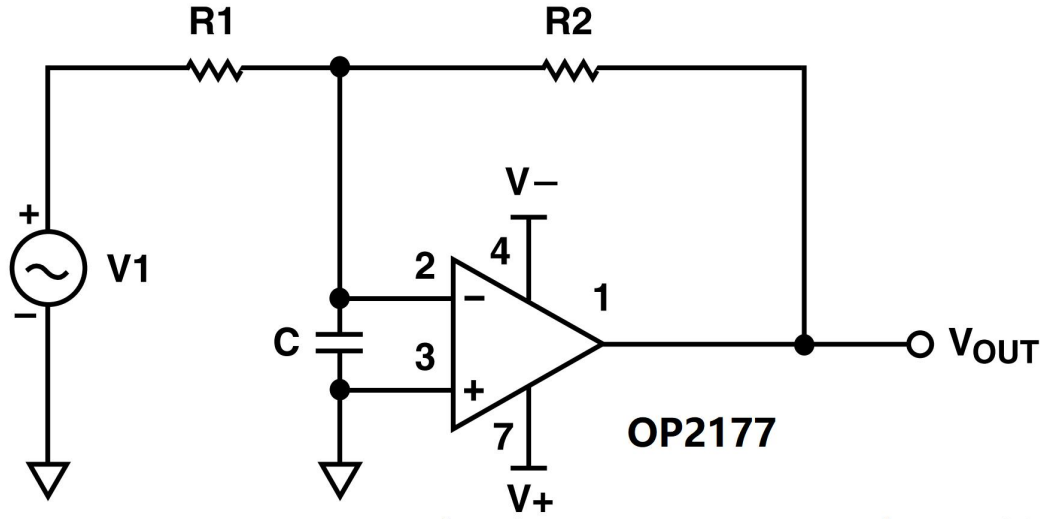
Compensation Using Feedback Capacitor OP2177

Reducing Electromagnetic Interference

A number of methods can be utilized to reduce the effects of EMI on amplifier circuits.

In one method, stray signals on either input are coupled to the opposite input of the amplifier. The result is that the signal is rejected according to the amplifier's CMRR.

This is usually achieved by inserting a capacitor between the inputs of the amplifier as shown in Figure 10. However, this method may also cause instability depending on the value of capacitance.



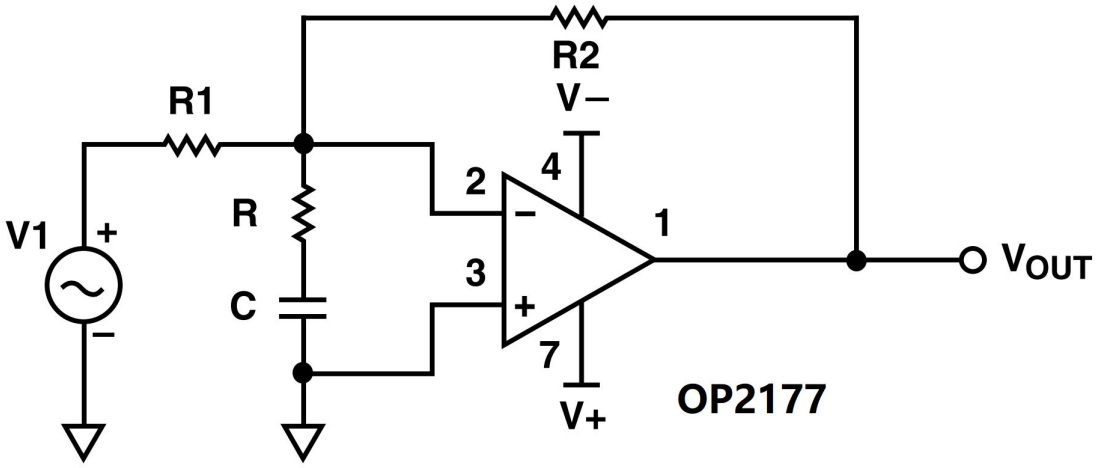
EMI Reduction Figure 10

Placing a resistor in series with the capacitor (Figure 11) increases the dc loop gain and reduces the output error. Positioning the breakpoint (introduced by R-C) below the secondary pole of the op amp improves the phase margin and hence stability.R can be chosen independently of C for a specific phase margin according to the formula.

$$R = \frac{R2}{ajf_2} - \left(1 + \frac{R2}{R1}\right)$$

where a is the open-loop gain of the amplifier and f2 is the frequency at which

the phase of a = Φm – 180°.



Compensation Using Input RC Network **Figure 11**

Proper Board Layout

The OP2177 is a high-precision device. In order to ensure optimum performance at the PC board level, care must be taken in the design of the board layout.

To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

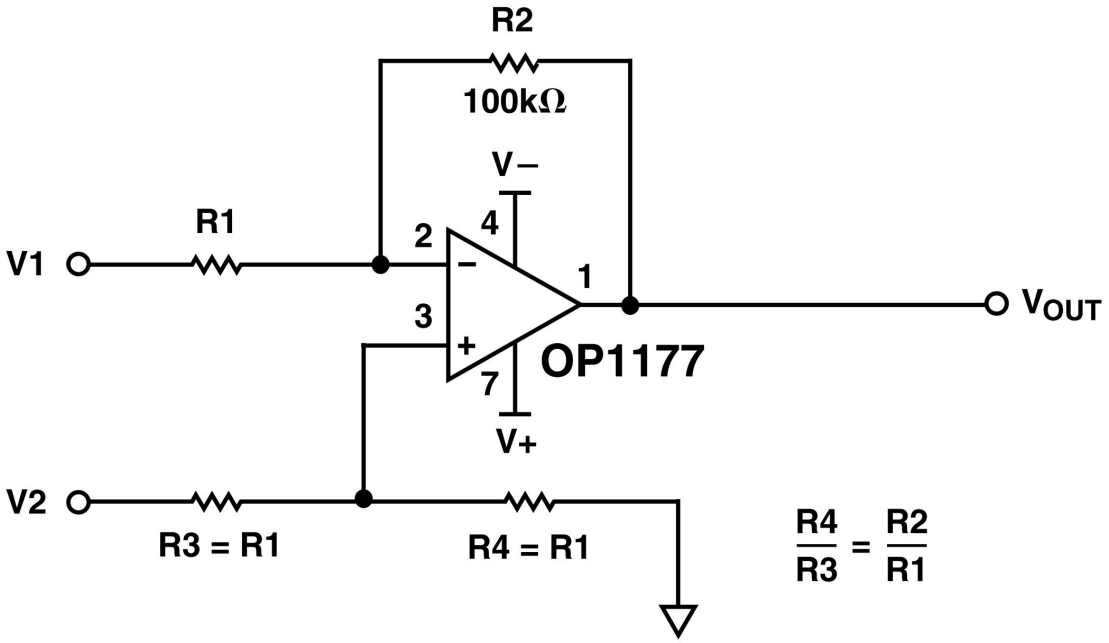
Keeping supply traces short and properly bypassing the power supplies will minimize power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as pos-sible to the device supply pins. Stray capacitances are a concern at the output and the inputs of the amplifier. It is recommended that signal traces be kept at least 5 mm from supply lines to minimize coupling.

A variation in temperature across the PC board can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, resistors should be oriented so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components where possible in order to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Leads should be of equal length so that ther-mal conduction is in equilibrium. Heat sources on the PC board should be kept as far away from

amplifier input circuitry as practical.
The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

Difference Amplifiers

Difference amplifiers are used in high-accuracy circuits to improve the common-mode rejection ratio (CMRR).



Difference Amplifier **Figure 12**

In the single amplifier instrumentation amplifier (circuit of Figure 12), where:

$$\frac{R4}{R3} = \frac{R2}{R1} \qquad V_O = \frac{R2}{R1}\left(V_2 - V_1\right)$$

a mismatch between the ratio **R2/R1** and **R4/R3** will cause the common-mode rejection ratio to be reduced. To better understand this effect, consider the following: By definition:

$$CMRR = \frac{A_{DM}}{A_{CM}}$$

where A_{DM} is the differential gain and A_{CM} is the common-mode gain.

$$A_{DM} = \frac{V_O}{V_{DIFF}} \text{ and } A_{CM} = \frac{V_O}{V_{CM}}$$

$$V_{DIFF} = V_1 - V_2 \text{ and } V_{CM} = \frac{1}{2}(V_1 + V_2)$$

In order for this circuit to act as a difference amplifier, its output must be proportional to the differential input signal. From Figure 12.

$$V_O = -\left(\frac{R2}{R1}\right)V_1 + \left[\frac{\left(1+\frac{R2}{R1}\right)}{\left(1+\frac{R3}{R4}\right)}\right]V_2$$

Arranging terms and combining the equations above yields:

$$CMRR = \frac{R4R1 + R3R2 + 2R4R2}{2R4R1 - 2R2R3} \quad (1)$$

The sensitivity of CMRR with respect to the R1 is obtained by taking the derivative of CMRR, in Equation 1, with respect to R1.

$$\frac{\delta CMRR}{\delta R1} = \frac{\delta}{\delta R1}\left(\frac{R1R4}{2R1R4 - 2R2R3} + \frac{2R2R4 + R2R3}{2R1R4 - 2R2R3}\right)$$

$$\frac{\delta CMRR}{\delta R1} = \frac{1}{2 - \frac{(2R2R3)}{R1R4}}$$

Assuming that: R1≈R2≈R3≈R4≈R and R(1 – δ) < R1, R2, R3, R4 < R(1 + δ). The worst-case CMRR error arises when: R1 = R4 = R(1 + δ) and R2 = R3 = R(1 – δ). Plugging these values into Equation 1 yields:

$$CMRR_{MIN} \cong \left|\frac{1}{2\delta}\right|$$

where δ is the tolerance of the resistors.
Lower tolerance value resistors result in higher common-mode rejection (up to the CMRR of the op amp).

Using 5% tolerance resistors, the highest CMRR that can be guaranteed is 20 dB. On the other hand, using 0.1% tolerance resistors would result in a common-mode rejection ratio of at least 54 dB (assuming that the op amp CMRR 54 dB).

With the CMRR of OP2177 at 120 dB minimum, the resistor match will be the limiting factor in most circuits. A trimming resistor can be used to further improve resistor matching and CMRR of the difference amp circuit.

A High-Accuracy Thermocouple Amplifier

A thermocouple consists of two dissimilar metal wires placed in contact. The dissimilar metals produce a voltage

$$V_{TC} = \alpha\left(T_J - T_R\right)$$

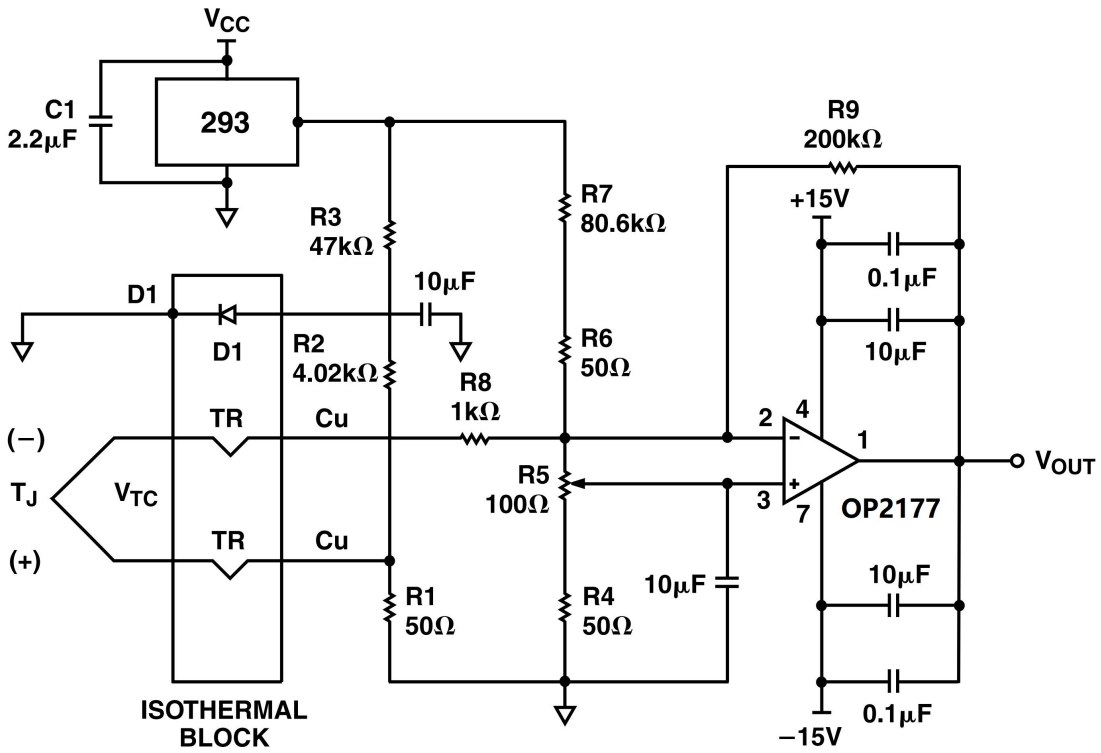
where T_J is the temperature at the measurement of the hot junction,TR is the one at the cold junction, and is the Seebeck coefficient specific to the dissimilar metals used in the thermocouple. V_{TC} is the thermocouple voltage. V_{TC} becomes larger with increasing temperature.

Maximum measurement accuracy requires cold junction compen-sation of the thermocouple as described below.

To perform the cold junction compensation, apply a copper wire short across the terminating junctions (inside the isothermal block) simulating a 0°C point. Adjust the output voltage to zero using the trimming resistor R5 and then remove the copper wire.

The OP2177 is an ideal amplifier for thermocouple circuits since it has a very low offset voltage, excellent PSSR and CMRR, and low noise at low frequencies.

It can be used to create a thermocouple circuit with great linearity. Resistors R1 and R2 and diode D1 shown in Figure 14 are mounted in an isothermal block.



Type K Thermocouple Amplifier Circuit **Figure 13**

Low Power Linearized RTD

A common application for a single element varying bridge is an RTD thermometer amplifier as shown in Figure 15. The excitation is delivered to the bridge by a 2.5 V reference applied at the top of the bridge.

RTDs may have thermal resistance as high as 0.5°C to 0.8°C per mW. In order to minimize errors due to resistor drift, the current through each leg of the bridge must be kept low. In this circuit, the amplifier supply current flows through the bridge.

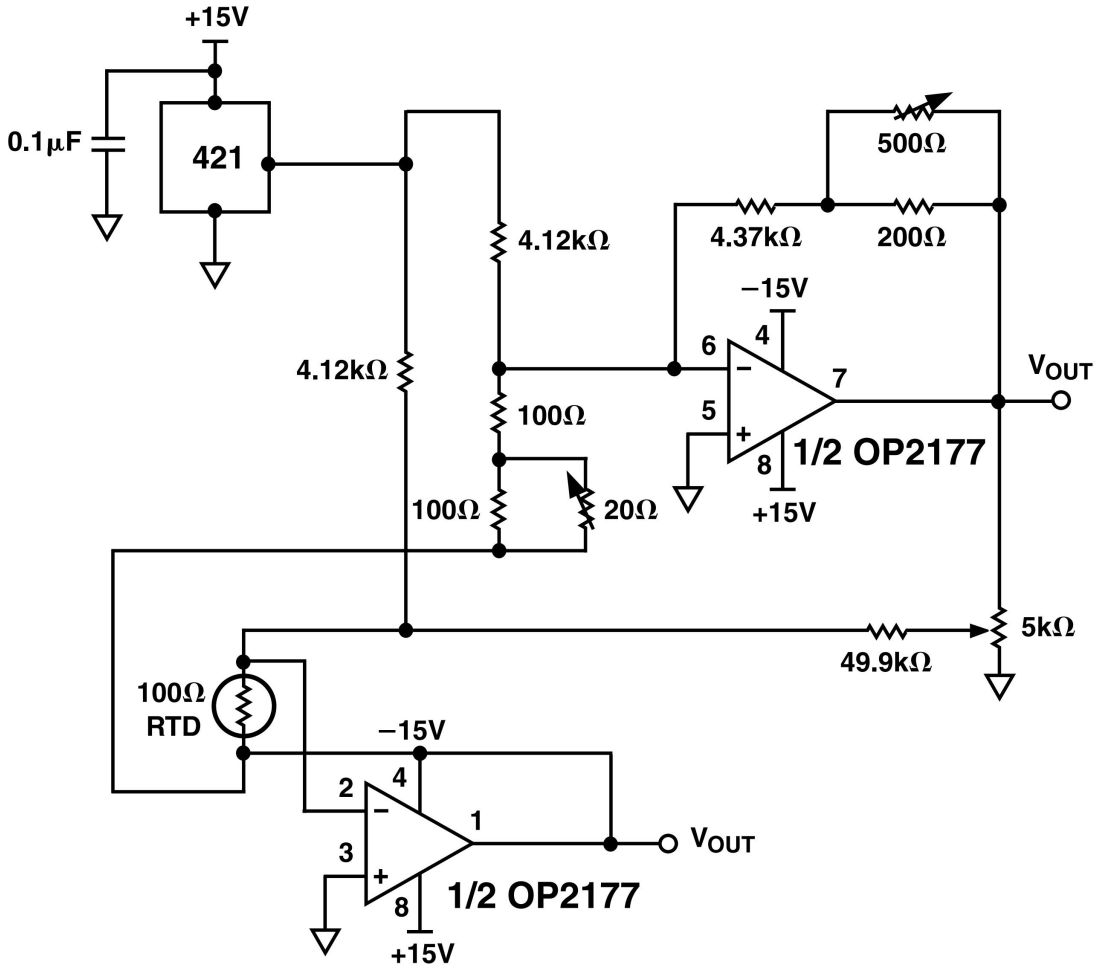
However, at the OP2177 maximum supply current of 600 µA, the RTD dissipates less than 0.1 mW of power even at the highest resistance. Errors due to power dissipation in the bridge are kept under 0.1°C.

Calibration of the bridge can be made at the minimum value of temperature to be measured by adjusting RP until the output is zero.

To calibrate the output span, set the full-scale and linearity pots to midpoint and apply a 500°C temperature to the sensor or substitute the equivalent 500°C RTD resistance.

Adjust the full-scale pot for a 5 V output. Finally, apply 250°C or the equivalent RTD resistance and adjust the linearity pot for 2.5 V output.

The circuit achieves better than ±0.5°C accuracy after adjustment.



Low Power Linearized RTD Circuit **Figure 14**

Single Op Amp Bridge

The low input offset voltage drift of the OP2177 makes it very effective for bridge amplifier circuits used in RTD signal condi-tioning. It is often more economical to use a single bridge op amp as opposed to an instrumentation amplifier.

In the circuit of Figure 16, the output voltage at the op amp is:

$$V_O = \frac{R2}{R}\left[V_{REF}\left(\frac{\delta}{\frac{R1}{R}+\left(1+\frac{R1}{R2}\right)(1+\delta)}\right)\right]$$

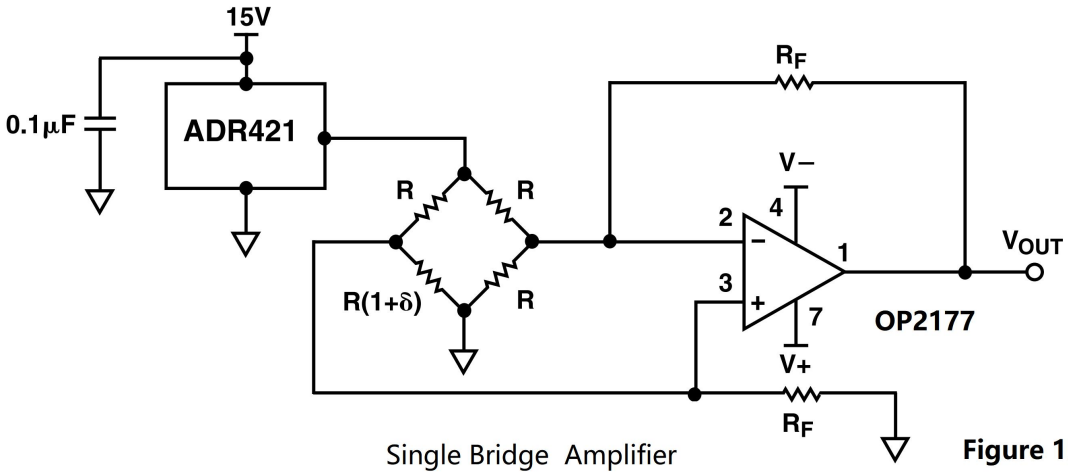
where δ = ΔR/R is the fractional deviation of the RTD resistance with respect to the bridge resistance due to the change in temperature at the RTD.

For δ << 1, the expression above becomes:

$$V_O \cong \left(\frac{R2}{R}\right)V_{REF}\left(\frac{\delta}{1+\frac{R1}{R}+\frac{R1}{R2}}\right)=\left[\left(\frac{R2}{R}\right)\left(1+\frac{R1}{R2}\right)+\left(\frac{R1}{R2}\right)\right]V_{REF}\,\delta$$

With VREF constant, the output voltage is linearly proportional to δ with a gain factor of:

$$V_{REF}\left(\frac{R2}{R}\right)\left[\left(1+\frac{R1}{R2}\right)+\left(\frac{R1}{R2}\right)\right]$$



Single Bridge Amplifier

Figure 15

Bandpass KRC or Sallen-Key Filter

The low offset voltage and the high CMRR of the OP2177 make it an excellent choice for precision filters such as the KRC filter shown in Figure 16. This filter type offers the capability to tune the gain and the cutoff frequency independently.

Since the common-mode voltage into the amplifier varies with the input signal in the KRC filter circuit, a high CMRR is required to minimize distortion. Also, the low offset voltage of the OP2177 allows a wider dynamic range when the circuit gain is chosen to be high.

The circuit of Figure 17 consists of two stages. The first stage is a simple high-pass filter whose corner frequency f_C is:

$$\frac{1}{2\pi\sqrt{C1C2R1R2}}$$ and whose $$Q = K\sqrt{\frac{R1}{R2}}$$

where K is the dc gain.
Choosing equal capacitor values minimizes the sensitivity and simplifies Equation 2 to:

$$\frac{1}{2\pi C\sqrt{R1R2}}$$

The value of Q determines the peaking of the gain versus frequency (ringing in transient response). Commonly chosen values for Q are generally near unity.

Setting $$Q = \frac{1}{\sqrt{2}}$$

yields minimum gain peaking and minimum ringing.Determine values for R1 and R2 by use of Equation 3.

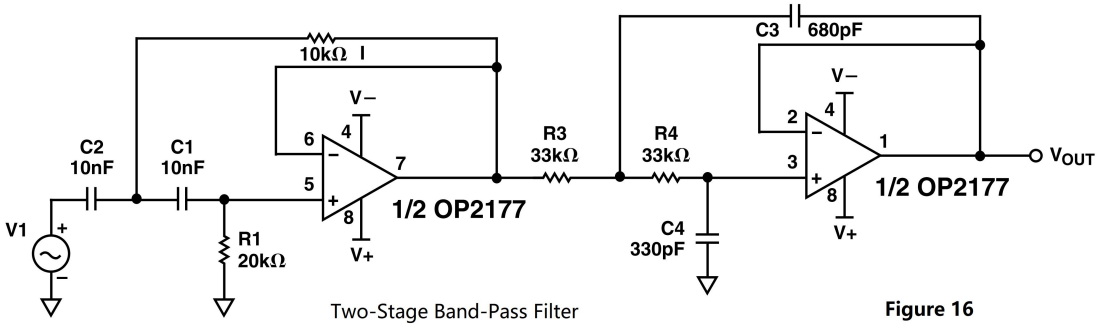
For $Q = 1/\sqrt{2}$, R1/R2 = 2 in the circuit example. Pick R1 = 5 kΩ and R2 = 10 kΩ for simplicity.

The second stage is a low-pass filter whose corner frequency can be determined in a similar fashion. For R3 = R4 = R.

$$f_C = \frac{1}{2\pi R\sqrt{\frac{C3}{C4}}} \text{ and } Q = \frac{1}{2}\sqrt{\frac{C3}{C4}}$$

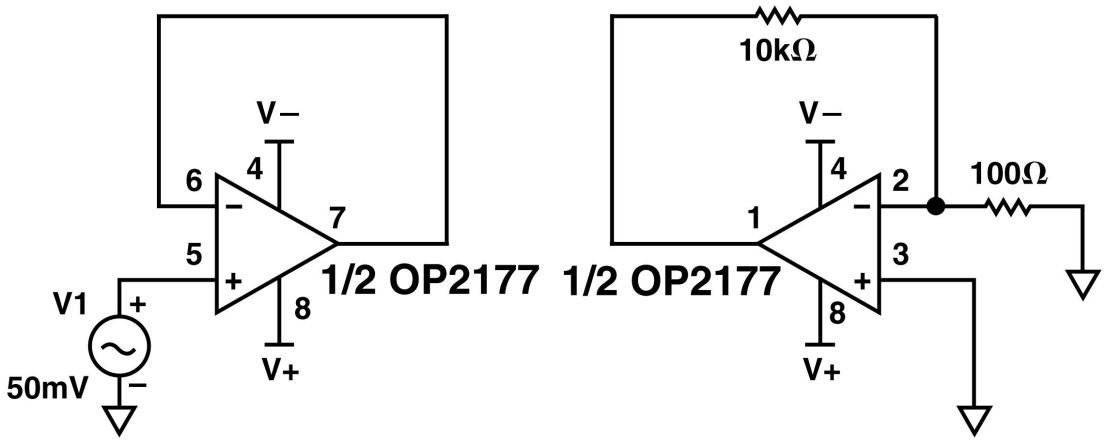
Channel Separation

Multiple amplifiers on a single die are often required to reject any signals originating from the inputs or outputs of adjacent channels. OP2177 input and bias circuitry is designed to prevent feedthrough of signals from one amplifier channel to the other. As a result the OP2177 has an impressive channel separation of greater than –120 dB for frequencies up to 100 kHz and greater than –115 dB for signals up to 1 MHz.



Two-Stage Band-Pass Filter

Figure 16



Channel Separation Test Circuit **Figure 17**

Package outline dimension