Fast 60V Protected High Side NMOS Static Switch Driver

FEATURES

- **Wide Operating V_{IN}: 3.5V to 60V**
- **1Ω Pull-Down, 2.2Ω Pull-Up for Fast Turn-On and Turn-Off Times with 35ns Propagation Delays**
- **Internal Charge Pump for 100% Duty Cycle**
- **Short-Circuit Protected**
- **Adjustable Current Trip Threshold**
- **Current Monitor Output**
- Automatic Restart Timer
- Open-Drain Fault Flag
- Adjustable Turn-On Slew Rate
- Gate Driver Supply from 3.5V to 15V
- Adjustable V_{IN} Undervoltage and Overvoltage Lockouts
- Adjustable Driver Supply V_{CC} Undervoltage Lockout
- Low Shutdown Current: 1µA
- CMOS Compatible Input
- Thermally Enhanced, High Voltage Capable 16-Lead MSOP Package

DESCRIPTION

The LTC®7003 is a fast high side N-channel MOSFET gate driver that operates from input voltages up to 60V. It contains an internal charge pump that fully enhances an external N-channel MOSFET switch, allowing it to remain on indefinitely.

Its powerful driver can easily drive large gate capacitances with very short transition times, making it well suited for both high frequency switching applications or static switch applications that require a fast turn-on and/or turn-off time.

When an internal comparator senses that the switch current has exceeded a preset level, a fault flag is asserted and the switch is turned off after a period of time set by an external timing capacitor. After a cooldown period, the LTC7003 automatically retries.

The LTC7003 is available in the thermally-enhanced 16-lead MSOP package.

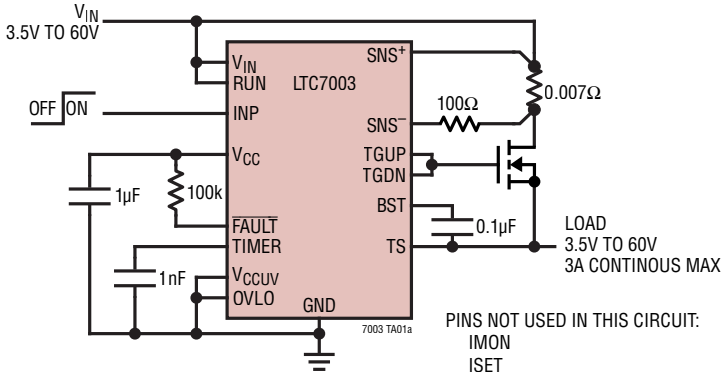
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APPLICATIONS

- Static Switch Driver
- Load and Supply Switch Driver
- Electronic Valve Driver
- High Frequency High Side Gate Driver

TYPICAL APPLICATION

High Side Switch with 100% Duty Cycle and Overcurrent Protection



Turn-On Transient Waveform

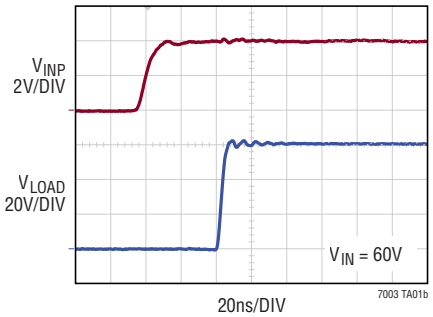


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ABSOLUTE MAXIMUM RATINGS

(Note 1)

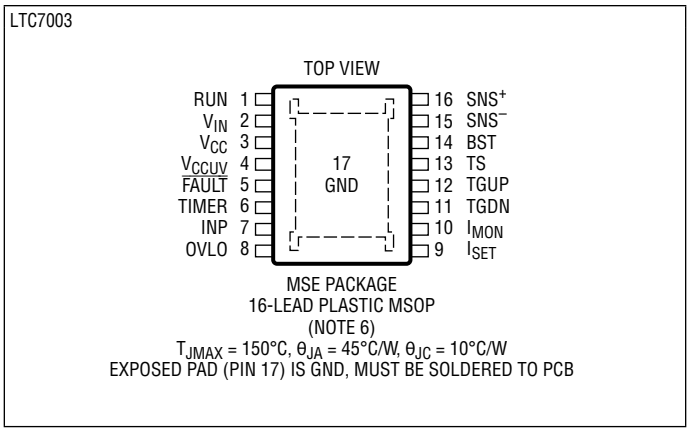
Supply Voltages
- V_{IN} ..... –0.3V to 65V
- BST-TS ..... –0.3V to 15V
- V_{CC} ..... –0.3V to 15V
- BST Voltage ..... –0.3V to 80V

TS Voltage ..... –6V to 65V
RUN, SNS^+ and SNS^- Voltages ..... –0.3V to 65V
$SNS^+ – SNS^-$
- Continuous ..... –0.3V to +0.3V
- <1msec ..... –100mA to +100mA

INP Voltage ..... –6V to 15V
Driver Outputs TGUP, TGDN ..... (Note 7)
TIMER, $\overline{FAULT}$, Voltages ..... –0.3V to 15V
V_{CCUV}, I_{SET}, I_{MON}, OVLO Voltages ..... –0.3V to 6V
Operating Junction Temperature Range (Notes 2, 3, 4)
- LTC7003E, LTC7003I ..... –40°C to 125°C
- LTC7003H ..... –40°C to 150°C
- LTC7003MP ..... –55°C to 150°C

Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
- MSOP Package ..... 300°C

PIN CONFIGURATION



MSE PACKAGE
16-LEAD PLASTIC MSOP
(NOTE 6)
T_{JMAX} = 150°C, θ_{JA} = 45°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7003EMSE#PBF	LTC7003EMSE#TRPBF	7003	16-Lead Plastic MSOP	–40°C to 125°C
LTC7003IMSE#PBF	LTC7003IMSE#TRPBF	7003	16-Lead Plastic MSOP	–40°C to 125°C
LTC7003HMSE#PBF	LTC7003HMSE#TRPBF	7003	16-Lead Plastic MSOP	–40°C to 150°C
LTC7003MPMSE#PBF	LTC7003MPMSE#TRPBF	7003	16-Lead Plastic MSOP	–55°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{SNS}^+ = 10V, V_{CC} = V_{BST} = 10V, V_{TS} = GND = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supplies							
V_{IN}	Input Voltage Operating Range			3.5		60	V
	TS Operating Voltage Range			0		60	V
	$SNS^{+/-}$ Input Voltage Range	Independent of V_{IN}		3.5		60	V
	Total Supply Current (Note 8) ON or Sleep, Charge Pump Regulating ON Mode, Charge Pump Overdriven Sleep Mode, Charge Pump Overdriven Shutdown Mode	C_{VCC} = 1µF V_{RUN} = 2V, V_{BST} = Open, V_{TS} = V_{SNS} = 12V V_{INP} = 4V, V_{RUN} = 2V, V_{BST-TS} = 13V V_{INP} = 0.4V, V_{RUN} = 2V, V_{BST-TS} = 13V V_{RUN} = 0V	 ● ● 		 250 60 37 1	 85 60 3	 µA µA µA µA
	V_{IN} DC Supply Current, Charge Pump Overdriven (Note 5) ON Mode Sleep Mode Shutdown Mode	C_{VCC} = 1µF, V_{BST-TS} = 13V, V_{INP} = 4V, V_{RUN} = 2V V_{INP} = 0.4V, V_{RUN} = 2V V_{RUN} = 0V			 35 25 1	 	 µA µA µA
	SNS^+ Current	V_{INP} = 4V, V_{RUN} = 2V V_{INP} = 0.4V, V_{RUN} = 2V V_{RUN} = 0V			21 12 0		µA µA µA
	SNS^- Current	V_{INP} = 4V, V_{RUN} = 2V V_{INP} = 0.4V, V_{RUN} = 2V V_{RUN} = 0V	●	2	4 0 0	6.5	µA µA µA
	V_{CC} LDO Output Voltage	C_{VCC} = 1µF, V_{IN} = 12V			10		V
	V_{CC} LDO Dropout Voltage (V_{IN}-V_{CC})	V_{IN} = 6V, I_{VCC} = –1mA			0.2		V
V_{CC} UVLO	V_{CC} Undervoltage Lockout	V_{CCUV} = OPEN, V_{IN} = V_{CC} V_{CC} Rising V_{CC} Falling Hysteresis V_{CCUV} = 0V, V_{IN} = V_{CC} V_{CC} Rising V_{CC} Falling Hysteresis V_{CCUV} = 1.5V, V_{IN} = V_{CC} V_{CC} Rising V_{CC} Falling Hysteresis	 ● ● ● ● 	 6.5 5.8 3.1 2.8 9.7 9.1 	 7.0 6.4 600 3.5 3.2 300 10.5 9.9 600	 7.5 6.9 3.7 3.4 10.9 10.3 	 V V mV V V mV V V mV
Bootstrapped Supply (BST-TS)							
V_{BST-TS}	V_{TG} Above V_{TS} with V_{INP} = 3.5V (DC)	V_{IN} = V_{CC} = V_{TS} = 7V, I_{BST} = 0µA V_{IN} = V_{CC} = V_{TS} = 10V, I_{BST} = 0µA V_{TS} = 60V, I_{BST} = 0µA	 ● ●	9 10 10	11 12 12	14 14 14	V V V
	Charge Pump Output Current	V_{TS} = 20V, V_{BST-TS} = 10V	●	–15	–30		µA
	BST-TS Floating UVLO	BST-TS Rising BST-TS Falling			3.1 2.8		V V
Output Gate Driver (TG)							
	TG Pull-Up Resistance	V_{IN} = V_{BST} = 12V	●		2.2	7	Ω
	TG Pull-Down Resistance	V_{IN} = V_{BST} = 12V	●		1	4	Ω
t_r	Output Rise Time	10% to 90%, CL = 1nF 10% to 90%, CL = 10nF			13 90		ns ns
t_f	Output Fall Time	10% to 90%, CL = 1nF 10% to 90%, CL = 10nF			13 40		ns ns
t_{PLH} t_{PHL}	Input to Output Propagation Delay	V_{INP} Rising, CL = 1nF V_{INP} Falling, CL = 1nF	● ●		35 35	70 70	ns ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{SNS}^+ = 10V, V_{CC} = V_{BST} = 10V, V_{TS} = GND = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operation							
V_{IH} V_{IL}	Input Threshold Voltages	V_{INP} Rising V_{INP} Falling Hysteresis	● ●	1.7 1.3	2 1.6 400	2.2 1.8	V V mV
	Input Pull-Down Resistance	V_{INP} = 1V			1		MΩ
	RUN and OVLO Pin Threshold Voltages	Rising Falling Hysteresis		1.16 1.05	1.21 1.10 110	1.26 1.15	V V mV
	RUN and OVLO Leakage Current	V_{RUN} = 1.3V, V_{OVLO} = 1.3V	●	–100	0	100	nA
	TIMER Threshold Voltage	V_{TIMER} Rising to $V_{\overline{FAULT}}$ Going Low		1.25	1.3	1.35	V
	TIMER Early Warning Voltage	$V_{\overline{FAULT}}$ Going Low to (TG-TS) Going Low		75	100	125	mV
	TIMER Pin Fault Pull-Up Current	V_{TIMER} = 1.0V, I_{SET} = OPEN	●	–115	–100	–80	µA
	TIMER Pin Pull-Down Current	V_{TIMER} = 0.6V I_{SET} = OPEN ΔV_{SNS} = 0mV		2.0	2.5	3.0	µA
	$\overline{FAULT}$ Output Low Voltage	$I_{\overline{FAULT}}$ = 1mA	●		0.2	0.5	V
	$\overline{FAULT}$ Leakage Current	$V_{\overline{FAULT}}$ = 5V	●	–100	0	100	nA
ΔV_{TH}	Current Sense Threshold Voltage ΔV_{SNS} = (V_{SNS}^+ – V_{SNS}^-)	I_{SET} = OPEN V_{ISET} = 1.2V V_{ISET} = 0V	●	22 54 15	30 60 20	36 64 24	mV mV mV
D	Retry Duty Cycle	ΔV_{SNS} = 200mV C_{TIMER} = 1nF	●		0.06	0.1	%
	I_{SET} and V_{CCUV} Pull-Up Current	V_{ISET} = 1.0V, V_{CCUV} = 1.0V		–11.3	–10	–8.7	µA
	I_{MON} Output Voltage	ΔV_{SNS} = 60mV, V_{TIMER} = 0V, V_{INP} = 3.5V ΔV_{SNS} = 30mV, V_{TIMER} = 0V, V_{INP} = 3.5V ΔV_{SNS} = 0mV, V_{TIMER} = 0V, V_{INP} = 3.5V	●	1.12 0.52	1.2 0.6 0	1.28 0.68 0.1	V V V
	Over-Current to TG Low Propagation Delay	ΔV_{SNS} Step 10mV to 50mV, I_{SET} = OPEN, V_{TIMER} = V_{CC}, V_{INP} = 3.5V			70		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7003 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC7003E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7003I is guaranteed over the –40°C to 125°C operating junction temperature range, the LTC7003H is guaranteed over the –40°C to 150°C operating junction temperature range and the LTC7003MP is tested and guaranteed over the –55°C to 150°C operating junction temperature range.

High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA}),$$ where θ_{JA} is 45°C/W.

Note 4: This IC includes over temperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

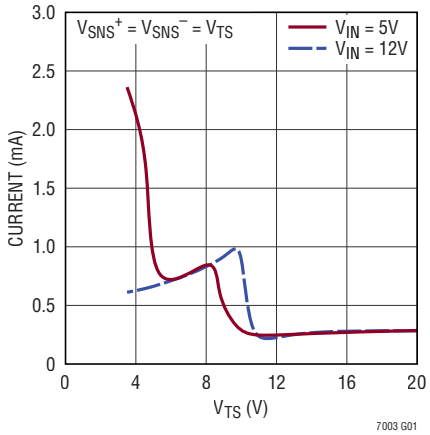
Note 6: For application concerned with pin creepage and clearance distances at high voltages, the MSE16(12) variation package should be used. See Applications Information.

Note 7: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only; otherwise permanent damage may occur.

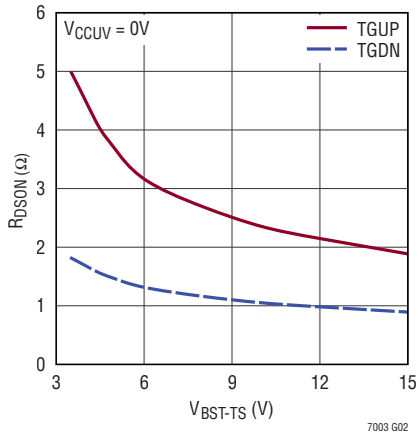
Note 8: Total supply current is the sum of the current into the V_{IN}, SNS^+, SNS^- and TS pins.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

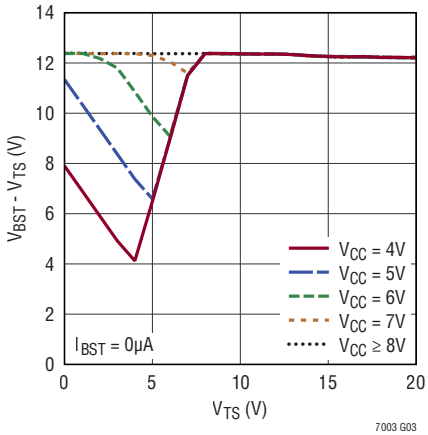
Total Supply Current vs V_{TS}



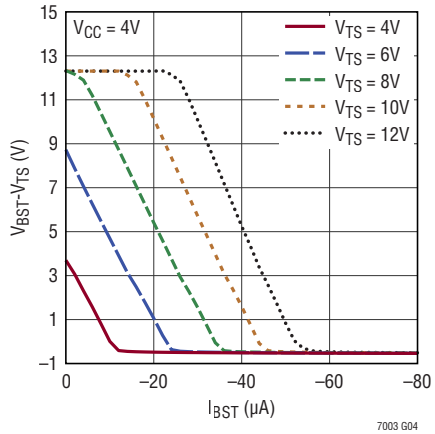
Driver On Resistance vs V_{BST-TS} Voltage



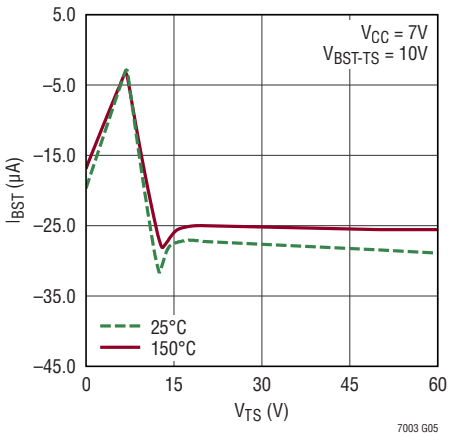
Charge Pump No-Load Output Voltage vs V_{TS}



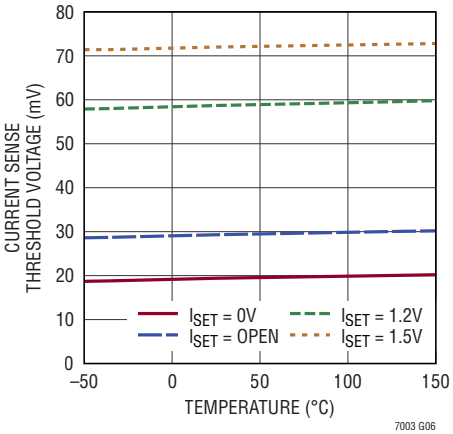
Charge Pump Load Regulation



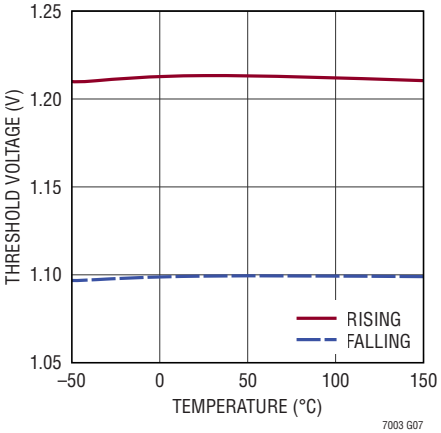
Charge Pump Output Current vs V_{TS}



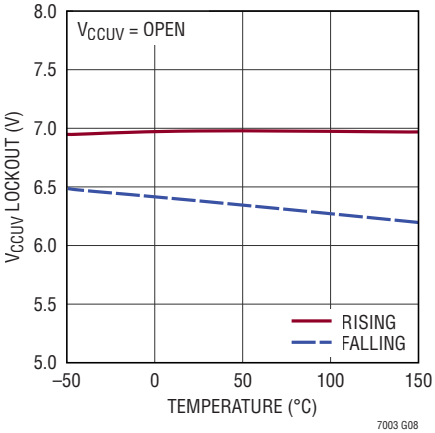
ΔV_{TH} vs Temperature



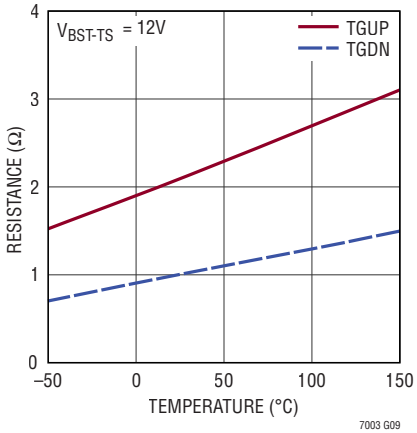
RUN and OVLO Threshold Voltages vs Temperature



V_{CCUV} Lockout vs Temperature

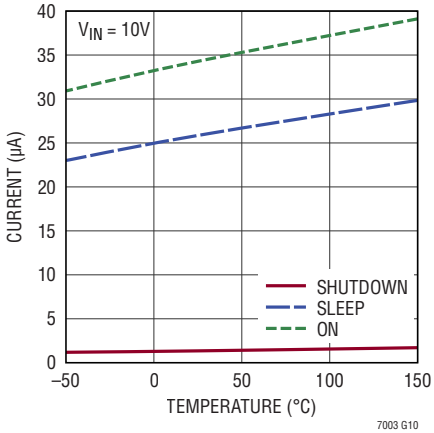


Driver On Resistance vs Temperature

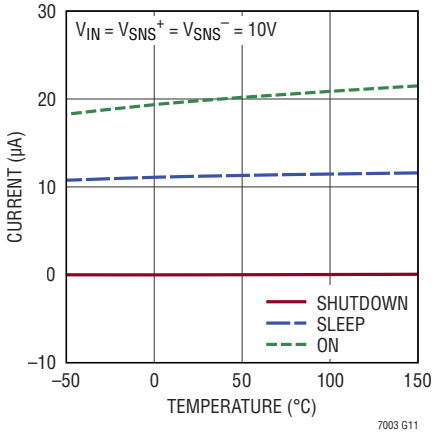


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

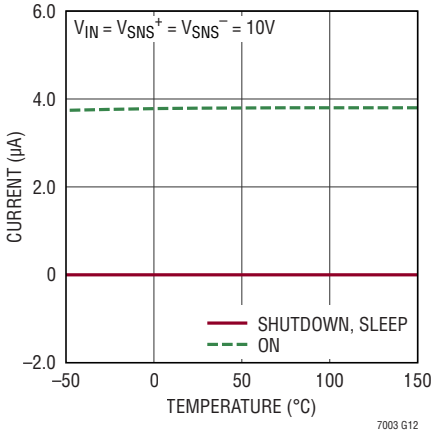
V_{IN} Supply Current vs Temperature



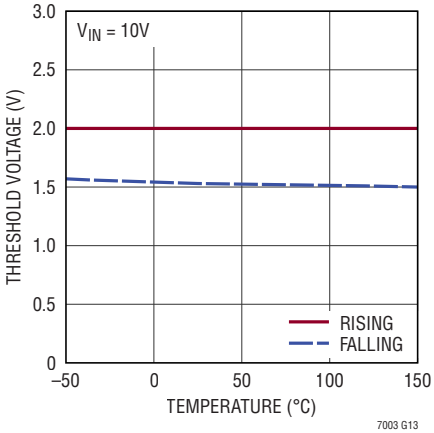
SNS^+ Supply Current vs Temperature



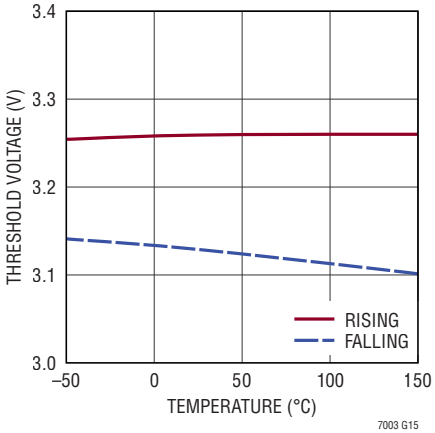
SNS^- Supply Current vs Temperature



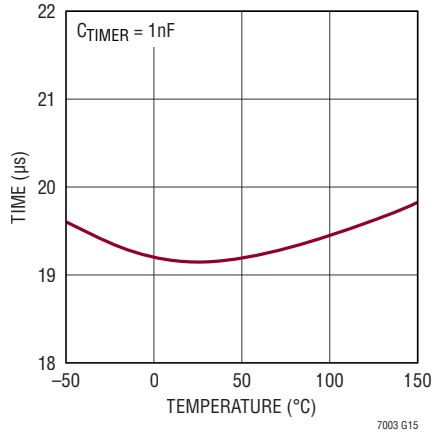
Input Threshold Voltage vs Temperature



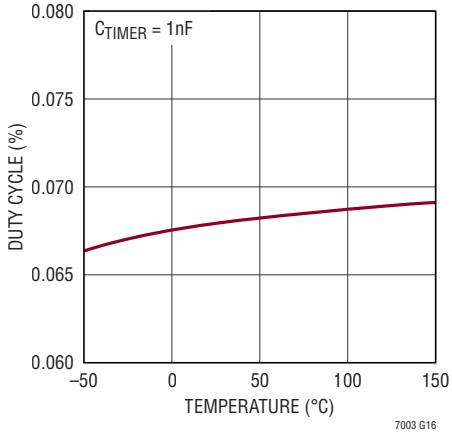
SNS^+ $\overline{FAULT}$ Threshold vs Temperature



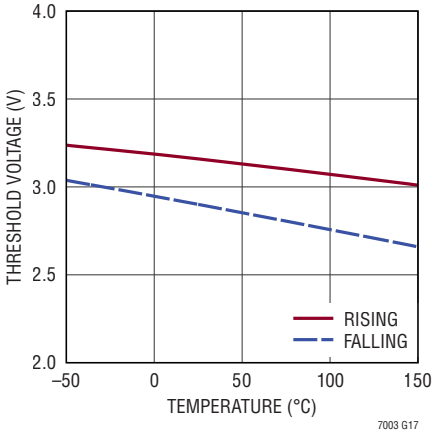
Overcurrent to TGDN = LOW Delay Time vs Temperature



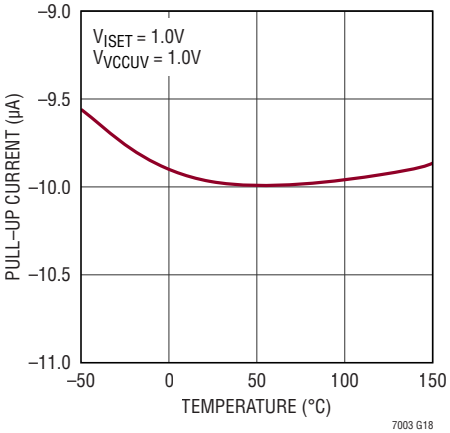
Retry Duty Cycle vs Temperature



V_{BST-TS} Floating UVLO Voltage vs Temperature



I_{SET} and V_{CCUV} Pull-Up Current vs Temperature



PIN FUNCTIONS

RUN (Pin 1): Run Control Input. A voltage on this pin above 1.21V enables normal operation. Forcing this pin below 0.7V shuts down the LTC7003, reducing quiescent current to approximately 1µA. Optionally connect to the input supply through a resistive divider to set the undervoltage lockout.

V_{IN} (Pin 2): Main Supply Pin. A bypass capacitor with a minimum value of 0.1µF should be tied between this pin and GND.

V_{CC} (Pin 3): Output of internal LDO and power supply for gate drivers and internal circuitry. Decouple this pin to GND with a minimum 1.0µF low ESR ceramic capacitor. Do not use the V_{CC} pin for any other purpose. V_{CC} can be overdriven from an external high efficiency source for high frequency switching applications that require higher power delivered to the external MOSFET. Do not connect V_{CC} to a voltage greater than V_{IN}.

V_{CCUV} (Pin 4): V_{CC} Supply Undervoltage Lockout. A resistor on this pin sets the reference for the Gate Drive undervoltage lockout. The voltage on this pin in the range of 0.4V to 1.5V is multiplied by 7 to be the undervoltage lockout for the Gate Drive (V_{CC} pin). Short to ground to set the minimum gate drive UVLO of 3.5V. Leave open to set gate drive UVLO to 7.0V

$\overline{\text{FAULT}}$ (Pin 5): Open Drain Fault Output. This pin pulls low after the voltage on the TIMER pin has reached the fault threshold of 1.3V. It indicates the pass transistor is about to turn off due to an overcurrent condition. The typical pull-down impedance is 200Ω. The $\overline{\text{FAULT}}$ pin does not go to a high-impedance state until the overcurrent condition and the TIMER cooldown period expire. If the TIMER pin is pulled above 3.5V, the TIMER function is disabled. In this state this pin pulls low when the $V_{TGUP-TS}$ signal is driven high.

TIMER (Pin 6): Fault Timer Input. A timing capacitor, CT, from the TIMER pin to GND sets the times for fault warning, fault turn off and retry periods (see Applications Information). When the TIMER pin is connected to a voltage higher than 3.5V, an overcurrent condition will immediately pull the TGUP pin to TS. TGDN will not go high again until the fault condition is reset by the INP pin going low and then back high.

INP (Pin 7): Input Signal. CMOS compatible input reference to GND that sets the state of TGDN and TGUP pins (see Applications Information). INP has an internal 1MΩ pull-down to GND to keep TGDN pulled to TS during startup transients.

OVLO (Pin 8): Overvoltage Lockout Input. Connect to the input supply through a resistor divider to set the overvoltage lockout level. A voltage on this pin above 1.21V causes TGDN to be pulled to TS. Normal operation resumes when the voltage on this pin decreases below 1.11V. Triggering an OVLO causes a fault condition. OVLO should be tied to GND when not used.

I_{SET} (Pin 9): Current Trip Threshold Set. A resistor on this pin to GND sets the peak current threshold. The voltage on this pin (internally clamped between 0.4V and 1.5V) is divided by 20 to be the current comparator reference. Short to GND for minimum peak current (20mV ΔV_{TH}). Leave open for an accurate peak current (30mV ΔV_{TH}).

I_{MON} (Pin 10): Current Monitor. The voltage on this pin with respect to GND represents the voltage across the sense resistor multiplied by 20. The range on this pin is 0V to 1.5V.

TGDN (Pin 11): High Current Gate Driver Pull-Down. This pin pulls down to TS. For the fastest turn-off, tie this pin directly to the gate of the external high side MOSFET.

TGUP (Pin 12): High Current Gate Driver Pull-Up. This pin pulls up to BST. Tie this pin to TGDN for maximum gate drive transition speed. A resistor can be connected between this pin and the gate of the external MOSFET to control the in-rush current during turn-on. See Applications Information.

TS (Pin 13): Top (High Side) source connection or GND if used in ground referenced applications.

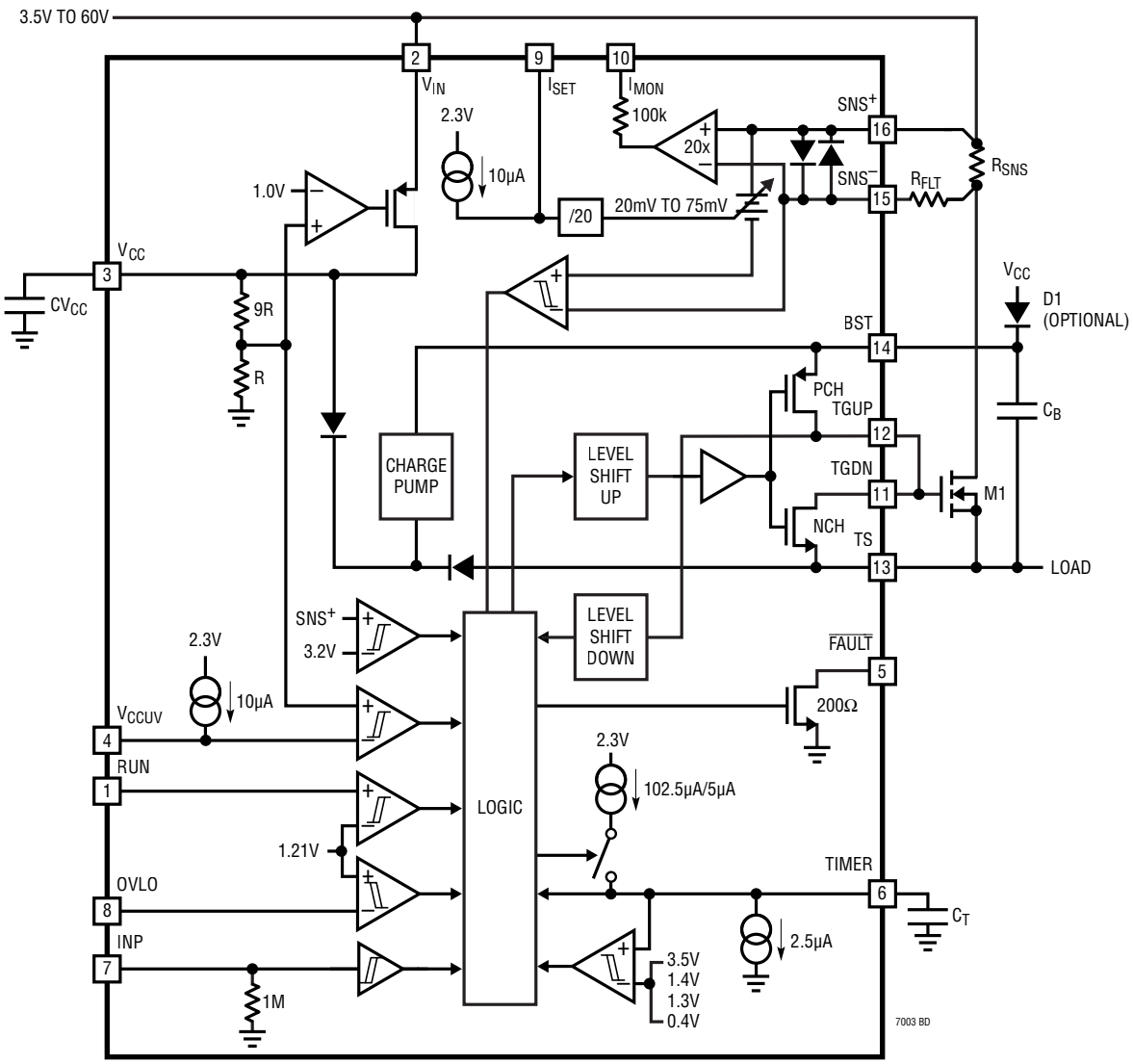
BST (Pin 14): High Side Bootstrapped Supply. An external capacitor with a minimum value of 0.1µF should be tied between this pin and TS. Voltage swing on this pin is 12V to (V_{IN} + 12V).

PIN FUNCTIONS

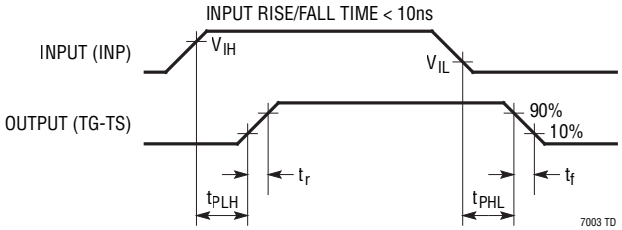
SNS⁻ (Pin 15), SNS⁺ (Pin 16): Current Sense Comparator Input. Place a sense resistor in series with the drain of the external MOSFET to set the peak current. The SNS⁻ pin should be connected to the sense resistor using a minimum 100Ω resistor. Use a Kelvin connection from the SNS⁺ pin to the sense resistor. The current comparator trip threshold voltage, ΔV_{TH} is the I_{SET} voltage divided by 20. The trip threshold is internally clamped to a minimum of 20mV and a maximum of 75mV. If I_{SET} is open or greater than 2.0V, ΔV_{TH} is set internally to 30mV.

GND (Exposed Pad Pin 17): Ground. The exposed pad must be soldered to the PCB for rated electrical and thermal performance.

BLOCK DIAGRAM



TIMING DIAGRAM



OPERATION (Refer to Block Diagram)

The LTC7003 is designed to receive a ground-referenced, low voltage digital input signal, INP and quickly drive and protect a high side N-channel power MOSFET whose drain can be up to 60V above ground. The LTC7003 is capable of driving a 1nF load using a 12V bootstrapped supply voltage (V_{BST}–V_{TS}) with 35ns of propagation delay and fast rise/fall times. The high gate drive voltage reduces external power losses associated with external MOSFET on-resistance. The strong drivers not only provide fast turn on and off times but hold the TGUP and TGDN to TS voltages in the desired state in the presence of high slew rate transients which can occur driving inductive loads at high voltages.

Overcurrent Protection

The LTC7003 protects a high side N-channel MOSFET from an overcurrent condition by monitoring the voltage across an external sense resistor placed in series with the drain of an external MOSFET and forcing the external MOSFET to turn off by pulling TGDN to TS when the voltage across the sense resistor, ΔV_{SNS}, exceeds the current comparator threshold voltage, ΔV_{TH}, after a period of time set by the timing capacitor, C_T. When an overcurrent condition is detected with I_{SET} open, ΔV_{TH} is internally programmed to a low value of 30mV minimizing the external conduction loss associated with current sensing by allowing the use of lower value sense resistors. A resistor placed between I_{SET} and ground allows ΔV_{TH} to be programmed from 20mV to 75mV.

An adjustable fault and overcurrent timer is enabled by placing a capacitor, C_T from the TIMER pin to ground and allows the load to continue functioning during brief overcurrent transient events while protecting the MOSFET from long periods of high currents. An external fault flag is available which can warn of an impending MOSFET turn off. A fast turn-off mode where TGDN is immediately pulled to TS due to an overcurrent is available by connecting the TIMER pin to V_{CC}.

Current Monitor

The LTC7003 provides an output voltage referenced to ground on the I_{MON} pin that reflects the current flowing through the external sense resistor connected between SNS^+ and SNS^- while TGUP is high. The voltage on I_{MON} is the voltage difference between the SNS^+ and SNS^- pins multiplied by 20x and referenced to ground with a range of 0V to 1.5V. The I_{MON} output voltage has an output impedance of 100kΩ and is pulled to ground with a 100kΩ resistor when INP is low.

V_{CC} Power

Power for the MOSFET driver and internal circuitry is derived from the V_{CC} pin. The V_{CC} pin voltage is generated from an internal P-channel LDO connected to V_{IN}. V_{CC} can also be overdriven from a high efficiency external source for high frequency switching applications that require higher power delivered to external MOSFET. V_{CC} should never be driven higher than V_{IN} or permanent damage to the LTC7003 could occur.

OPERATION (Refer to Block Diagram)

Internal Charge Pump

The LTC7003 contains an internal charge pump that enables the MOSFET gate drive to have 100% duty cycle. The charge pump regulates the BST-TS voltage to 12V reducing external power losses associated with external MOSFET on-resistance. The charge pump uses the higher voltage of TS or V_{CC} as the source for the charge.

Start-Up and Shutdown

If the voltage on the RUN pin is less than 0.7V, the LTC7003 enters a shutdown mode in which all internal circuitry is disabled, reducing the DC supply current to approximately 1µA. When the voltage on the RUN pin exceeds 0.7V, the internal LDO connected to V_{IN} is enabled and regulates V_{CC} to 10V. At V_{IN} voltages less than 10V, the LDO will operate in drop-out and V_{CC} will follow V_{IN}. When the voltage on the RUN pin exceeds 1.21V, the input circuitry is enabled allowing TGUP and TGDN to be driven high with respect to TS.

Protection Circuitry

When using the LTC7003, care must be taken not to exceed any of the ratings specified in the Absolute Maximum Ratings section. As an added safeguard, the LTC7003 incorporates an overtemperature shutdown feature. If the junction temperature reaches approximately 180°C, the LTC7003 will enter thermal shutdown mode and TGDN will be pulled to TS. After the part has cooled below 160°C, TGDN will be allowed to go back high. The overtemperature level is not production tested. The LTC7003 is guaranteed to start a temperatures below 150°C.

The LTC7003 additionally implements protection features which prohibit TGUP being pulled to BST when V_{IN}, V_{CC} or (V_{BST}–V_{TS}) are not within proper operating ranges. By using a resistive divider from V_{IN} to ground, the RUN and OVLO pins can serve as a precise input supply overvoltage/undervoltage lockouts. TGDN is pulled to TS when either RUN falls below 1.11V or OVLO rises above 1.21V, which can be configured to limit switching to a specific range on input supply voltages. Furthermore, if V_{IN} falls below 3.5V, an internal undervoltage detector pulls TGDN to TS.

V_{CC} contains an undervoltage lockout feature that will pull TGDN to TS and is configured by the V_{CCUV} pin. If V_{CCUV} is open, TGDN is pulled to TS until V_{CC} is greater than 7.0V. By using a resistor from V_{CCUV} to ground, the rising undervoltage lockout on V_{CC} can be adjusted from 3.5V to 10.5V.

An additional internal undervoltage lockout is included that will pull TGDN to TS when the floating voltage from BST to TS is less than 3.1V (typical).

APPLICATIONS INFORMATION

Input Stage

The LTC7003 employs CMOS compatible input thresholds that allow a low voltage digital signal connected to INP to drive standard power MOSFETs. The LTC7003 contains an internal voltage regulator which biases the input buffer connected to INP allowing the input thresholds (V_{IH} = 2.0V, V_{IL} = 1.6V) to be independent of variations in V_{CC}. The 400mV hysteresis between V_{IH} and V_{IL} eliminates false triggering due to noise events. However, care should be taken to keep INP from any noise pickup, especially in high frequency, high voltage applications.

INP also contains an internal 1MΩ pull-down resistor to ground, keeping TGDN pulled to TS during startup and other unknown transient events. During shutdown (V_{RUN}<0.7V) the internal 1MΩ pull-down resistor is disabled and INP becomes high impedance.

INP has an Absolute Maximum of –6V to +15V which allows the signal driving INP to have voltage excursions outside the normal power supply and ground range. It is not uncommon for signals routed with long PCB traces and driven with fast rise/fall times to inductively ring to voltages higher than power supply or lower than ground.

Output Stage

A simplified version of the LTC7003 output stage is shown in Figure 1. The pull-down device is an N-channel MOSFET with a typical 1Ω $R_{DS(ON)}$ and the pull-up device is a P-channel MOSFET with a typical 2.2Ω $R_{DS(ON)}$. The pull-up and pull-down pins have been separated to allow the turn-on transient to be controlled while maintaining a fast turn-off.

The LTC7003 powerful output stage (1Ω pull-down and 2.2Ω pull-up) minimizes transition losses when driving external MOSFETs and keeps the MOSFET in the state commanded by INP even if high voltage and high frequency transients couple from the power MOSFET back to the driving circuitry.

The large gate drive voltage on TGUP and TGDN reduces conduction losses in the external MOSFET because $R_{DS(ON)}$ is inversely proportional to its gate overdrive ($V_{GS} – V_{TH}$).

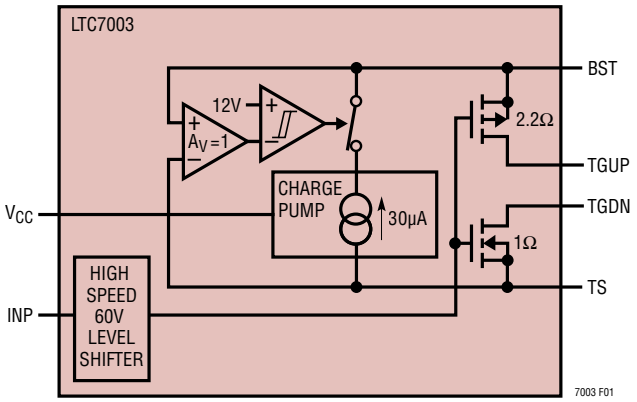


Figure 1. Simplified Output Stage

SNS+ and SNS– Pins

SNS+ and SNS– are the inputs to the high side current comparator and current monitor. The common mode operational voltage range for these pins is 3.5V to 60V independent of any other voltages. SNS+ also provides power to the current comparator and current monitor and draws approximately 21µA when not shut down and INP is high. SNS– draws a bias current of approximately 4µA when not shut down and INP is high. When SNS+ is less than 3.2V typical (3.5V maximum), a fault condition occurs and the adjustable fault timer is enabled with the same behavior as an overcurrent fault. Normally the SNS pins are connected to the drain side of the external MOSFET. However, the SNS pins can be connected to the source side of the external MOSFET as long as the source voltage rises above 3.5V before the Fault Timer expires. See Fault Timer and Fault Flag section.

A filter resistor, R_{FLT} should be placed in series with the SNS– pin as shown in Figure 2. Note that the SNS– pin takes 4µA of bias current which will affect the current sense and current monitoring functions. R_{FLT} should be at least 2000× larger than R_{SNS} (minimum 100Ω) to provide robustness during short-circuit events. The current injected in to the SNS+ and SNS– pins, during a short circuit event, depends on the voltage on POWER, R_{SNS}, external MOSFET R_{DSON}, timer capacitor value and the value of R_{FLT}.

APPLICATIONS INFORMATION

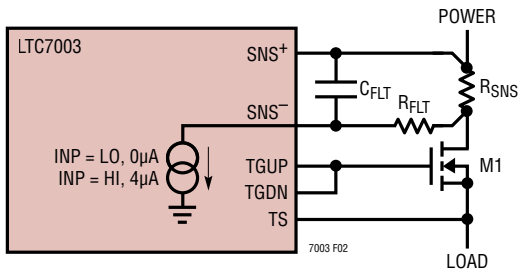


Figure 2. Sense Pins Filtering

I_{SET} Pin

The current comparator has an adjustable threshold voltage, ΔV_{TH}, of 20mV to 75mV and is set by placing a resistor to ground on the I_{SET} pin. The I_{SET} pin is biased with an internal 10µA current source. Floating I_{SET} enables the current comparator to have an accurate 30mV threshold voltage which allows for lower value sense resistors and reduces the external power dissipation. By placing a 40kΩ to 150kΩ resistor between I_{SET} and ground, the sense threshold voltage can be programmed to values between 20mV and 75mV. The value of resistor for a particular sense threshold voltage can be selected using Figure 3 or the following equation:

$$R_{ISET} = \frac{\Delta V_{TH}}{0.5\mu A}$$

Where 20mV< ΔV_{TH} < 75mV.

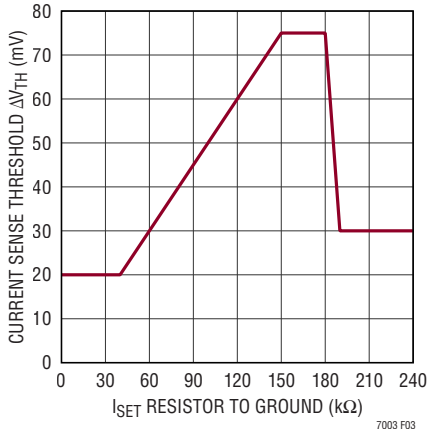


Figure 3. R_{ISET} Selection

Fault Timer and Fault Flag

The LTC7003 includes an adjustable fault timer. Connecting a capacitor from the TIMER pin to ground sets the delay period before the external MOSFET is turned off during an overcurrent fault condition. The same capacitor also sets the cooldown period before the external MOSFET is allowed to turn back on. Once a fault condition is detected, a 100µA current charges the TIMER pin. When the voltage on the TIMER pin reaches 1.3V, the $\overline{FAULT}$ pin pulls low to indicate the detection of a fault condition and provide warning of an impending power loss. After the TIMER voltage crosses the 1.4V threshold, TGDN is immediately pulled to TS turning off the external MOSFET. The on-time of the external MOSFET, $T_{OVER_CURRENT}$, during an overcurrent event is given by the following equation:

$$T_{OVER_CURRENT} = \frac{1.4V \bullet C_{TIMER}}{100\mu A} + 1.5\mu sec$$

The warning time, $T_{WARNING}$, generated by an overcurrent event is given by the following equation:

$$T_{WARNING} = \frac{0.1V \bullet C_{TIMER}}{100\mu A} + 1.5\mu sec$$

If the overcurrent fault condition disappears before TIMER has reached 1.4V, TIMER is discharged by a 2.5µA current. If TIMER had reached 1.3V ($\overline{FAULT}$ has gone low) and the overcurrent fault condition disappears, TIMER is discharged with a 2.5µA current and $\overline{FAULT}$ will be reset when TIMER reaches 0.4V. The on-time and warning times are shown graphically in Figure 4.

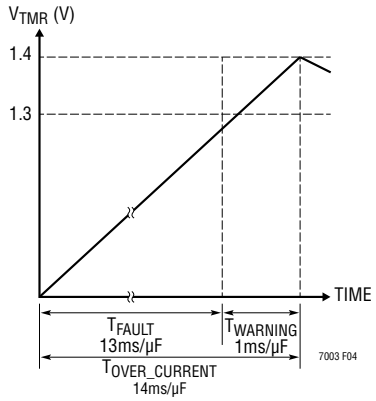


Figure 4. Fault Timer Trip Points

APPLICATIONS INFORMATION

Cooldown Period and Restart

As soon as TIMER reaches 1.4V, TGDN is pulled to TS in an overcurrent fault condition and the TIMER pin starts discharging with a 2.5µA current. When TIMER reaches 0.4V, TIMER charges with a 2.5µA current. When TIMER reaches 1.4V, it starts discharging again with a 2.5µA current. This pattern repeats 32 times to form a long cooldown timer period (T_{COOL_DOWN}) before retry (Figure 5).

If INP is cycled low, TGDN will be pulled to TS and TIMER will be pulled low with an internal 100kΩ resistor. If INP is cycled low during the cooldown period, the timer counter will be reset. If INP then goes high, TGUP will pulled to BST and the fault timer will be reactivated with the TIMER voltage starting from it's current value.

At the end of the cooldown period (when TIMER drops below 0.4V for the 32nd time), the LTC7003 retries, pulling TGUP to BST and turning on the external MOSFET. The $\overline{FAULT}$ pin will then go to a high impedance state. The total cooldown timer period is given by:

$$T_{COOL_DOWN} = \frac{63 \bullet 1.0V \bullet C_{TIMER}}{2.5\mu A}$$

The retry duty cycle in percent is to a first order independent of C_T and is defined by:

$$D = \frac{100 \bullet T_{OVER_CURRENT}}{T_{OVER_CURRENT} + T_{COOL_DOWN}}$$

To defeat the automatic retry, place a 100kΩ resistor in parallel with the TIMER capacitor. Note that the time to turn off from an overcurrent fault will be increased by 7% and the $\overline{FAULT}$ pin will remain low indicating a fault has occurred. To get the LTC7003 to retry and to clear the fault flag the INP signal needs to cycle low then back high.

Typical turn-off times and cooldown periods for some standard value timer capacitors are shown Table 1:

Table 1. Fault Time for Typical Capacitors

C_{TIMER} (nF)	$T_{OVER_CURRENT}$ (µs)	T_{COOL_DOWN} (s)	Retry Duty Cycle %
<0.1	~3	0.0005	~0.6
1	16	0.025	0.06
10	142	0.250	0.06
100	1402	2.500	0.06

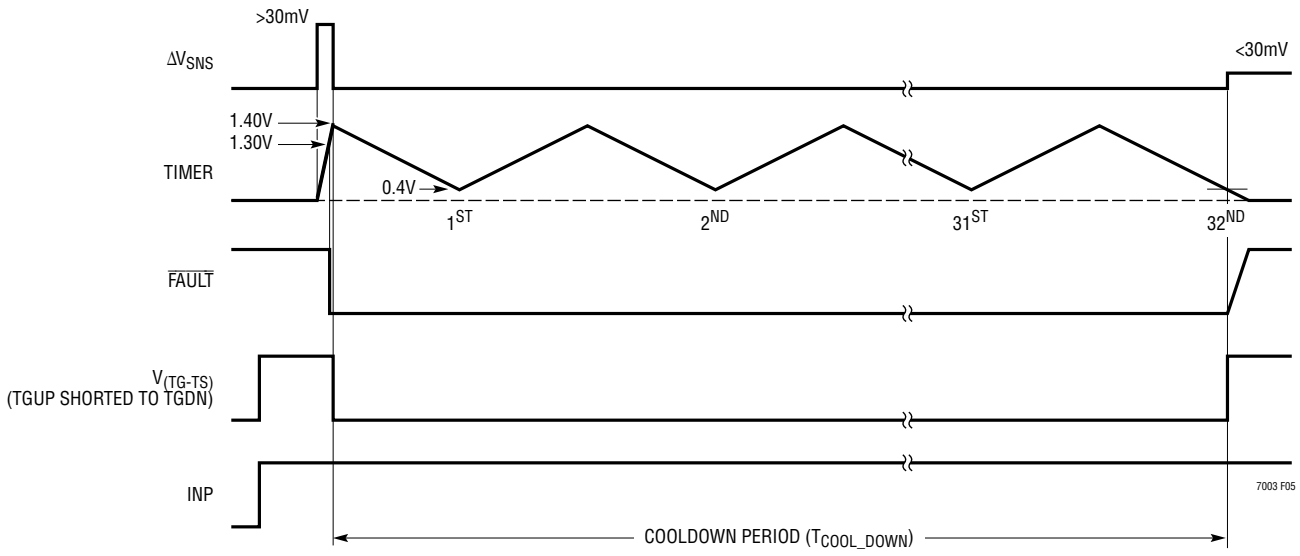


Figure 5. Auto Retry Cool-Down Timer Cycle

APPLICATIONS INFORMATION

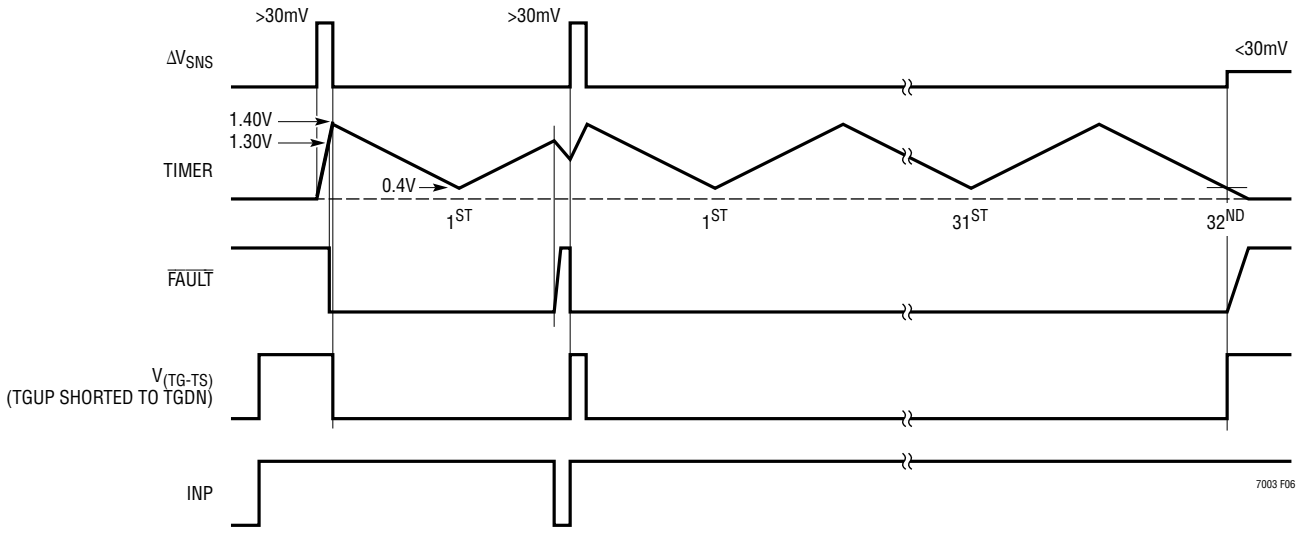


Figure 6. Auto Retry with INP Cycling Low

Fast Turn-Off Mode

If the TIMER pin is connected to V_{CC} or any other supply greater than 3.5V (abs max 15V), an overcurrent event will immediately pull TGDN to TS and the LTC7003 will remain there until the INP signal has cycled low and then back high. In fast turn-off mode, the typical delay from a ΔV_{SNS} overcurrent step to TG going low is around 70ns, so very fast short-circuit events can be detected. Also, when the TIMER pin is connected to a voltage greater than 3.5V, the $\overline{FAULT}$ signal is redefined to be the inverse state of the high side pull-up ($V_{TGUP} – V_{TS}$). The $\overline{FAULT}$ signal can be used in this application as low-voltage digital information that has been level shifted down from the high side MOSFET. An application for this could include using this signal to wait until $V_{TGUP}–V_{TS}$ has gone low before turning on a redundant power MOSFET.

High Side Current Monitor Output

The LTC7003 contains a high side current monitor output. The high side differential voltage sensed across the SNS^+ and $SNS^–$ pins (ΔV_{SNS}) is multiplied by 20 and ground referenced on the I_{MON} pin which makes it suitable for monitoring and regulating the MOSFET current. The working range of I_{MON} is 0V to 1.5V as ΔV_{SNS} varies from 0mV to 75mV. The I_{MON} pin is a voltage output whose nominal output impedance is 100kΩ and should not be resistively loaded. The current monitor output is only available after the INP signal has been high for 150µsec (typical), otherwise the I_{MON} pin is pulled to ground. A block diagram of the I_{MON} circuit is shown in Figure 7. The gm of the transimpedance amplifier tracks the 100kΩ internal resistor to ground which makes variations over process minimal.

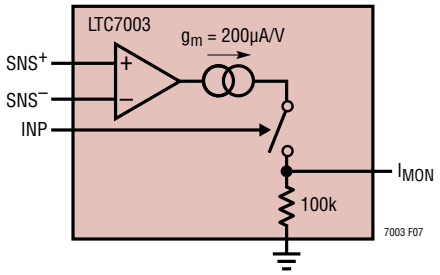


Figure 7. I_{MON} Block diagram

RUN Pin and External Input Overvoltage/Undervoltage Lockout

The RUN pin has two different threshold voltage levels. Pulling RUN below 0.7V puts the LTC7003 into a low quiescent current shutdown mode (I_Q ~ 1µA). When the RUN pin is greater than 1.21V, the part is enabled. Figure 8 shows examples of configurations for driving the RUN pin from logic.

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The RUN and OVLO pins can alternatively be configured as precise undervoltage (UVLO) and overvoltage (OVLO) lockouts on the V_{IN} supply with a resistive divider from V_{IN} to ground. A simple resistive divider can be used as shown in Figure 9 to meet specific V_{IN} voltage requirements. When RUN is less that 1.11V or OVLO is greater than 1.21V, TGDN will be pulled to TS and the external MOSFET will be turned off. The approximate delay time for the OVLO pin to turn on or turn off the external MOSFET is 2.5µsec. The approximate delay time for the RUN pin falling lower than 1.11V to turn off the external MOSFET is 3.5µsec.

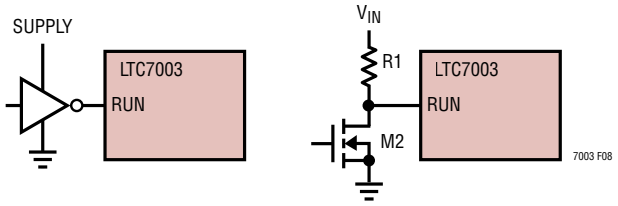


Figure 8. RUN Pin Interface to Logic

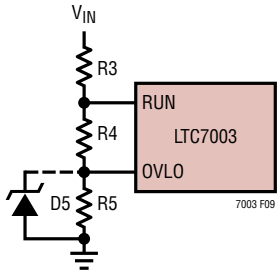


Figure 9. Adjustable UV and OV Lockout

The current that flows through the R3 – R4 – R5 divider will directly add to the shutdown, sleep and active current of the LTC7003, and care should be taken to minimize the impact of this current on the overall current used by the application circuit. Resistor values in the megaohm range may be required to keep the impact of the quiescent shutdown and sleep currents low. To pick resistor values, the sum total of R3 + R4 + R5 (R_{TOTAL}) should be chosen first based on the allowable DC current that can be drawn from V_{IN}. The individual values of R3, R4 and R5 can then be calculated from the following equations:

$$R5 = R_{TOTAL} \bullet \frac{1.21V}{\text{Rising } V_{IN} \text{ OVLO Threshold}}$$

$$R4 = R_{TOTAL} \bullet \frac{1.21V}{\text{Rising } V_{IN} \text{ UVLO Threshold}} - R5$$

$$R3 = R_{TOTAL} - R5 - R4$$

For applications that do not need a precise external OVLO the OVLO pin is required to be tied directly to ground. The RUN pin in this type of application can be used as an external UVLO using the above equations with R5 = 0Ω.

Similarly, for applications that do not require a precise UVLO, the RUN pin can be tied to V_{IN}. In this configuration, the UVLO threshold is limited by the internal V_{IN} UVLO thresholds as shown in the Electrical Characteristics table. The resistor values for the OVLO can be computed using the above equations with R3 = 0Ω.

Be aware that the OVLO pin cannot be allowed to exceed its absolute maximum rating of 6V. To keep the voltage on the OVLO pin from exceeding 6V, the following relationship should be satisfied:

$$V_{IN(MAX)} \bullet \left(\frac{R5}{R3 + R4 + R5} \right) < 6V$$

If the $V_{IN(MAX)}$ relationship for the OVLO pin cannot be satisfied, an external 5V Zener diode should also be placed from OVLO to ground in addition to any lockout setting resistors.

Bootstrapped Supply (BST-TS)

An external bootstrapped capacitor, C_B, connected between BST and TS supplies the gate drive voltage for the MOSFET driver. The LTC7003 keeps the BST-TS supply charged with an internal charge pump, allowing for duty cycles up to 100%. When the high side external MOSFET is to be turned on, the driver places the C_B voltage across the gate-source of the MOSFET. This enhances the high side MOSFET and turns it on. The source of the MOSFET, TS, rises to V_{IN} and the BST pin follows. With the high side MOSFET on, the BST voltage is above the input supply; $V_{BST} = V_{IN} + 12V$. The boost capacitor, C_B, supplies the charge to turn on the external MOSFET and needs to have at least 10 times the charge to turn on the external MOSFET fully. The charge to turn on the external MOSFET

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is referred to gate charge, Q_G, and is typically specified in the external MOSFET data sheet. Gate charge can range from 5nC to hundreds of nCs and is influenced by the gate drive level and the type of external MOSFET used. For most applications, a capacitor value of 0.1µF for C_B will be sufficient. However, the following relationship for C_B should be maintained:

$$C_B > \frac{\text{External MOSFET } Q_G}{1V}$$

The internal charge pump that charges the BST-TS supply outputs approximately 30µA to the BST pin. If the time to charge the external bootstrapped capacitor, C_B from initial power-up with the internal charge pump is not sufficient for the application, a low reverse leakage external silicon diode, D1, with a reverse voltage rating greater than V_{IN} connected between V_{CC} and BST should be used as shown in Figure 10. An external silicon diode between V_{CC} and BST should be used if the following relationship cannot be met:

$$\text{BST diode required if power-up to INP going high} < \frac{C_B \bullet 12V}{30\mu A} \cong 40ms$$

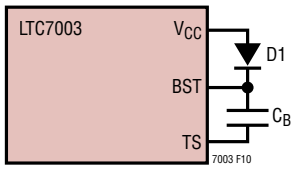


Figure 10. External BST Diode

Another reason to use an external silicon diode between V_{CC} and BST is if the external MOSFET is switched at a frequency so high that the BST-TS supply collapses. An external silicon diode between V_{CC} and BST should be used if the following relationship cannot be met:

$$\text{BST diode required if switching frequency} > \frac{30\mu A}{2 \bullet \text{MOSFET } Q_G} \cong 500Hz$$

A Schottky diode should not be used between V_{CC} and BST, as the reverse leakage of the Schottky diode at hot will be more current than the charge pump can overcome.

Some example silicon diodes with low leakage include:

- BAS116 Series, Multiple Vendors
- BAS416, Nexperia
- BAQ34, Vishay Semiconductors
- CMOD6001, Central Semiconductor

V_{CC} Generation

The V_{CC} pin provides the power for the MOSFET gate drivers and internal circuitry. The LTC7003 features an internal P-channel low dropout regulator (LDO) that can supply power at V_{CC} from the V_{IN} supply pin or V_{CC} can be driven from an external power supply. If the internal P-channel LDO is used to power V_{CC}, it must have a minimum 1.0µF low ESR ceramic capacitor to ensure stability and should not be connected to any other circuitry other than optionally biasing some pins on the LTC7003 ($\overline{FAULT}$, INP or TIMER).

If the internal P-channel LDO is used to power V_{CC} and an external silicon diode is used between V_{CC} and BST, care must be taken not to switch an external MOSFET at too high a frequency that can collapse the internal LDO. The internal LDO can only supply 1mA with a 200mV drop-out. In order to keep the internal LDO supply from collapsing when an external silicon diode is used from V_{CC} to BST, the following relationship should be maintained:

$$\text{Maximum switching frequency with internal LDO} < \frac{1mA}{2 \bullet \text{MOSFET } Q_G} \cong 20kHz$$

For higher gate charge applications, an external silicon diode between V_{CC} and BST should be used and V_{CC} can be driven from a high efficiency external supply. V_{CC} should never be driven higher than V_{IN} or permanent damage to the LTC7003 could occur.

V_{CC} Undervoltage Comparator

The LTC7003 contains an adjustable undervoltage lockout (UVLO) on the V_{CC} voltage that pulls TGDN to TS and can be easily programmed using a resistor (R_{VCCUV}) between the V_{CCUV} pin and ground. The voltage generated on V_{CCUV} by R_{VCCUV} and the internal 10µA current source set the V_{CC} UVLO. The rising V_{CC} UVLO is internally limited within

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the range of 3.5V and 10.5V. If V_{CCUV} is open the rising V_{CC} UVLO is set internally to 7.0V. The typical value of resistor for a particular rising V_{CC} UVLO can be selected using Figure 11 or the following equation:

$$R_{VCCUV} = \frac{\text{Rising } V_{CC} \text{ UVLO}}{70\mu A}$$

Where 3.5V < Rising V_{CC} UVLO < 10.5V.

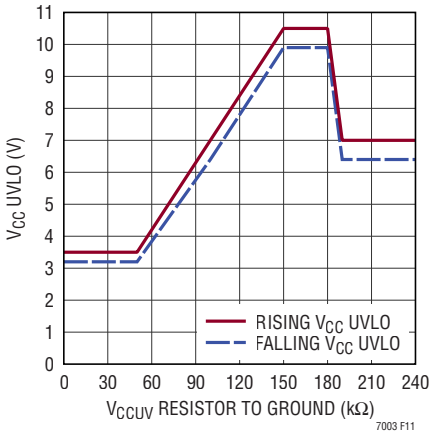


Figure 11. V_{CCUV} Resistor Selection

MOSFET Selection

The most important parameters in high voltage applications for MOSFET selection are the breakdown voltage BV_{DSS}, on-resistance $R_{DS(ON)}$ and the safe operating area, SOA.

The MOSFET, when off, will see the full input range of the input power supply plus any additional ringing than can occur when driving inductive loads.

External conduction losses are minimized when using low $R_{DS(ON)}$ MOSFETs. Since many high voltage MOSFETs have higher threshold voltages (typical $V_{TH} \geq 5V$) and $R_{DS(ON)}$ is directly related to the (V_{GS}–V_{TH}) of the MOSFET, the LTC7003 maximum gate drive of greater than 10V makes it an ideal solution to minimize external conduction losses associated with external high voltage MOSFETs.

SOA is specified in Typical Characteristic curves in power N-channel MOSFET data sheets. The SOA curves show the relationship between the voltages and current allowed in a timed operation of a power MOSFET without causing damage to the MOSFET. The overcurrent trip point (R_{SNS} and R_{ISET}) of the LTC7003 and TIMER capacitor should be chosen to stay within the SOA region of the MOSFET selected for the application.

Limiting Inrush Current During Turn-On

Driving large capacitive loads such as complex electrical systems with large bypass capacitors should be powered using the circuit shown in Figure 12. The pull-up gate drive to the power MOSFET from TGUP is passed through an RC delay network, R_G and C_G, which greatly reduces the turn-on ramp rate of the MOSFET. Since the MOSFET source voltage follows the gate voltage, the load is powered smoothly from ground. This dramatically reduces the inrush current from the source supply and reduces the transient ramp rate of the load allowing for slower activation of sensitive electrical loads. The turn-off of the MOSFET is not affected by the R_C delay network as the pull-down for the MOSFET gate is directly from the TGDN pin. Note that the voltage rating on capacitor C_G needs to be the same or higher than the external MOSFET and C_{LOAD}.

Adding C_G to the gate of the external MOSFET can cause high frequency oscillation. A low power, low ohmic value resistor (10Ω) should be placed in series with C_G to dampen the oscillations as shown in Figure 12 whenever C_G is used in an application. Alternatively, the low ohmic value resistor can be placed in series with the gate of the external MOSFET.

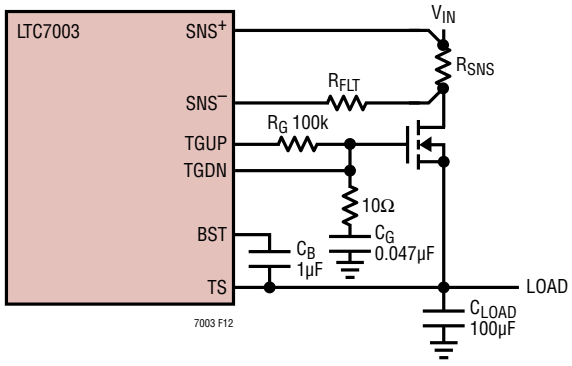


Figure 12. Powering Large Capacitive Loads

APPLICATIONS INFORMATION

The values for R_G and C_G to limit the inrush current can be calculated from the below equation:

$$I_{IN_RUSH} \cong \frac{0.7 \bullet 12V \bullet C_{LOAD}}{R_G \bullet C_G}$$

For the values shown in Figure 12 the inrush current will be:

$$I_{IN_RUSH} \cong \frac{0.7 \bullet 12V \bullet 100\mu F}{100k\Omega \bullet 0.047\mu F} \cong 180mA$$

Correspondingly, the ramp rate at the load for the circuit in Figure 12 is approximately:

$$\frac{\Delta V_{LOAD}}{\Delta T} \cong \frac{0.7 \bullet 12V}{R_G \bullet C_G} \cong 2V/ms$$

When C_G is added to the circuit in Figure 12, the value of the bootstrap capacitor, C_B, must be increased to be able to supply the charge to both to MOSFET gate and capacitor C_G. The relationship for C_B that needs to be maintained when C_G is used is given by:

$$C_B > \frac{MOSFET\ Q_G}{1V} + 10 \bullet C_G$$

Optional Schottky Diode Usage on TS

When turning off a power MOSFET that is connected to an inductive load (inductor, long wire or complex load), the TS pin can be pulled below ground until the current in the inductive load has completely discharged. The TS pin is tolerant of voltages down to –6V, however, an optional Schottky diode with a voltage rating at least as high as the load voltage should be connected between TS and ground to prevent discharging the load through the TS pin of the LTC7003. See Figure 13.

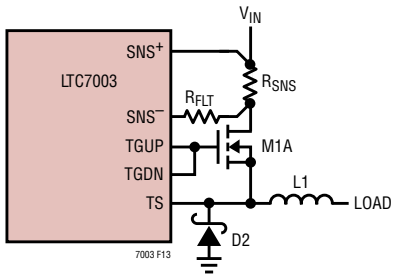


Figure 13. Optional Schottky Diode Usage

Reverse Current Protection

To protect the load from discharging back into V_{IN} when the external MOSFET is off and the V_{IN} voltage drops below the load voltage, two external N-channel MOSFETs should be used and must be configured in a back-to-back arrangement as shown in Figure 14. Dual N-channel packages such as the following devices are good choices for space saving designs:

- FDS3890, Fairchild/ON Semiconductor
- IRF7380PbF, Infineon/IR
- SQJB80EP, Vishay/Siliconix

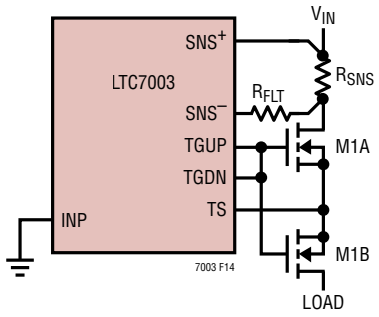


Figure 14. Protecting Load from Voltage Drops on V_{IN}

Design Example

As a design example, consider a fast power supply switch with the following specifications: $V_{IN} = V_{LOAD} = 4V$ to 60V, $I_{LOAD} = 3A$, Insertion Loss < 0.5W at room temp with maximum load, output rise time with a 1µF load is 1V/µs (1A inrush current) and a shorted load should immediately turn off the MOSFET.

The first item to select is the N-channel MOSFET. The Si7812DN is selected because it has sufficient breakdown voltage ($BV_{DSS_MIN} = 75V$), sufficient continuous current rating for a 3A load ($I_{D_MAX} = 5.7A$) and the on-resistance is low enough ($R_{DS(ON)_MAX} = 46m\Omega$) to be able to meet the power loss specification.

Examining the MOSFET data sheet, the V_{GS} vs $R_{DS(ON)}$ typical performance curve shows a sharp increase in $R_{DS(ON)}$ as the MOSFET V_{GS} gets below 5.0V. Since the default V_{CC} UVLO is 7.0V, the V_{CCUV} pin can be left open. The OVLO pin is connected to ground since there is no specification for Overvoltage Lockout.

APPLICATIONS INFORMATION

The value of the current sense resistor, R_{SNS} is calculated next. With I_{SET} open, the LTC7003 has a fixed current sense threshold, ΔV_{TH}, of 30mV typical and 22mV minimum. To provide a minimum 3A load current, the minimum specified ΔV_{TH} = 22mV should be used for the R_{SNS} calculation below:

$$R_{SNS} = \frac{22mV}{3A} = 7.3m\Omega$$

The closest standard value is 7mΩ. The power dissipation of R_{SNS} is 63mW so choose a power rating of greater than 0.25W to provide adequate margin.

The next item to check is to make sure the insertion loss specification is satisfied. The insertion loss is given by:

$$P_{LOSS} = I_{LOAD}^2 \bullet \left(R_{DS(ON)(MAX)} + R_{SNS}\right)$$
$$= 3A^2 \bullet \left(0.046\Omega + 0.007\Omega\right) = 0.48W$$

Which meets the design specification of less than 0.5W.

The fast output slew rate specification of 1V/µs into a 1µF load can be met by placing a resistor, R_G, in series with the TGUP pin to the MOSFET gate, as well as connecting TGDN and a capacitor, C_G, to ground on the MOSFET gate. The values of R_G and T_G can be calculated from the following expression:

$$R_G \bullet C_G \cong \frac{0.7 \bullet 12V}{1V/\mu s} = 8.4\mu s$$

C_G needs to have a voltage rating as high as the BV_{DSS} of the MOSFET. A good choice for C_G is the AVX 06031C471KAT2A which has a value of 470pF and a voltage rating of 100V. R_G is then calculated to be 17.8kΩ.

The bootstrap capacitor C_B can be calculated from the gate charge as specified in the MOSFET data sheet and C_G as follows:

$$C_B > \frac{Q_G}{1V} + 10 \bullet C_G = \frac{24nC}{1V} + 10 \bullet 470pF$$
$$\cong 0.33nF$$

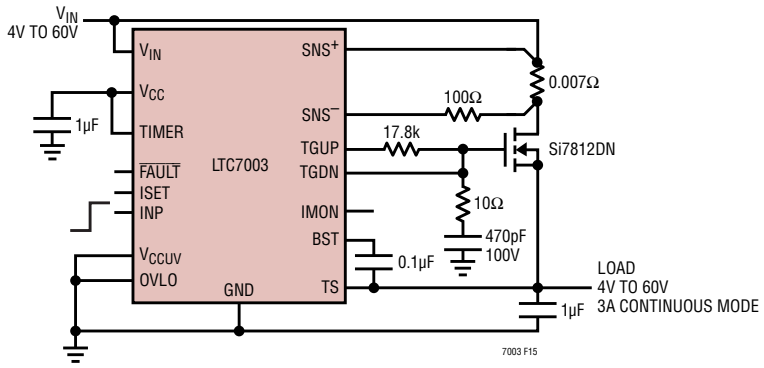
100nF will be used.

To meet the short-circuit specification, the TIMER pin should be connected to V_{CC} to enable immediate turn-off (approximately 70ns) of the MOSFET in the case of an overcurrent condition. If an overcurrent condition turns off the MOSFET, it will not turn back on until the INP pin has cycled low then back high.

The complete circuit is shown in Figure 15.

PC Board Layout Considerations

1. *Solder the exposed pad* on the backside of the LTC7003 packages directly to the ground plane of the board.
2. Kelvin connect the SNS^+ pin to the current sense resistor.
3. Limit the resistance of the TS trace, by making it short and wide.
4. C_B needs to be close to chip.
5. Always include an option in the PC board layout to place a resistor in series with the gate of any external MOSFET. High frequency oscillations are design dependent and having the option to add a series dampening resistor can save a design iteration of the PC board.



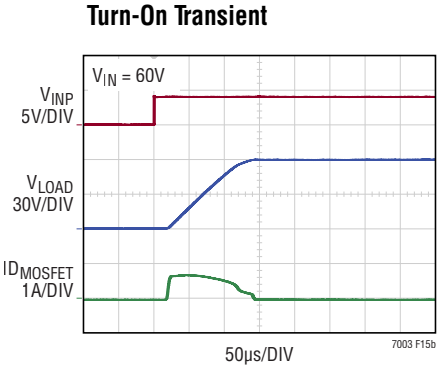
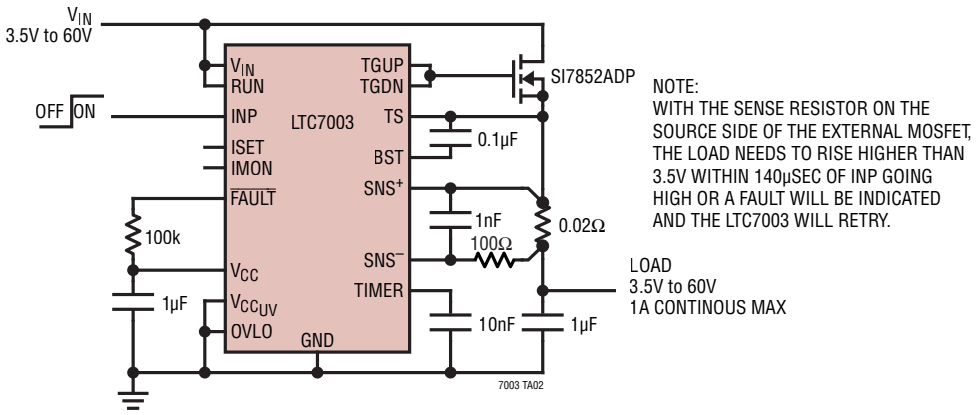


Figure 15. Design Example

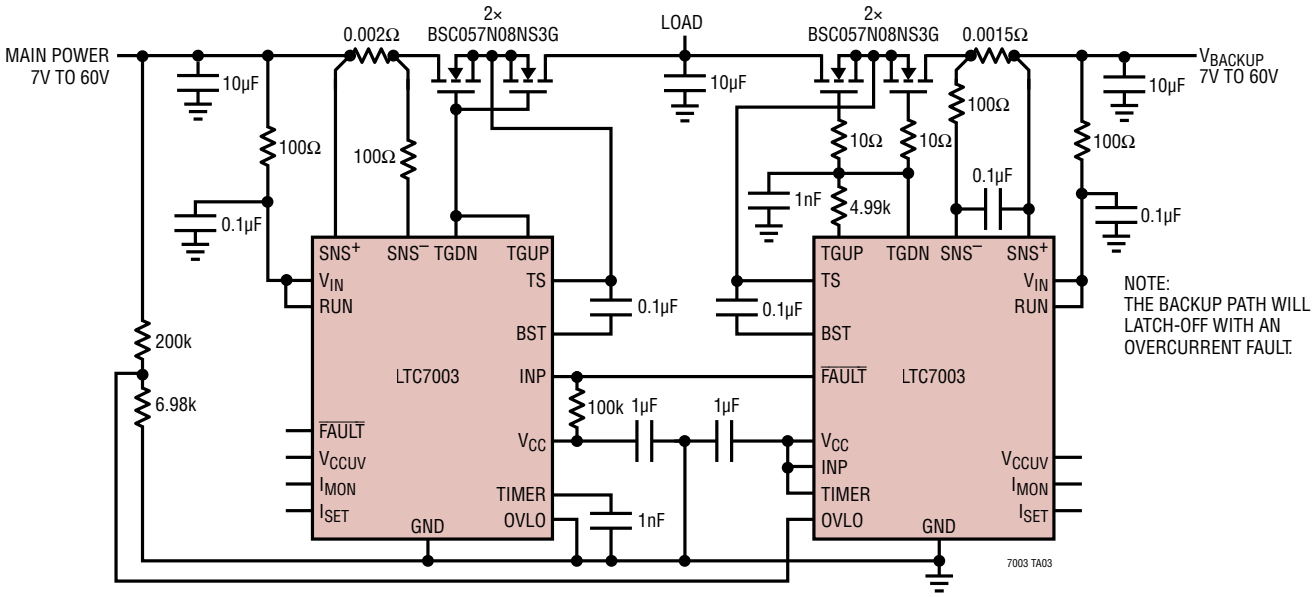
TYPICAL APPLICATIONS

Source Side Current Sense



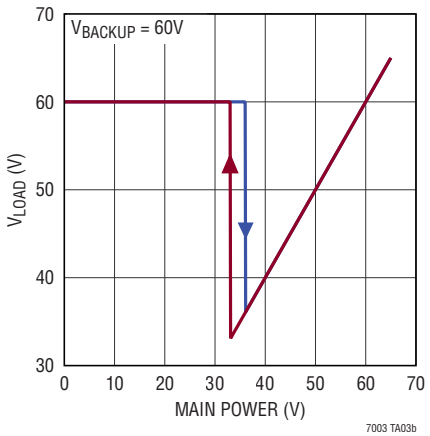
NOTE:
WITH THE SENSE RESISTOR ON THE SOURCE SIDE OF THE EXTERNAL MOSFET, THE LOAD NEEDS TO RISE HIGHER THAN 3.5V WITHIN 140µSEC OF INP GOING HIGH OR A FAULT WILL BE INDICATED AND THE LTC7003 WILL RETRY.

Protected Redundant Supply Switchover with Shoot Through Protection

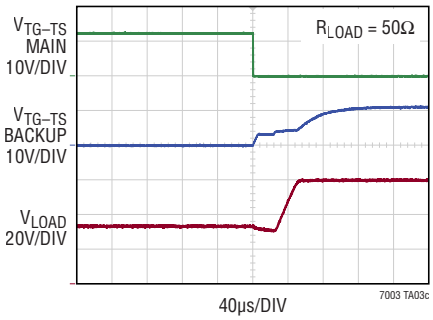


NOTE:
THE BACKUP PATH WILL LATCH-OFF WITH AN OVERCURRENT FAULT.

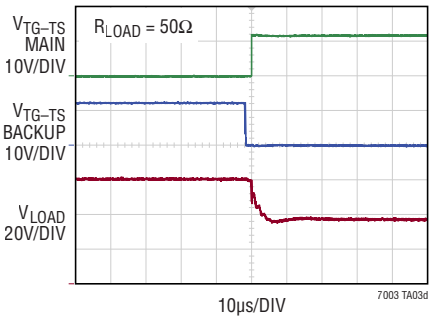
V_{LOAD} vs Main Power Voltage



V_{MAIN} Falling Through 33V

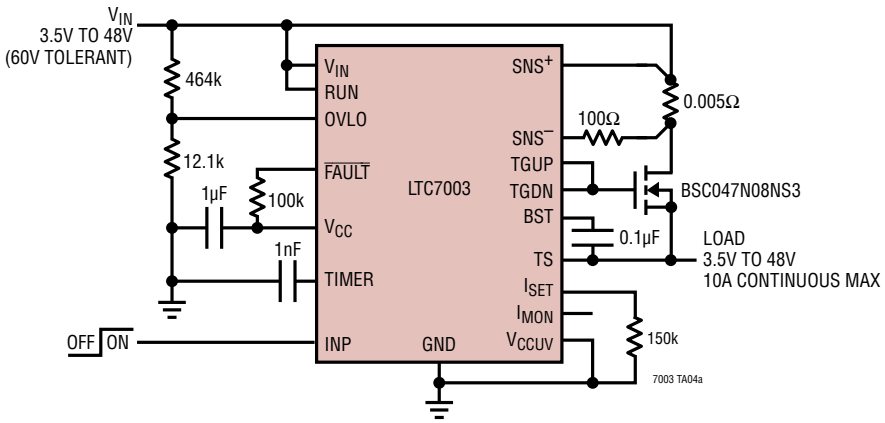


V_{MAIN} Rising Through 36V

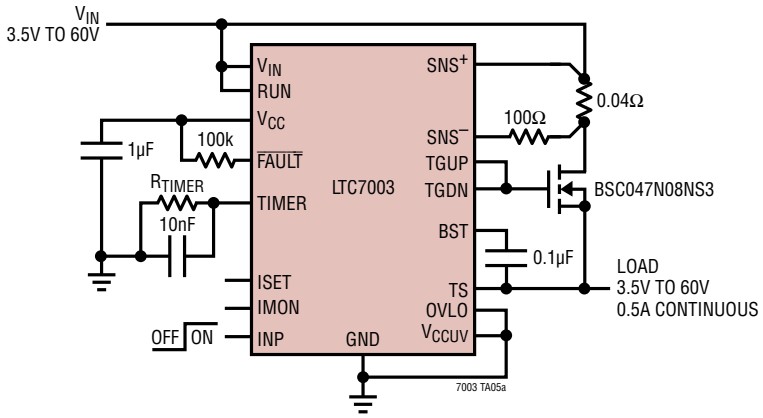


TYPICAL APPLICATIONS

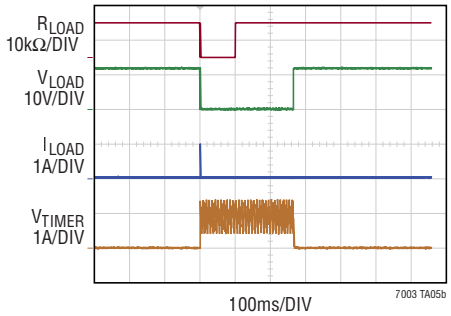
High Side Switch with Input Overvoltage and Overcurrent Protection



High Side Switch with Overcurrent Protection and Fault Latchoff

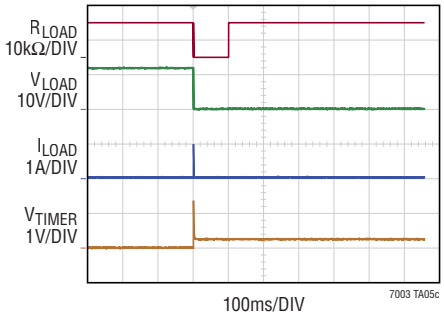


R_{TIMER} = OPEN
12Ω/100ms LOAD PULSE



V_{IN} = 12V
V_{INP} = 4V

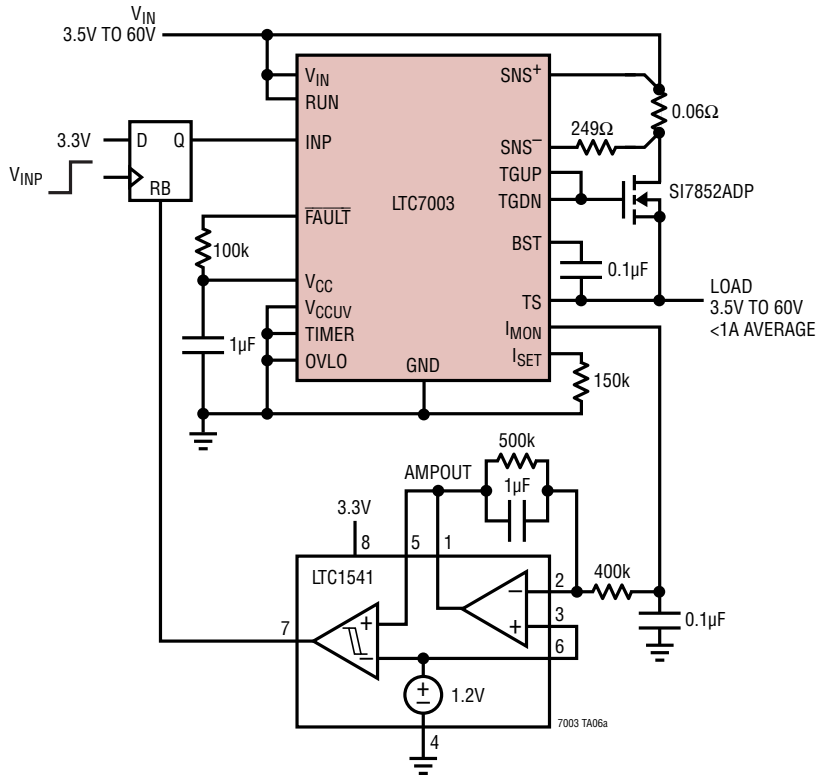
R_{TIMER} = 100k
12Ω/100mS LOAD PULSE



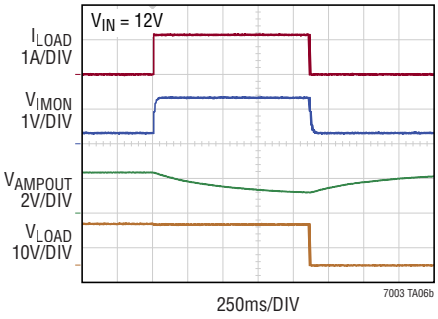
V_{IN} = 12V
V_{INP} = 4V

TYPICAL APPLICATIONS

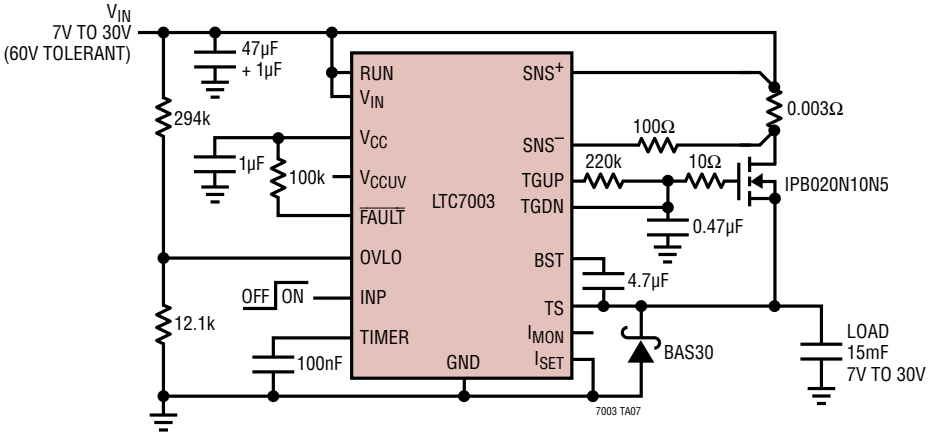
Average Current Trip



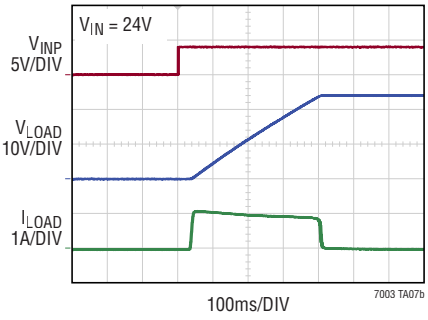
Response to 1.2A Load Step



High Side Switch with Auto-Retry, Inrush Control and OVLO

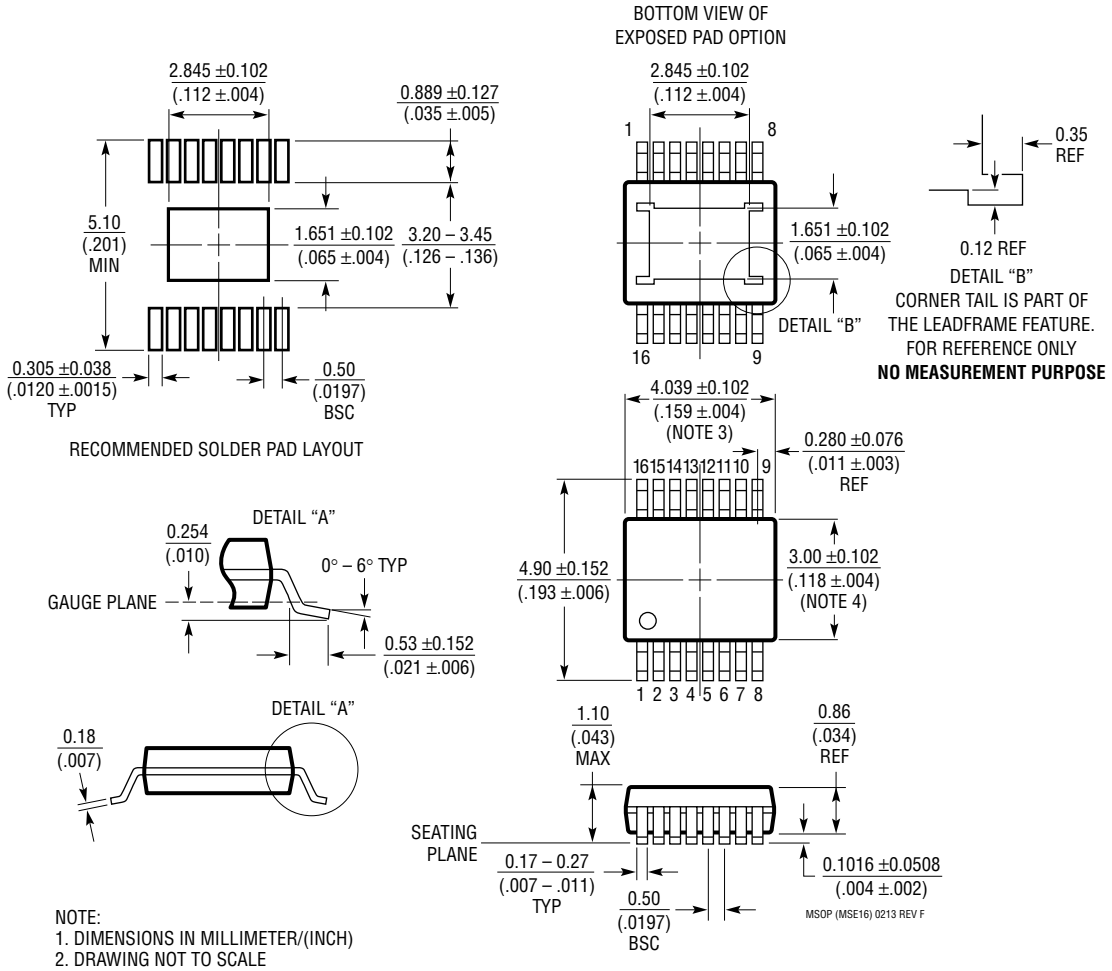


Turn-On Response



PACKAGE DESCRIPTION

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

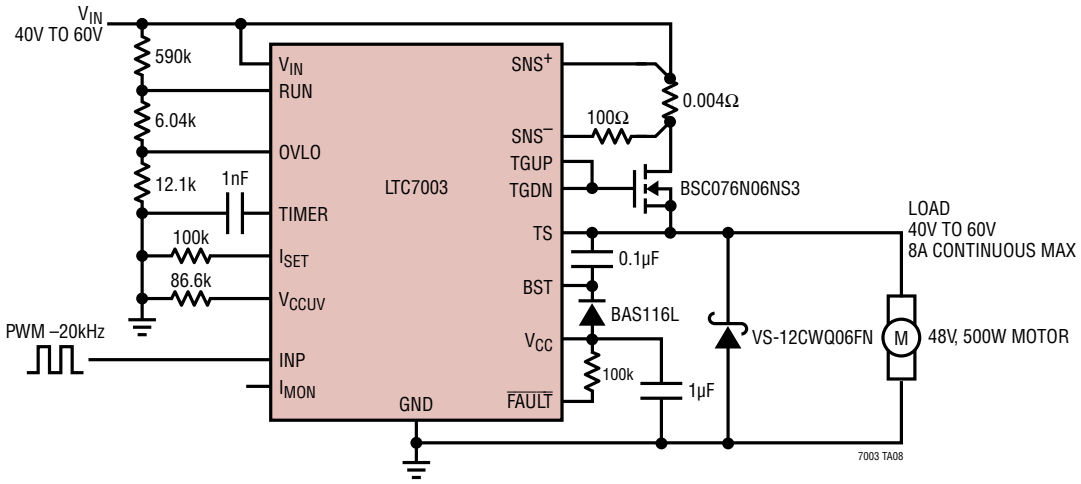
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/18	Added 100Ω resistor to Typical Application.	1
		Added Total Supply Current with Charge Pump Regulating section to Electrical Characteristics table.	4
		Removed the temperature dot from the TIMER Pin Pull-Down Current specification.	5
		Updated SNS^+ and SNS^- in Pin Functions.	9
		Added R_{FLT}.	18, 19, 20, 21, 22, 23, 26
B	09/20	Change parameter INP = 3V (DC) to V_{INP} = 3.5V (DC). Change condition V_{IN} = V_{TS} = 60V, I_{BST} = 0µA to V_{TS} = 60V, I_{BST} = 0µA.	4
		Add mV in units columns where indicated (two places).	5
		Update title to graph 7003 G01.	6

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TYPICAL APPLICATION

Protected Motor Driver



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC7000/LTC7000-1	Fast 150V Protected High Side NMOS Static Switch Driver	3.5V to 150V Operation, Short Circuit Protected, Delta V_{SNS} = 30mV, I_Q = 35µA, Turn-On (C_L = 1 nF) = 35ns, Internal Charge Pump
LTC7001	Fast 150V High Side NMOS Static Switch Driver	3.5V to 150V Operation, I_Q = 35µA, Turn-On (C_L = 1nF) = 35ns, Internal Charge Pump
LTC7004	Fast 60V High Side NMOS Static Switch Driver	3.5V to 60V Operation, I_Q = 27µA, Turn-On (C_L =1 nF) = 35ns, Internal Charge Pump
LTC4440/LTC4440-5/ LTC4440A-5	High Speed, High Voltage High Side Gate Driver	Up to 100V Supply Voltage, 8V ≤ V_{CC} ≤ 15V, 2.4A Peak Pull-Up/1.5Ω Peak Pull-Down
LTC7138	High Efficiency, 150V 250mA/400mA Synchronous Step-Down Regulator	Integrated Power MOSFETs, 4V ≤ V_{IN} ≤ 150V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 12µA, MSOP-16 (12)
LTC7103	105V, 2.3A Low EMI Synchronous Step-Down Regulator	4.4V ≤ V_{IN} ≤ 105V, 1V ≤ V_{OUT} ≤ V_{IN}, I_Q = 2µA Fixed Frequency 200kHz to 2MHz, 5mm x 6mm QFN
LTC7801	150V Low I_Q, Synchronous Step-Down DC/DC Controller	4V ≤ V_{IN} ≤ 140V, 150V abs max, 0.8V ≤ V_{OUT} ≤ 60V, I_Q = 40µA ,PLL Fixed Frequency 320kHz to 2.25MHz
LT1910	Protected High Side MOSFET Driver	8V to 48V Operation, ΔV_{SNS} = 65mV, I_Q = 110µA, Turn-On (C_L = 1nF) = 220µs, Internal Charge Pump
LTC1255	Dual 24V High Side MOSFET Driver	9V to 24V Operation, ΔV_{SNS} = 100mV, I_Q = 600µA, Turn-On (C_L = 1nF) = 100µs, Internal Charge Pump
LTC4367	100V Overvoltage, Undervoltage and Reverse Supply Protection Controller	Wide Operating Range: 2.5V to 60V, Protection Range: –40V to 100V, No TVS Required for Most Applications
LTC4368	100V Overvoltage, Undervoltage and Reverse Supply Protection Controller with Bidirectional Circuit Breaker	Wide Operating Range: 2.5V to 60V, Protection Range: –40V to 100V, No TVS Required for Most Applications
LTC4364	Surge Stopper with Ideal Diode	4V to 80V Operation, ΔV_{SNS} = 50mV, I_Q = 425µA, Turn-On (C_L = 1nF) = 500µs, Internal Charge Pump
LTC7860	High Efficiency Switching Surge Stopper	4V to 60V Operation, ΔV_{SNS} = 95mV, I_Q = 370µA, PMOS Driver
LTC4231	Micropower Hot Swap Controller	2.7V to 36V Operation, ΔV_{SNS} = 50mV, I_Q = 4µA, Turn-On (C_L = 1nF) = 1ms, Internal Charge Pump
LTC3895	150V Low I_Q, Synchronous Step-Down DC/DC Controller	PLL Fixed Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 140V, 0.8V ≤ V_{OUT} ≤ 60V, I_Q = 40µA
LTC4380	Low Quiescent Current Surge Stopper	4V to 80V Operation, ΔV_{SNS} = 50mV, I_Q = 8µA, Turn-On = 5ms, Internal Charge Pump
LTC3639	High Efficiency, 150V 100mA Synchronous Step-Down Regulator	Integrated Power MOSFETs, 4V ≤ V_{IN} ≤ 150V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 12µA, MSOP-16(12)

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