UMW PCF8563

Real-time clock/calendar

1.Description

The PCF8563 is a CMOS Real-Time Clock (RTC) and calendar optimized for low power consumption. A programmable clock output, interrupt output, and voltage-low detector are also provided. All addresses and data are transferred serially via a two-line bidirectional I^2C-bus. Maximum bus speed is 400 kbit/s. The register address is incremented automatically after each written or read day tabte.

2.Application

- Mobile telephones
- Portable instruments
- Electronic metering
- Battery powered products

3.Features

- Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768kHz quartz crystal
- Clock operating voltage: 1.0V to 5.5V at room temperature
- Low backup current; typical 0.25μA at V_{DD}=3.0V and Tamb=25°C
- 400kHz two-wire I^2C-bus interface (at V_{DD}=1.8V to 5.5V)
- Century flag
- Programmable clock output for peripheral devices (32.768kHz, 1.024kHz, 32Hz, and 1Hz)
- Alarm and timer functions
- Integrated oscillator capacitor
- Internal Power-On Reset (POR)
- I^2C-bus slave address: read A3h and write A2h Open-drain interrupt pin

4.Block Diagram

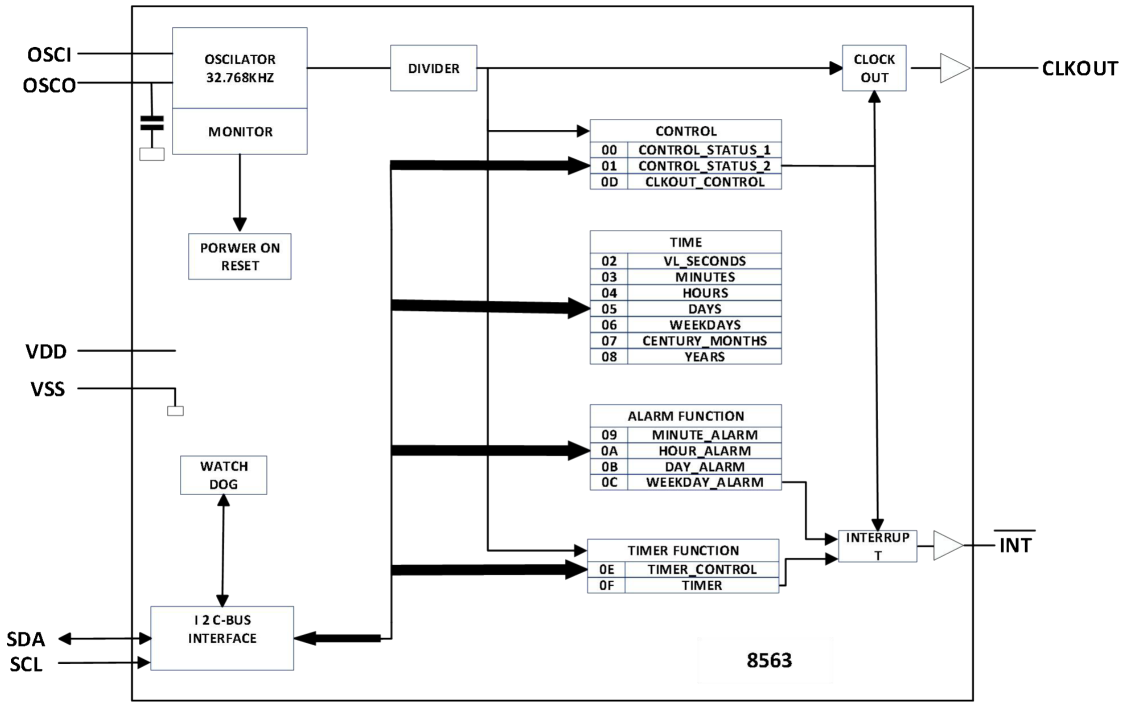
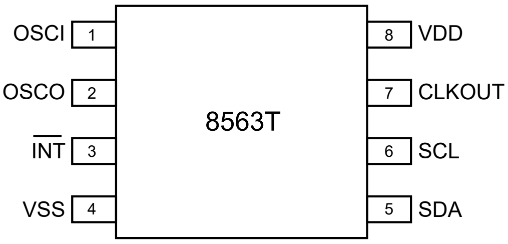
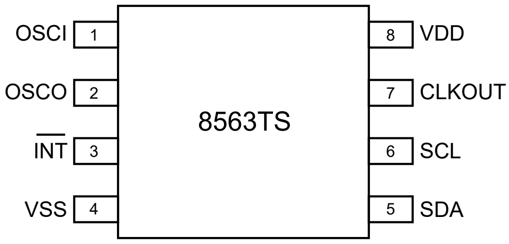


Figure 1. Block diagram of PCF8563

5.Pinning Information



SOP-8



MSOP-8

Pin Description

Pin		Symbol	Description
MSOP8	**SOP8**		
1	1	OSCI	Oscillator Input
2	2	OSCO	Oscillator Output
3	3	$\overline{\text{INT}}$	Interrupt Output (Open-drain; Active Low)
4	4	V_{SS}	Ground
5	5	SDA	Serial Data Input And Output
6	6	SCL	Serial Clock Input
7	7	CLKOUT	Clock Output, Open-drain
8	8	V_{DD}	Supply Voltage
-	-	n.c.	Not Connected; Do Not Connect And Do Not Use As Feed

[1] The die paddle (exposed pad) is wired to V_{SS} but should not be electrically connected.

6.Internal Circuitry

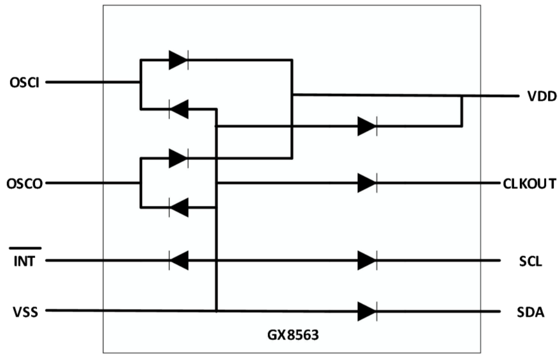


Figure 2. Device diode protection diagram

7.Limiting Values

Parameter	Symbol	Conditions	Min	Max	Units
Supply Voltage	V_{DD}		-0.5	6.5	V
Supply Current	I_{DD}		-50	50	mA
Input Voltage	V_I	on pins SCL, SDA, and OSCI	-0.5	6.5	V
Output Voltage	V_O	on pins CLKOUT and INT	-0.5	6.5	V
Input Current	I_I	at any input	-10	10	mA
Output Current	I_O	at any output	-10	10	mA
Total Power Dissipation	Ptot			300	mW
Electrostatic Discharge Voltage	V_{ESD}	HBM		±2000	V
Storage Temperature	T_{STG}		-65	150	°C
Ambient Temperature	T_{amb}	operating device	-40	85	°C

8.Electrical Characteristic

V_{DD}=1.0V to 5.5V; V_{SS}=0V; T_{amb}=-40°C to +85°C; f_{osc}=32.768kHz; quartz R_S=40kΩ; C_L=8pF; unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supplies						
Supply Voltage	V_{DD}	Interface Inactive; f_{SCL}=0Hz; T_{amb}=25°C [1]	1		5.5	V
		Interface Inactive; f_{SCL}=400kHz [1]	1.8		5.5	V
		Clock Data Integrity; T_{amb}=25°C	V_{low}		5.5	V
Supply Current	I_{DD}	Interface Active				V
		f_{SCL}=400kHz			800	μA
		f_{SCL}=100kHz			200	μA
		Interface Inactive (f_{SCL}=0Hz); CLKOUT Disabled; T_{amb}=25°C [2]				
		V_{DD}=5.0V		400	600	nA
		V_{DD}=3.0V		250	500	nA
		Interface Inactive (f_{SCL}=0Hz); CLKOUT Disabled; T_{amb}=-40°C to +85°C [2]				
		V_{DD}=5.0V		500	700	nA
		V_{DD}=3.0V		400	600	nA
Inputs						
Low-level Input Voltage	V_{IL}		V_{SS}		0.3V_{DD}	V
High-level Input Voltage	V_{IH}		0.7V_{DD}		V_{DD}	V
Input Leakage Current	I_{LI}	V_I=V_{DD} or V_{SS}	-1	0	1	μA
Input Capacitance	C_i				7	pF
Outputs						
LOW-level output current	I_{OL}	Output Sink Current; V_{OL}=0.4V; V_{DD}=5V				
		on pin SDA	3			mA
		on pin $\overline{INT}$	1			mA
		on pin CLKOUT	1			mA
Output Leakage Current	I_{LO}	V_O=V_{DD} or V_{SS}	-1	0	1	μA

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Voltage Detector						
Low Voltage	V_{low}	T_{amb}=25°C; sets bit VL		0.9	1	V

[1] For reliable oscillator start-up at power-up: $V_{DD(min)power-up}=V_{DD(min)}$ + 0.3V.

[2] Timer source clock = 1/60 Hz, level of pins SCL and SDA is V_{DD} or V_{SS}.

9.Static Characteristics

V_{DD}=1.0V to 5.5V; V_{SS}=0V; T_{amb}=-40°C to +85°C; f_{osc}=32.768kHz; quartz R_S=40kΩ; C_L=8pF; unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Oscillator						
Capacitance on pin OSCO	C_{OSCO}		15	25	35	pF
	$\Delta f_{osc}/f_{osc}$	ΔV_{DD}=200mV; T_{amb}=25°C		0.2		ppm
Quartz crystal parameters (f=32.768 kHz)						
Series resistance	R_S				100	KΩ
Load capacitance	C_L	parallel	7[1]		12.5	pF
Trimmer capacitance	C_{trim}	external; on pin OSCI	5		25	pF
CLKOUT output						
Duty cycle on pin CLKOUT	δ_{CLKOUT}			50		%
I²C-bus timing characteristics						
SCL clock frequency	f_{SCL}				400	kHz
Hold time (repeated) START condition	$t_{HD;STA}$		0.6			μs
set-up time for a repeated START condition	$t_{SU;STA}$		0.6			μs
LOW period of the SCL clock	t_{LOW}		1.3			μs
HIGH period of the SCL clock	t_{HIGH}		0.6			μs
Rise time of both SDA and SCL signals	t_r					
		standard-mode			1	μs
		fast-mode			0.3	μs
Fall time of both SDA and SCL signals	t_f				03	μs
Bus free time between a STOP and START condition	t_{BUF}		1.3			μs
Capacitive load for each bus line	C_b				400	pF
Data set-up time	$t_{SU;DAT}$		100			ns
Data hold time	$t_{HD;DAT}$		0			ns

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Set-up time for STOP condition	$t_{SU;STO}$		0.6			μs
Spike pulse width	$t_{w(spike)}$	on bus			50	ns

[1] C_L is a calculation of C_{trim} and C_{OSCO} in series: $C_L = \frac{C_{trim} \cdot C_{OSCO}}{C_{trim} + C_{OSCO}}$

[2] Unspecified for f_{CLKOUT} = 32.768 kHz.

[3] All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

[4] I²C-bus access time between two STARTs or between a START and a STOP condition to this device must be less than one second.

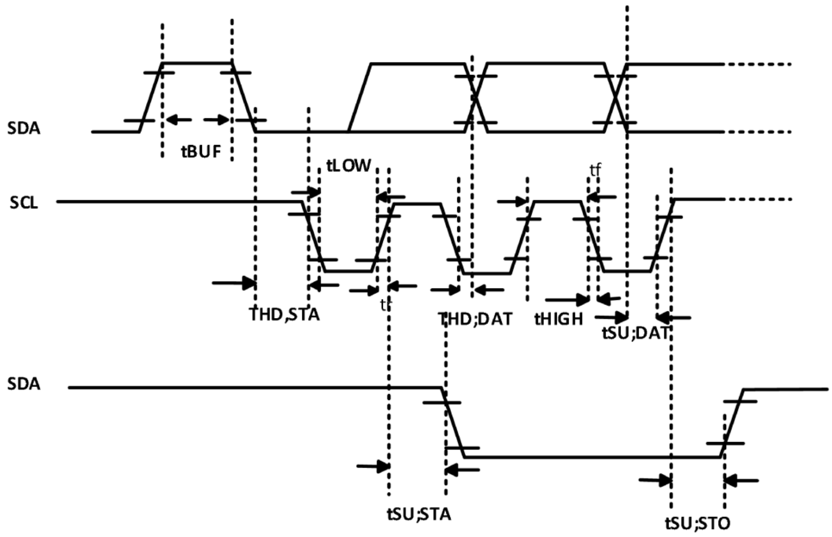


Figure 3. I²C-bus timing waveforms

10.Situation of Application

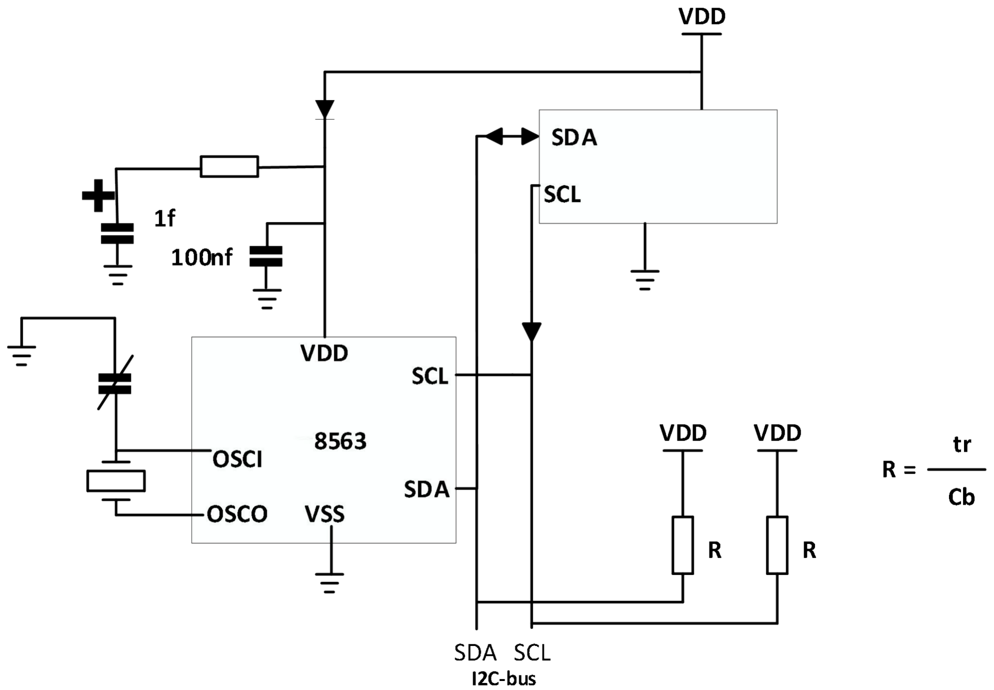


Figure 4. Application diagram

11.Functional Description

The PCF8563 contains sixteen 8-bit registers with an auto-incrementing register address, an on-chip 32.768 kHz oscillator with one integrated capacitor, a frequency divider which provides the source clock for the Real-Time Clock (RTC) and calender, a programmable clock output, a timer, an alarm, a voltage-low detector, and a 400 kHz I^2C-bus interface.

All 16 registers are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00h and 01h) are used as control and/or status registers. The memory addresses 02h through 08h are used as counters for the clock function (seconds up to years counters). Address locations 09h through 0Ch contain alarm registers which define the conditions for an alarm.

Address 0Dh controls the CLKOUT output frequency. 0Eh and 0Fh are the Timer_control and Timer registers, respectively.

The Seconds, Minutes, Hours, Days, Months, Years as well as the Minute_alarm, Hour_alarm, and Day_alarm registers are all coded in Binary Coded Decimal (BCD) format.

When one of the RTC registers is written or read, the contents of all time counters are frozen. Therefore, faulty writing or reading of the clock and calendar during a carry condition is prevented.

11.1 CLKOUT Output

A programmable square wave is available at the CLKOUT pin. Operation is controlled by the register CLKOUT_control at address 0Dh. Frequencies of 32.768 kHz (default), 1.024 kHz, 32 Hz, and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator. CLKOUT is an open-drain output and enabled at power-on. If disabled it becomes high-impedance.

11.2 Register Organization

Table 2. Formatted registers overview

Address	Register Name	BIT							
		7	6	5	4	3	2	1	0
Control and status registers									
00h	Control_status_1	TEST1	N	STOP	N	TESTC	N	N	N
01h	Control_status_2	N	N	N	TI_TP	AF	TF	AIE	TIE
Time and date registers									
02h	VL_seconds	VL	SECONDS (0 to 59)						
03h	Minutes	x	MINUTES (0 to 59)						
04h	Hours	x	x	HOURS (0 to 23)					
05h	Days	x	x	DAYS (1 to 31)					
06h	Weekdays	x	x	x	x	x	WEEKDAYS (0 to 6)		
07h	Century_months	C	x	x	MONTHS (1 to 12)				
08h	Years	YEARS (0 to 99)							
Alarm registers									
09h	Minute_alarm	AE_M	MINUTE_ALARM (0 to 59)						
0Ah	Hour_alarm	AE_H	x	HOUR_ALARM (0 to 23)					
0Bh	Day_alarm	AE_D	x	DAY_ALARM (1 to 31)					
0Ch	Weekday_alarm	AE_W	x	x	x	x	WEEKDAY_ALARM (0 to 6)		

Address	Register Name	BIT							
		7	6	5	4	3	2	1	0
CLKOUT control register									
0Dh	CLKOUT_control	FE	x	x	x	x	x	FD[1:0]	
Timer registers									
0Eh	Timer_control	TE	x	x	x	x	x	TD[1:0]	
0Fh	Timer	TIMER[7:0]							

Bit positions labelled as x are not relevant. Bit positions labelled with N should always be written with logic 0; if read they could be either logic 0 or logic 1. After reset, all registers are set according to Table 2.

11.3 Control registers

11.3.1 Register Control_status_1

Table 3. Control_status_1 - control and status register 1 (address 00h) bit description

BIT	Symbol	Value	Description
7	TEST1	default 0	normal mode, must be set to logic 0 during normal operations
		1	EXT_CLK test mode
6	N	0[1]	unused
5	STOP	default 0	RTC source clock runs
		1	all RTC divider chain flip-flops are asynchronously set to logic 0; the RTC clock is stopped (CLKOUT at 32.768 kHz is still available)
4	N	0[1]	unused
3	TESTC	0	Power-On Reset (POR) override facility is disabled; set to logic 0 for normal operation
		default 1	Power-On Reset (POR) override may be enabled
2 to 0	N	000[1]	unused

[1] Bits labeled as N should always be written with logic 0.

11.3.2 Register Control_status_2

Table 4. Control_status_2 - control and status register 2 (address 01h) bit description

BIT	Symbol	Value	Description
7 to 5	N	000[1]	unused
4	TI_TP	default 0	INT is active when TF is active (subject to the status of TIE)
		1	$\overline{INT}$ pulses active according to Table 4 (subject to the status of TIE); Remark: note that if AF and AIE are active then $\overline{INT}$ will be permanently active
3	AF	default 0	read: alarm flag inactive
			write: alarm flag is cleared
		1	read: alamm flag active
			write: alarm flag remains unchanged
2	TF	default 0	read: alarm flag inactive
			write: alarm flag is cleared
		1	read: alarm flag active
			write: alarm flag remains unchanged
1	AIE	default 0	alarm interrupt disabled
		1	alarm interrupt enabled
0	TIE	default 0	timer interrupt disabled
		1	timer interrupt enabled

[1] Bits labeled as N should always be written with logic 0.

11.3.2.1 Interrupt output

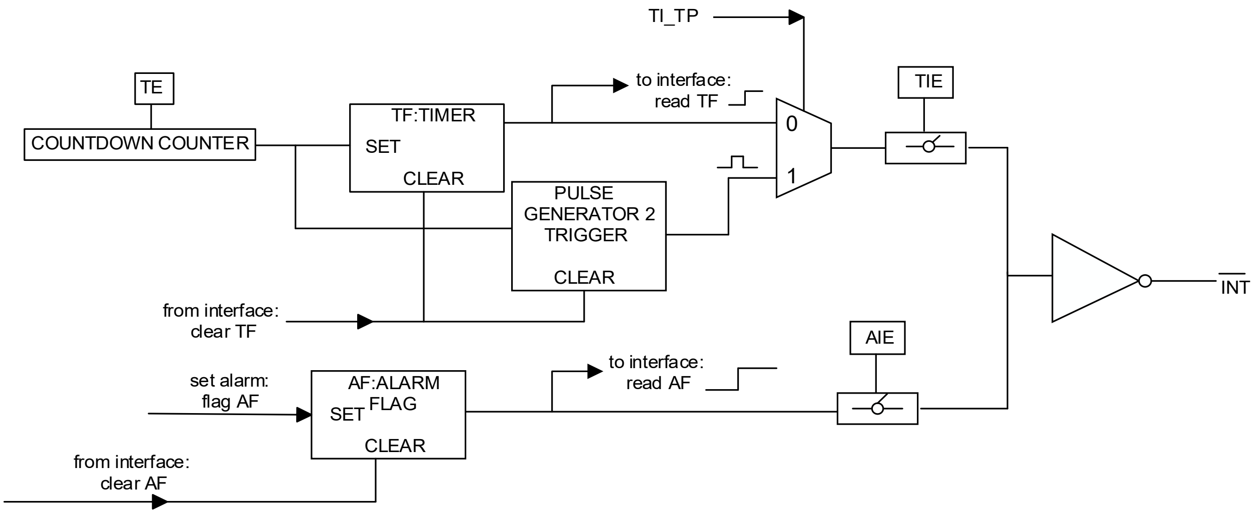


Figure 5. Interrupt scheme

Bits TF and AF: When an alarm occurs, AF is set to logic 1. Similarly, at the end of a timer countdown, TF is set to logic 1. These bits maintain their value until overwritten using the interface. If both timer and alarm interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another, a logic AND is performed during a write access.

Bits TIE and AIE: These bits activate or deactivate the generation of an interrupt when TF or AF is asserted, respectively. The interrupt is the logical OR of these two conditions when both AIE and TIE are set.

Countdown timer interrupts: The pulse generator for the countdown timer interrupt uses an internal clock and is dependent on the selected source clock for the countdown timer and on the countdown value n. As a consequence, the width of the interrupt pulse varies.

Table 5. $\overline{\text{INT}}$ operation (bit TI_TP = 1)[1]

Source Clock (Hz)	$\overline{\text{INT}}$ Period (s)	
	n = 1[2]	n > 1[2]
4096	1/8192	1/4096
64	1/128	1/64
1	1/64	1/64
1/60	1/64	1/64

[1] TF and $\overline{\text{INT}}$ become active simultaneously.

[2] n = loaded countdown value. Timer stops when n = 0.

11.4 Time and Date Registers

The majority of the registers are coded in the BCD format to simplify application use.

11.4.1 Register VL_seconds

Table 6. VL_seconds - seconds and clock integrity status register (address 02h) bit description

BIT	Symbol	Value	Place Value	Description
7	VL	0	-	clock integrity is guaranteed
		1 (Start-up value)	-	integrity of the clock information is not guaranteed
6 to 4	SECONDS	0 to 5	ten's place	actual seconds coded in BCD format, see Table 7
3 to 0		0 to 9	unit place	

Table 7. Seconds coded in BCD format

Seconds Value (decimal)	UPPER-DIGIT (ten's place)			DIGIT (unit place)			
	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00	0	0	0	0	0	0	0
01	0	0	0	0	0	0	1
02	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:
09	0	0	0	1	0	0	1
10	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:
58	1	0	1	1	0	0	0
59	1	0	1	1	0	0	1

11.4.1.1 Voltage-low Detector and Clock Monitor

The PCF8563 has an on-chip voltage-low detector (see Figure 6). When VDD drops below Vlow, bit VL in the VL_seconds register is set to indicate that the integrity of the clock information is no longer guaranteed. The VL flag can only be cleared by using the interface.

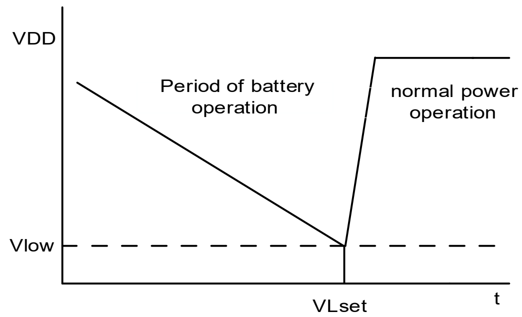


Figure 6. Voltage-low detection

The VL flag is intended to detect the situation when VDD is decreasing slowly, for example under battery operation. Should the oscillator stop or VDD reach Vlow before power is re-asserted, then the VL flag is set. This will indicate that the time may be corrupted.

11.4.2 Register Minutes

Table 8. Minutes - minutes register (address 03h) bit description

BIT	Symbol	Value	Place Value	Description
7	-	-	-	unused
6 to 4	MINUTES	0 to 5	ten's place	actual minutes coded in BCD format
3 to 0		0 to 9	unit place	

11.4.3 Register Hours

Table 9. Hours - hours register (address 04h) bit description

BIT	Symbol	Value	Place Value	Description
7 to 6	-	-	-	unused
5 to 4	HOURS	0 to 2	ten's place	actual hours coded in BCD format
3 to 0		0 to 9	unit place	

11.4.4 Register Days

Table 10. Days - days register (address 05h) bit description

BIT	Symbol	Value	Place Value	Description
7 to 6	-	-	-	unused
5 to 4	DAYS[1]	0 to 3	ten's place	actual day coded in BCD format
3 to 0		0 to 9	unit place	

[1] The PCF8563 compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.

11.4.5 Register Weekdays

Table 11. Weekdays - weekdays register (address 06h) bit description

BIT	Symbol	Value	Description
7 to 3	-	-	unused
2 to 0	WEEKDAYS	0 to 6	actual weekday values, see Table 12

Table 12. Weekday assignments

DAY[1]	BIT		
	2	1	0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

[1] Definition may be re-assigned by the user.

11.4.6 Register Century_months

Table 13. Century_months - century flag and months register (address 07h) bit description

BIT	Symbol	Value	Place Value	Description
7	C[1]	0[2]	-	indicates the century is x
		1	-	indicates the century is x+1
6 to 5	-	-	-	unused
4	MONTHS	0 to 1	ten's place	actual month coded in BCD format, see Table 14
3 to 0		0 to 9	unit place	

[1] This bit may be re-assigned by the user.

[2] This bit is toggled when the register Years overflows from 99 to 00.

Table 14. Month assignments in BCD format

MONTH	Upper-Digit (ten's place)	DIGIT (unit place)			
	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

11.4.7 Register Years

Table 15. Years - years register (08h) bit description

BIT	Symbol	Value	Place Value	Description
7 to 4	YEARS	0 to 9	ten's place	actual year coded in BCD format[1]
3 to 0		0 to 9	unit place	

[1] When the register Years overflows from 99 to 00, the century bit C in the register Century_months is toggled.

11.5 Setting and Reading The Time

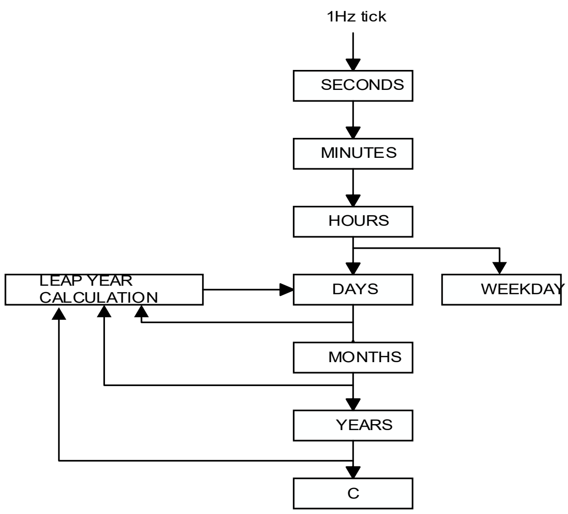


Figure 7. Data flow for the time function

Shows the data flow and data dependencies starting from the 1 Hz clock tick.

During read/write operations, the time counting circuits (memory locations 02h through 08h) are blocked.

This prevents faulty reading of the clock and calendar during a carry condition and incrementing the time registers, during the read cycle.

After this read/write access is completed, the time circuit is released again and any pending request to increment the time counters that occurred during the read access is serviced. A maximum of 1 request can be stored; therefore, all accesses must be completed within 1 second.

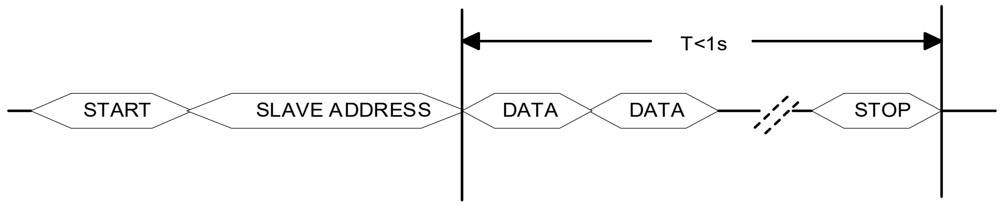


Figure 8. Access time for read/write operations

As a consequence of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time may increment between the two accesses. A similar problem exists when reading. A roll over may occur between reads thus giving the minutes from one moment and the hours from the next.

Recommended method for reading the time:

1. Send a START condition and the slave address for write (A2h).
2. Set the address pointer to 2 (VL_seconds) by sending 02h.
3. Send a RESTART condition or STOP followed by START.
4. Send the slave address for read (A3h).
5. Read VL_seconds.
6. Read Minutes.
7. Read Hours.
8. Read Days.
9. Read Weekdays.
10. Read Century_months.
11. Read Years.
12. Send a STOP condition.

11.6 Alarm Registers

11.6.1 Register Minute_alarm

Table 16. Minute_alarm - minute alarm register (address 09h) bit description

BIT	Symbol	Value	Place Value	Description
7	AE_M	0	-	minute alarm is enabled
		default 1	-	minute alarm is disabled
6 to 4	MONTHS	0 to 5	ten's place	minute alarm information coded in BCD format
3 to 0		0 to 9	unit place	

11.6.2 Register Hour_alarm

Table 17. Hour_alarm - hour alarm register (address 0Ah) bit description

BIT	Symbol	Value	Place Value	Description
7	AE_H	0	-	hour alarm is enabled
		default 1	-	hour alarm is disabled
6	-	-	-	unused
5 to 4	HOUR_ALARM	0 to 2	ten's place	hour alarm information coded in BCD format
3 to 0		0 to 9	unit place	

11.6.3 Register Day_alarm

Table 17. Hour_alarm - hour alarm register (address 0Ah) bit description

BIT	Symbol	Value	Place Value	Description
7	AE_H	0	-	day alarm is enabled
		default 1	-	day alarm is disabled
6	-	-	-	unused
5 to 4	DAY_ALARM	0 to 3	ten's place	day alarm information coded in BCD format
3 to 0		0 to 9	unit place	

11.6.4 Register Weekday_alarm

Table 19. Weekday_alarm - weekday alarm register (address 0Ch) bit description

BIT	Symbol	Value	Description
7	AE_W	0	weekday alarm is enabled
		default 1	weekday alarm is disabled
6 to 3	-	-	unused
2 to 0	WEEKDAY_ALARM	0 to 6	weekday alarm information coded in BCD format

11.6.5 Alarm Flag

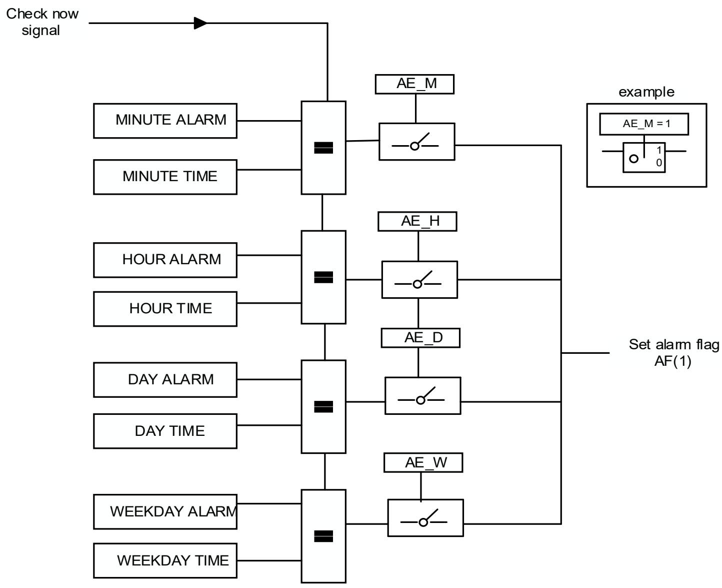


Figure 9. Alarm function block diagram

Only when all enabled alarm settings are matching. It's only on increment to a matched case that the alarm flag is set.

By clearing the alarm enable bit (AE_x) of one or more of the alarm registers, the corresponding alarm condition(s) are active. When an alarm occurs, AF is set to logic 1. The asserted AF can be used to generate an interrupt (INT). The AF is cleared using the interface.

The registers at addresses 09h through 0Ch contain alarm information. When one or more of these registers is loaded with minute, hour, day or weekday, and its corresponding AE_x is logic 0, then that information is compared with the current minute, hour, day, and weekday. When all enabled comparisons first match, the alarm flag (AF in register Control_2) is set to logic 1.

The generation of interrupts from the alarm function is controlled via bit AIE. If bit AIE is enabled, the $\overline{\text{INT}}$ pin follows the condition of bit AF. AF will remain set until cleared by the interface. Once AF has been cleared, it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their AE_x bit at logic 1 are ignored.

11.7 Register CLKOUT_control and Clock Output

Frequencies of 32.768 kHz (default), 1.024 kHz, 32 Hz, and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

Table 20. CLKOUT_control - CLKOUT control register (address 0Dh) bit description

BIT	Symbol	Value	Description
7	FE	0	the CLKOUT output is inhibited and CLKOUT output is set high-impedance
		default 1	the CLKOUT output is activated
6 to 2	-	-	unused
1 to 0	FD[1:0]		frequency output at pin CLKOUT
		00	32.768kHz
		01	1.024kHz
		10	32Hz
		11	1Hz

11.8 Timer Function

The 8-bit countdown timer at address 0Fh is controlled by the Timer_control register at address 0Eh. The Timer_control register determines one of 4 source clock frequencies for the timer (4.096 Hz, 64 Hz, 1 Hz, or 1⁄60 Hz), and enables or disables the timer. The timer counts down from a software-loaded 8-bit binary value. At the end of every countdown, the timer sets the timer flag TF. The TF may only be cleared by using the interface. The asserted TF can be used to generate an interrupt on pin INT. The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the state of TF. Bit TI_TP is used to control this mode selection. When reading the timer, the current countdown value is returned.

11.8.1 Register Timer_control

Table 21. Timer_control - timer control register (address 0Eh) bit description

BIT	Symbol	Value	Description
7	TE	0[1]	timer is disabled
		1	timer is enabled
6 to 2	-	-	unused
1 to 0	TD[1:0]		timer source clock frequency select[2]
		00	4.096kHz
		01	64Hz
		10	1Hz
		11[2]	1/60Hz

[1] Default value.

[2] These bits determine the source clock for the countdown timer; when not in use, TD[1:0] should be set to 1⁄60Hz for power saving.

11.8.2 Register Timer

Table 22. Timer - timer value register (address 0Fh) bit description

BIT	Symbol	Value	Description
7 to 0	TIMER[7:0]	00h to FFh	countdown period in seconds: $\text{CountdownPeriod} = \frac{n}{\text{SourCeCloCkFrequenCy}}$
where n is the countdown value			

Table 23. Timer register bits value range-

BIT							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
128	64	32	16	8	4	2	1

The register Timer is an 8-bit binary countdown timer. It is enabled and disabled via the Timer_control register bit TE. The source clock for the timer is also selected by the Timer_control register. Other timer properties such as interrupt generation are controlled via the register Control_status_2.

For accurate read back of the count down value, it is recommended to read the register twice and check for consistent results, since it is not possible to freeze the countdown timer counter during read back.

11.9 EXT_CLK Test Mode

A test mode is available which allows for on-board testing. In such a mode it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bit TEST1 in register Control_status_1. Then pin CLKOUT becomes an input. The test mode replaces the internal 64 Hz signal with the signal applied to pin CLKOUT. Every 64 positive edges applied to pin CLKOUT will then generate an increment of one second.

The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a maximum period of 1000 ns. The internal 64 Hz clock, now sourced from CLKOUT, is divided down to 1 Hz by a 26 divide chain called a prescaler. The prescaler can be set into a known state by using bit STOP. When bit STOP is set, the prescaler is reset to 0 (STOP must be cleared before the prescaler can operate again).

Entry into EXT_CLK test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

11.9.1 Operation Example:

1. Set EXT_CLK test mode (Control_status_1, bit TEST1 = 1).
2. Set STOP (Control_status_1, bit STOP = 1).
3. Clear STOP (Control_status_1, bit STOP = 0).
4. Set time registers to desired value.
5. Apply 64 clock pulses to CLKOUT.
6. Read time registers to see the first change.
7. Apply 64 clock pulses to CLKOUT.
8. Read time registers to see the second change.

Repeat steps 7 and 8 for additional increments.

11.10 STOP Bit Function

The function of the STOP bit is to allow for accurate starting of the time circuits. The STOP bit function will cause the upper part of the prescaler (F_3 to F_{14}) to be held in reset and thus no 1 Hz ticks will be generated (see Figure 10). The time circuits can then be set and will not increment until the STOP bit is released (see Figure 11). The STOP bit function will not affect the output of 32.768 kHz on CLKOUT, but will stop the generation of 1.024 kHz, 32 Hz, and 1 Hz.

The lower three stages of the prescaler (F0 and F1 and F3) are not reset; and because the I²C-bus is asynchronous to the crystal oscillator, the accuracy of re-starting the time circuits will be between zero and one 4096 Hz cycle (see Figure 11).

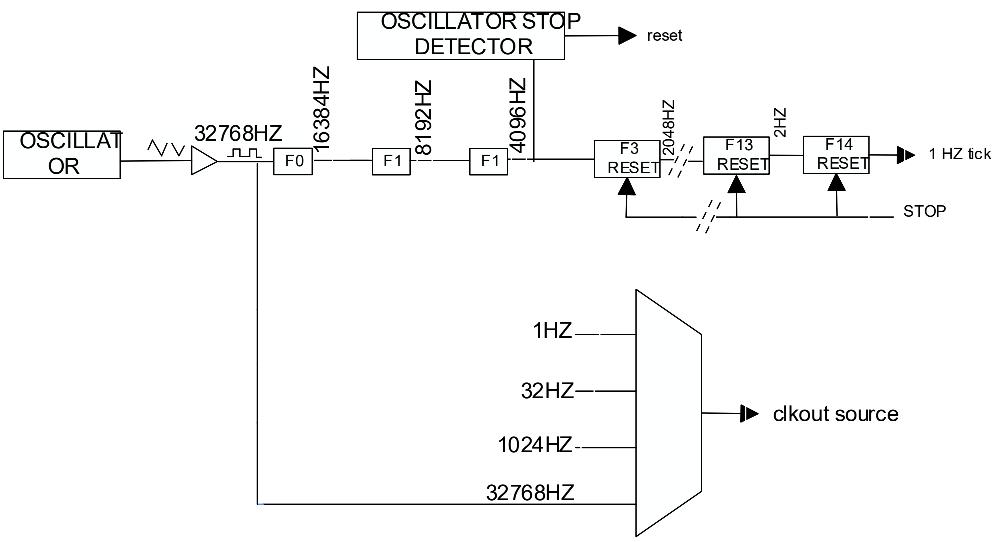


Figure 10. STOP bit functional diagram

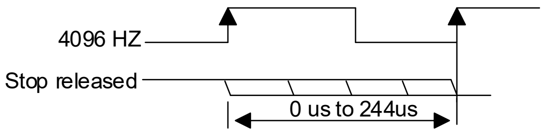


Figure 11. STOP bit release timing

11.11 Reset

The PCF8563 includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state the I²C-bus logic is initialized including the address pointer and all registers are set according to Table 25. I²C-bus communication is not possible during reset.

Table 25. Register reset value [1]

Address	Register Name	Register Name							
		7	6	5	4	3	2	1	0
00h	Control_status_1	0	0	0	0	1	0	0	0
01h	Control_status_2	0	0	0	0	0	0	0	0
02h	VL_seconds	1	x	x	x	x	x	x	x
03h	Minutes	x	x	x	x	x	x	x	x
04h	Hours	x	x	x	x	x	x	x	x
05h	Days	x	x	x	x	x	x	x	x
06h	Weekdays	x	x	x	x	x	x	x	x
07h	Century_months	x	x	x	x	x	x	x	x
08h	Years	x	x	x	x	x	x	x	x
09h	Minute_alarm	1	x	x	x	x	x	x	x
0Ah	Hour_alarm	1	x	x	x	x	x	x	x
0Bh	Day_alarm	1	x	x	x	x	x	x	x
0Ch	Weekday_alarm	1	x	x	x	x	x	x	x
0Dh	CLKOUT_control	1	x	x	x	x	x	0	0
0Eh	Timer_control	0	x	x	x	x	x	1	1
0Fh	Timer	x	x	x	x	x	x	x	x

[1] Registers marked x are undefined at power-up and unchanged by subsequent resets.

12.Characteristics of The I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

12.1 Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Figure 12).

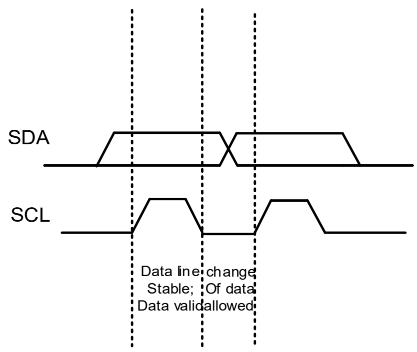


Figure 12. Bit transfer

12.2 START and STOP Conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P (see Figure 13).

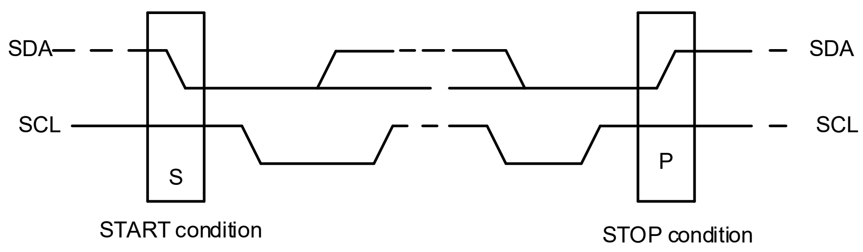


Figure 13. Definition of START and STOP conditions

12.3 System Configuration

A device generating a message is a transmitter; a device receiving a message is a receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves (see Figure 14).

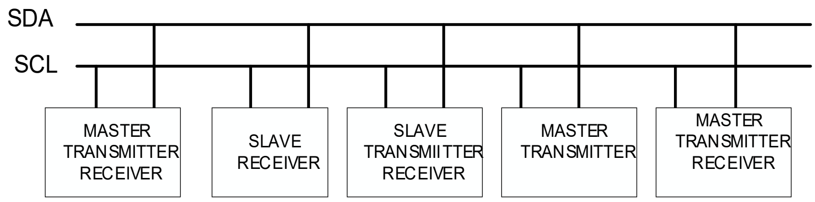


Figure 14. System configuration

12.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I^{2}C-bus is illustrated in Figure 15.

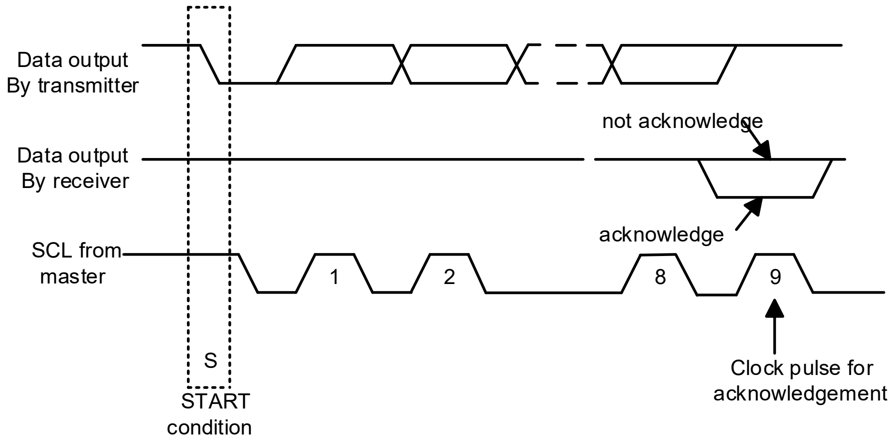


Figure 15. Acknowledgement on the I²C-bus

12.5 I²C-bus Protocol

12.5.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The PCF8563 acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

Two slave addresses are reserved for the PCF8563:

Read: A3h (10100011)

Write: A2h (10100010)

The PCF8563 slave address is illustrated in Figure 16.

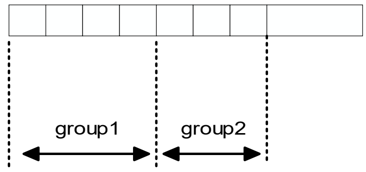


Figure 16. Slave address

12.5.2 Clock and Calendar READ or WRITE Cycles

The I²C-bus configuration for the different PCF8563 READ and WRITE cycles is shown in Figure 17, Figure 18 and Figure 19. The register address is a 4-bit value that defines which register is to be accessed next. The upper four bits of the register address are not used.

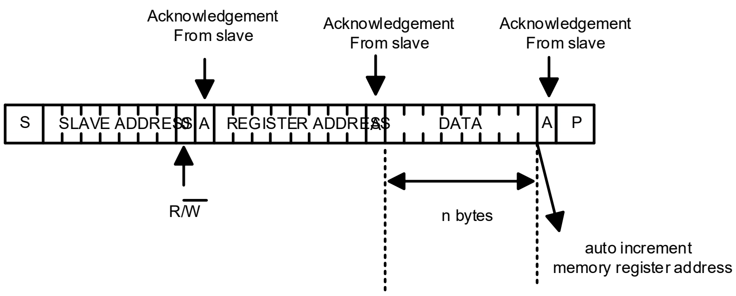


Figure 17. Master transmits to slave receiver (WRITE mode)

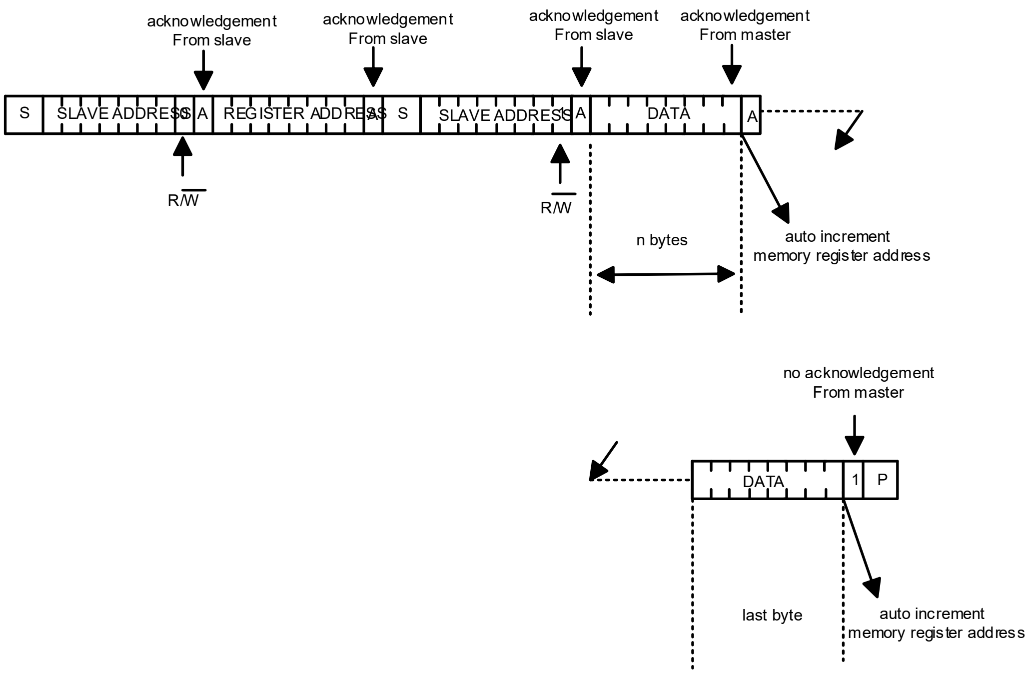


Figure 18. Master reads after setting register address (write register address; READ data)

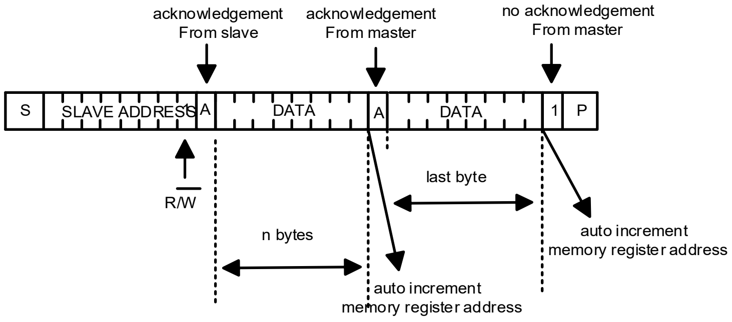


Figure 19. Master reads slave immediately after first byte (READ mode)

13.Internal Circuitry

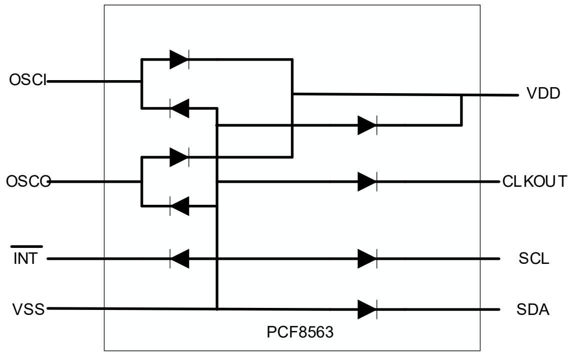


Figure 20. Device diode protection diagram

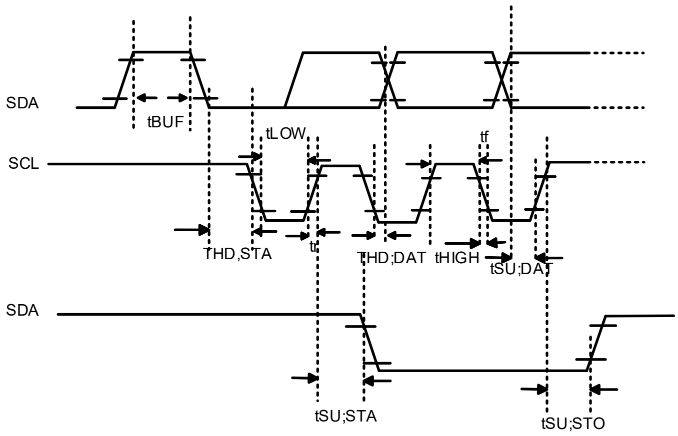
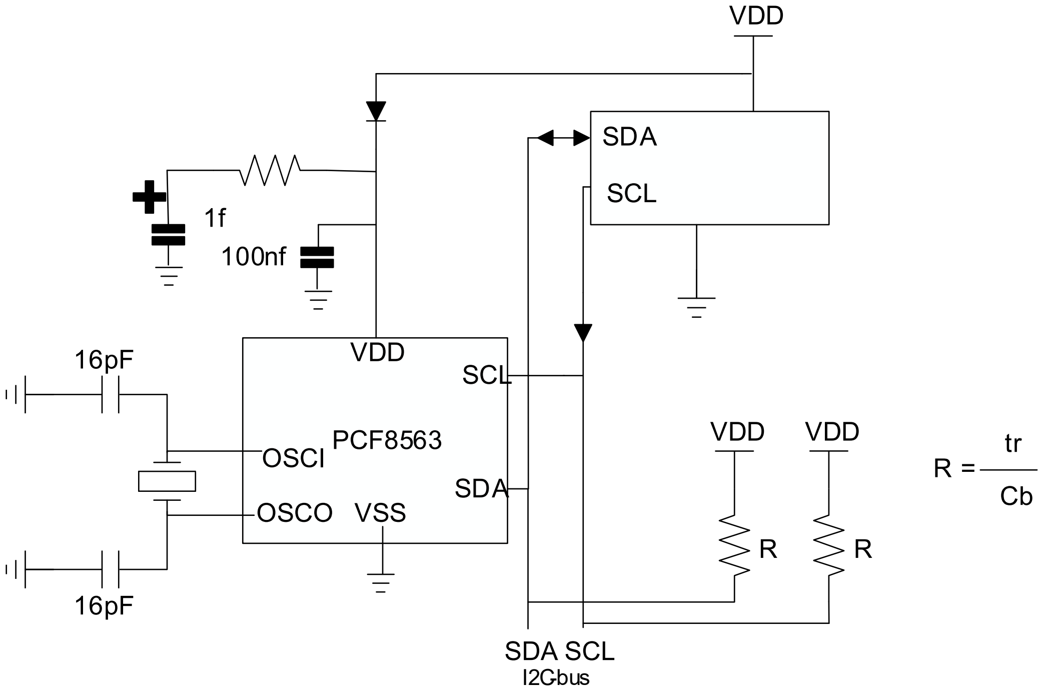
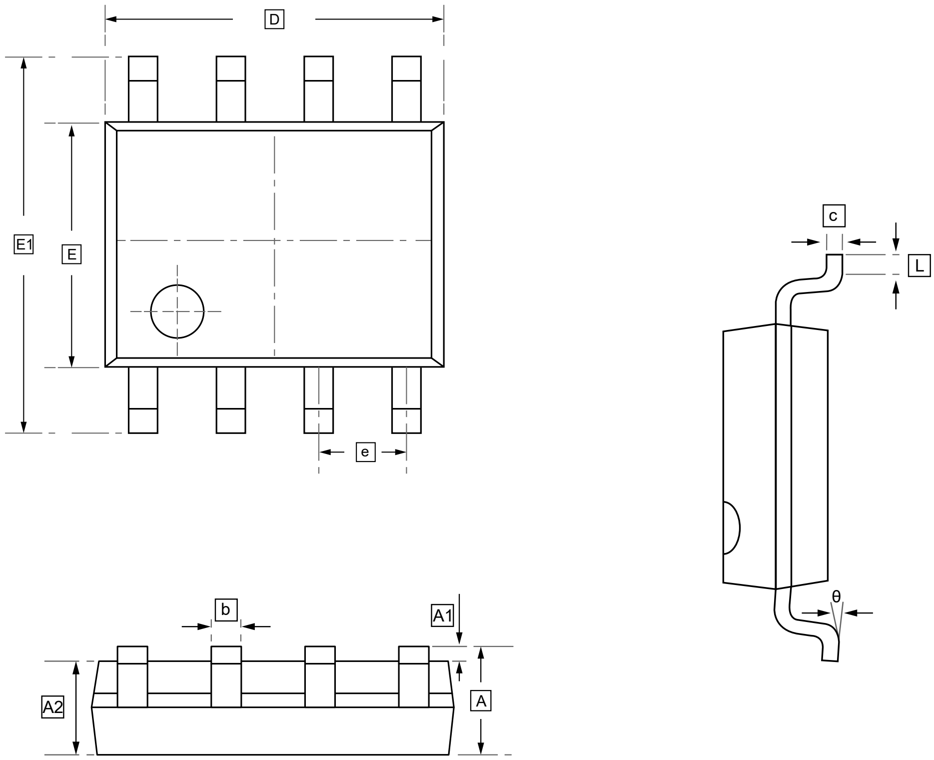


Figure 21. I²C-bus timing waveforms

14.Situation of application



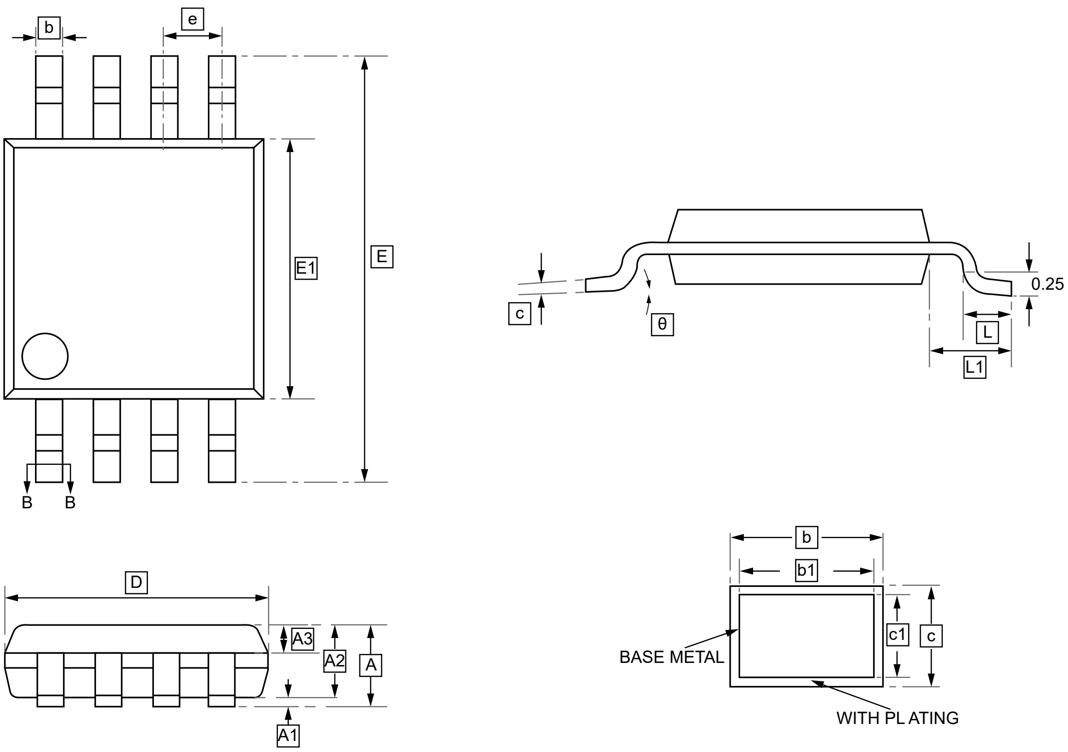
15.1 SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°

15.2 MSOP-8 Package Outline Dimensions

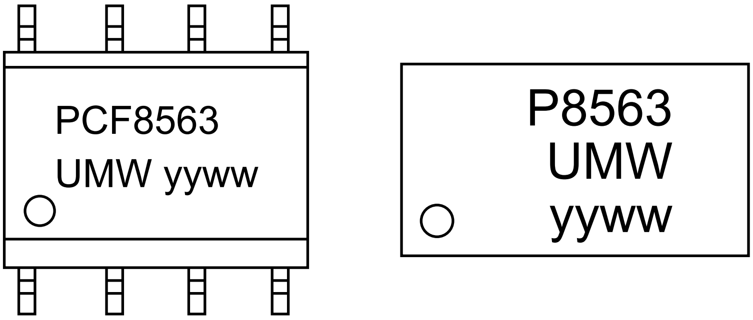


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	b1	c	c1	D	E	E1	e
Min	-	0.05	0.75	0.30	0.28	0.27	0.15	0.14	2.90	4.70	2.90	0.65
Max	1.10	0.15	0.95	0.40	0.36	0.33	0.19	0.16	3.10	5.10	3.10	BSC

Symbol	L	L1	θ
Min	0.40	0.95	0°
Max	0.70	REF	8°

16.Ordering Information



yy: Year Code
ww: Week Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW PCF8563T	PCF8563	SOP-8	4000	Tape and reel
UMW PCF8563TS	P8563	MSOP-8	4000	Tape and reel

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