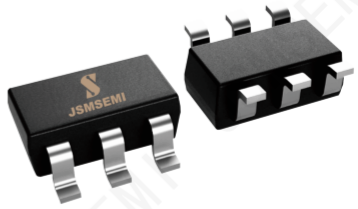
Description

The IRS10752/20752 is a high-side, single-channel gate driver IC with 100V/200V blocking and levelshifting capability. This allows for the gate driver to be connected directly to the gate of a high-side power MOSFET, while being controlled by the low-side, ground potential circuitry. The IRS10752/20752 includes a wide VCC supply range, UVLO protection, and excellent immunity to harsh dv/dt or –VS switching environments. JSMSEMI's HVIC technology allows for these functions and features to be realized in a 6-pin SOT-23 package.



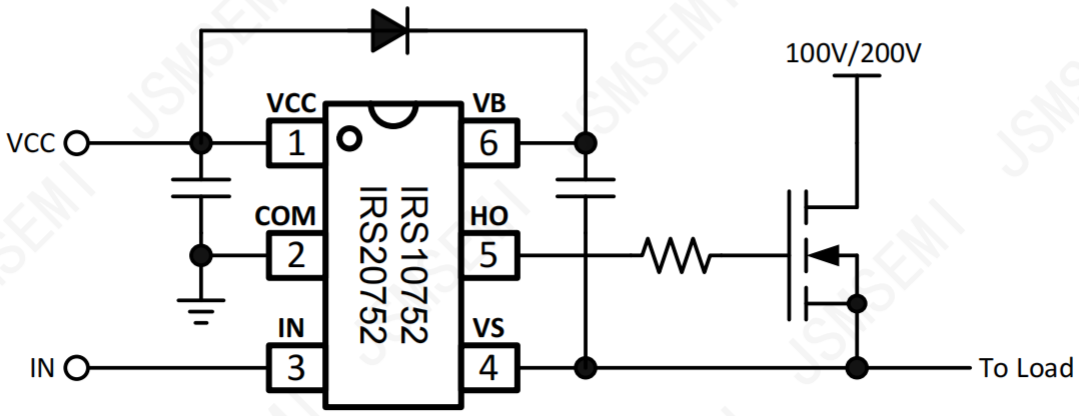
Features

- Floating gate driver designed for bootstrap operation
- Fully operational to
  IRS10752LTRPBF +100 V
  IRS20752LTRPBF +200 V
- Excellent dv/dt immunity
- Excellent negative V_S transient immunity
- Wide V_{CC} range
- UVLO on low-side and high-side
- Schmitt-trigger input with internal pull-down
- Output in phase with input
- Excellent latch immunity on all inputs & outputs
- RoHS compliant
- SOT-23-6 package

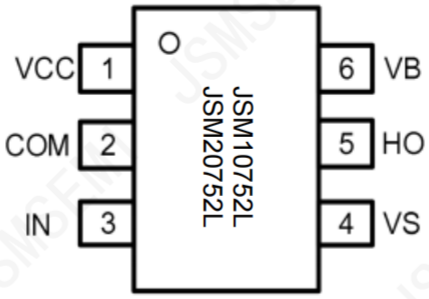
Applications

- Motor drive control
- Universal inverter
- High-side gate driver control
- Pulse transformer replacement
- General purpose switched mode power electronics

Typical Connection Diagram



Pin Assignments



Pin Definitions

Pin	Symbol	Description
1	VCC	IC supply voltage
2	COM	IC power and signal ground
3	IN	Logic input
4	VS	High side floating supply offset voltage
5	HO	High side gate driver output
6	VB	High side floating supply voltage

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship,Quantity	Green
IRS10752LTRPBF-JSM	SOT-23-6	S10I	-40 to 125°C	3	T&R,3000	Rohs
IRS20752LTRPBF-JSM	SOT-23-6	S20H	-40 to 125°C	3	T&R,3000	Rohs

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any pin. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min	Max	Units
V_B	High side floating absolute voltage		-0.3	120	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating gate drive output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{IN}	Logic input voltage		COM - 0.3	V_{CC} + 0.3	
COM	Logic ground		V_{CC} - 25	V_{CC} + 0.3	
dVS/dt	High side floating supply offset voltage slew rate		---	50	V/ns
$R\Theta_{JA}$	Thermal resistance, junction to ambient	6L-SOT-23	---	200	℃/W
T_J	Junction temperature		-55	150	℃
T_S	Storage temperature				
T_L	IC Pin temperature (soldering, 10 seconds)		---	300	

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

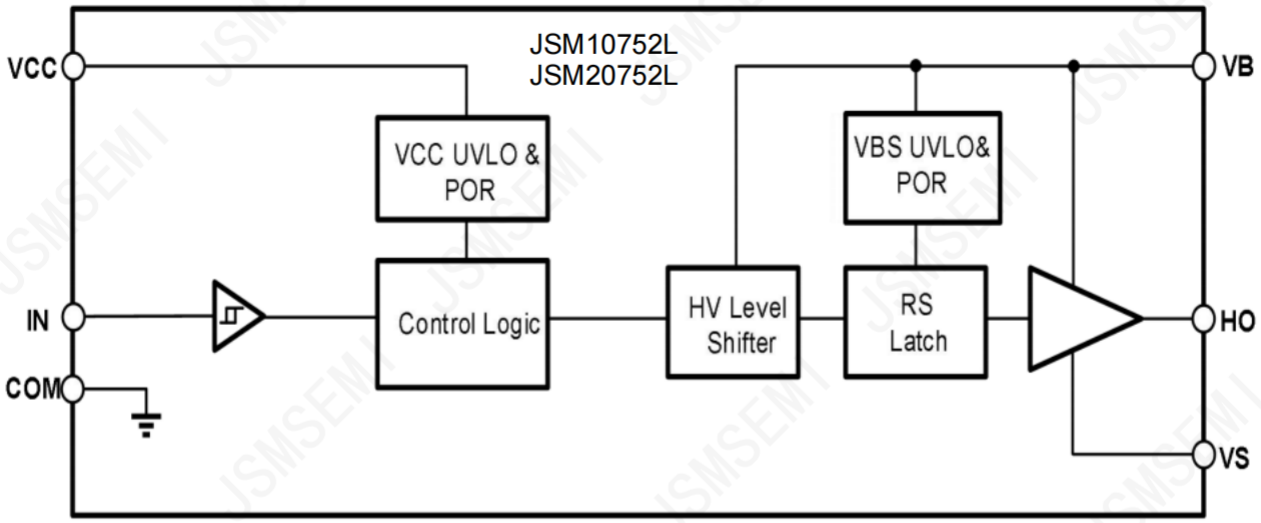
Symbol	Definition	Min	Max	Units
V_B	High side floating absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	- 9	100	
V_{HO}	High side floating gate drive output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{IN}	Logic input voltage	COM	V_{CC}	
T_J	Junction temperature	-40	125	℃

Electrical Characteristics

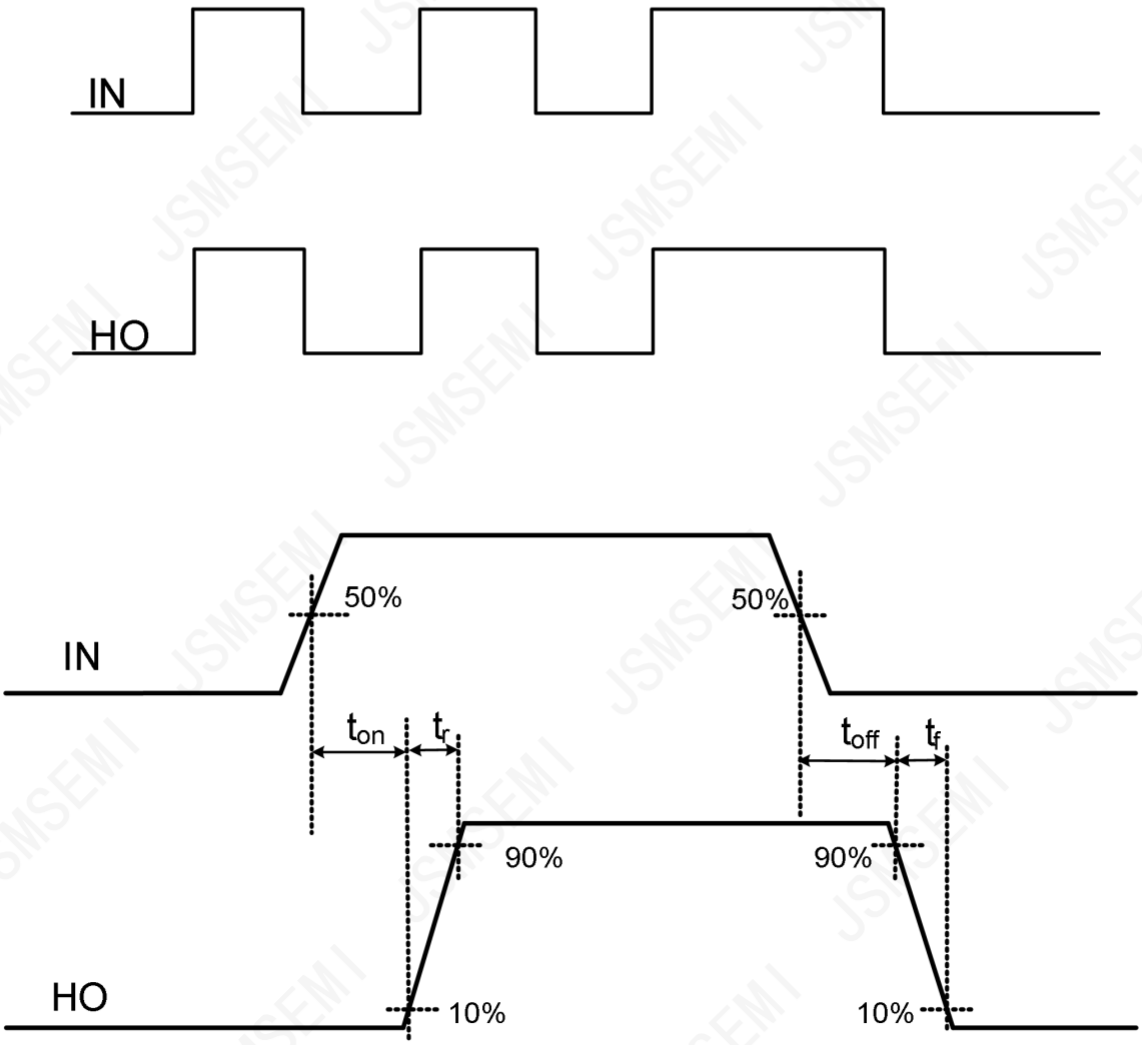
V_{CC}=V_{BS}=15V, C_L=1nF, and T_A = 25 °C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Low Side Characteristics						
V_{CCUV+}	V_{CC} supply UVLO positive-going	8.0	8.8	10.0	V	
V_{CCUV-}	V_{CC} supply UVLO negative-going	7.4	8.2	9.0		
I_{QCC}	Quiescent V_{CC} supply current	---	100	---	μA	
V_{CC_CLAMP}	V_{CC} internal Zener clamp voltage	---	20.4	---	V	I_{CC} = 5mA
V_{IH}	Logic "1" input voltage	2.5	---	---		
V_{IL}	Logic "0" input voltage	---	---	0.8		
I_{IN+}	Logic "1" input bias current	---	3	10	μA	V_{IN} = 5V
I_{IN-}	Logic "0" input bias current	---	---	5		V_{IN} = 0V
High Side Characteristics						
V_{BSUV+}	V_{BS} supply UVLO positive-going	8.0	8.8	10.0	V	
V_{BSUV-}	V_{BS} supply UVLO negative-going	7.4	8.2	9.0		
V_{BS_CLAMP}	V_{BS} internal Zener clamp voltage	---	20.4	---		I_{BS} = 5mA
V_{OH}	High level output voltage (V_B – HO)	---	0.05	0.2		I_O = 2mA
V_{OL}	Low level output voltage (HO – V_S)	---	0.02	0.1		
I_{LK}	Offset supply leakage current	---	---	50	μA	V_B = V_S = 100/200V
I_{QBS}	Quiescent V_{BS} supply current	---	---	80		V_{IN} = V_{CC} or COM
Gate Drive Characteristics						
t_{ON}	Turn-on propagation delay	---	120	---	ns	V_S = 0V
t_{OFF}	Turn-off propagation delay	---	130	---		V_S = 100V
t_{RISE}	Turn-on rise time	---	70	---		V_S = 0V
t_{FALL}	Turn-off fall time	---	30	---		
I_{O+}	HO gate drive output source current	---	290	---	mA	
I_{O-}	HO gate drive output sink current	---	600	---		

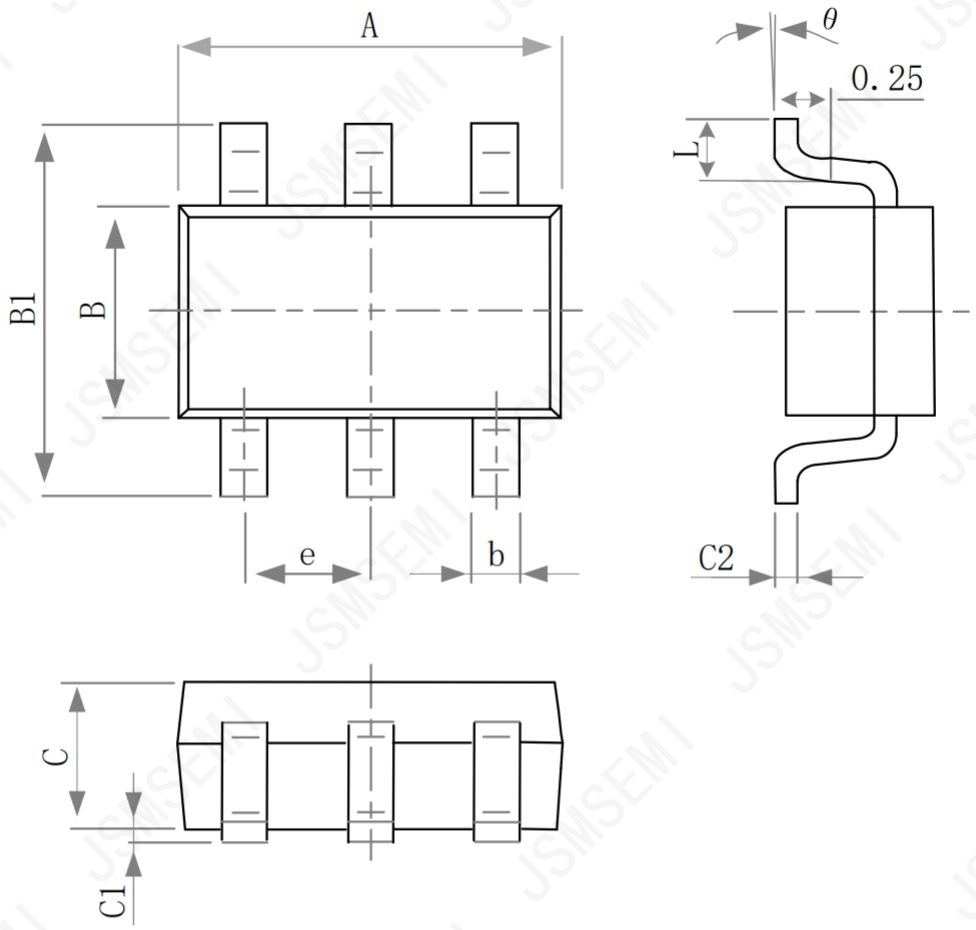
Functional Block Diagram



Timing Diagram



SOT23-6 Package Outlines



SOT23-6 Package Dimensions

尺寸 / 标注	MIN(mm)	MAX(mm)	尺寸 / 标注	MIN(mm)	MAX(mm)
A	2.82	3.02	C	1.05	1.15
e	0.95（BSC）		C1	0.03	0.15
b	0.28	0.45	C2	0.12	0.23
B	1.50	1.70	L	0.35	0.55
B1	2.60	3.00	θ	0°	8°

Revision History

Rev.	Change	Date
V1.0	Initial version	2/23/2022

Important Notice

JSMSEMI Semiconductor (JSMSEMI) PRODUCTS ARE NEITHER DESIGNED NOR INTENDED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS UNLESS THE SPECIFIC JSMSEMI PRODUCTS ARE SPECIFICALLY DESIGNATED BY JSMSEMI FOR SUCH USE. BUYERS ACKNOWLEDGE AND AGREE THAT ANY SUCH USE OF JSMSEMI PRODUCTS WHICH JSMSEMI HAS NOT DESIGNATED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS IS SOLELY AT THE BUYER’S RISK.

JSMSEMI assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using JSMSEMI products.

Resale of JSMSEMI products or services with statements diferent from or beyond the parameters stated by JSMSEMI for that product or service voids all express and any implied warranties for the associated JSMSEMI product or s ervice. JSMSEMI is not responsible or liable for any such statements.

Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc.When designing equipment, refer to the "Delivery Specification" for the JSMSEMI product that you intend to use.

For additional information please contact Kevin@jsmsemi.com or visit www.jsmsemi.com