4.1A, Brushless DC Motor Driver with Integrated Current Regulation

(compatible to DRV8251 (TI USA)

1. Feature

- N-channel H-bridge brushed DC motor driver
- 4.5V to 48V Operating Supply Voltage Range
- High Output Current Capability: 4.1-A Peak
- Low MOSFET $R_{DS(on)}$ Typical 0.5Ω(HS+LS)
- Low Power Sleep Mode
  - <1uA at VM=24V, T_J = 25°C
- PWM Control Interface
- Protection Features:
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
  - VM Undervoltage Lockout (UVLO)

2. Applications

- POS Printers
- Printers
- Washer and Dryer
- Coffee machine
- Surgical Equipment
- Fitness Machine

3. General Description

The HT8251B device is an integrated motor driver with N-channel H-bridge, charge pump, current regulation, and protection circuitry. The charge pump improves efficiency by supporting N-channel MOSFET half bridges and 100% duty cycle driving.

The HT8251B implements a current regulation feature by comparing the analog input VREF and the voltage across a current-sense shunt resistor on the ISEN pin. The ability to limit current can significantly reduce large currents during motor startup and stall conditions.

A low-power sleep mode achieves ultra-low quiescent current draw by shutting down most of the internal circuitry. Internal protection features include supply undervoltage lockout, output overcurrent, and device overtemperature.

The HT8251B is available in a 8-pin eSOP8

4. Package

Part Number	Package	Body Size
HT8251BREZ	eSOP8	4.9mm x 6.0mm

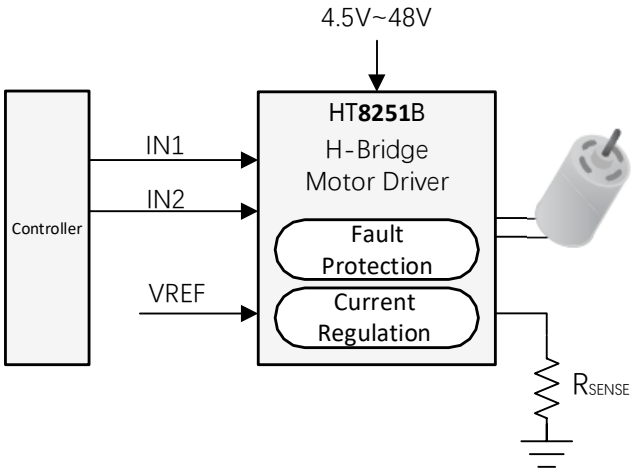
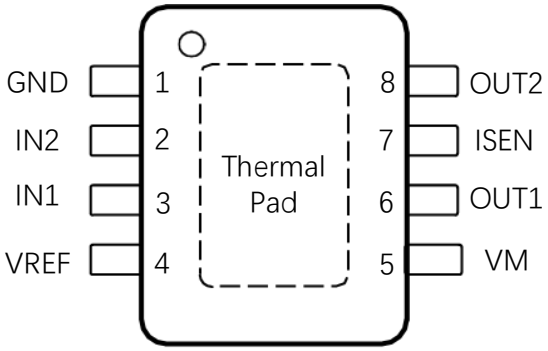


Fig.1 Block diagram of HT8251B

5. PIN Definition



8-Pin HSOP Top View

Fig.2 Pad definition of HT8251B

Table 1 Pad Functions

Pin	Name	I/O	Description
1	GND	GROUND	Logic ground. Connect to board ground
2	IN2	I	Logic inputs. Controls the H-bridge output. Has internal pulldowns
3	IN1	I	Logic inputs. Controls the H-bridge output. Has internal pulldowns
4	VREF	I	Analog input. Apply a voltage between 0 to 5 V. For information on current regulation
5	VM	POWER	4.5-V to 48-V power supply. Connect a 0.1-µF bypass capacitor to ground
6	OUT1	I	H-bridge output. Connect directly to the motor or other inductive load
7	ISEN	GROUND	High-current ground path. If using current regulation, connect ISEN to a resistor (low-value, high-power-rating) to ground. If not using current regulation, connect ISEN directly to ground
8	OUT2	I	H-bridge output. Connect directly to the motor or other inductive load

Absolute Maximum Ratings

(If out of these ratings, the filter may be fail or damaged)

Table 2

		MIN	MAX	UNIT
Power supply pin voltage	VM	-0.3	50	V
Power supply transient voltage ramp	VM	0	2	V/μs
Logic pin voltage	INx	-0.3	7	V
Reference input pin voltage	VREF	-0.3	6	V
Output pin voltage	OUTx	-0.7	VM + 0.7	V
Current sense input pin voltage	ISEN	-0.5	1	V
Output current	OUTx	Internally Limited	Internally Limited	A
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

6. Recommended Operating Conditions

Table 3

			MIN	TYP	MAX	UNIT
V_{VM}	Power supply voltage	VM	4.5		48	V
V_{VREF}	Reference voltage	VREF	0		5	V
V_{IN}	Logic input voltage	INx	0		5.5	V
f_{PWM}	PWM frequency	INx		0		200 kHz
I_{OUT}	Peak output current 4.5V≤V_{VM}<5.5V	OUTx			3.7	A
	Peak output current 5.5V≤V_{VM}				4.1	
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

7. Electrical Characteristics

Table 4

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VM)						
I_{VMQ}	VM sleep mode current	V_{VM} = 24 V, IN1 = IN2 = 0, T_J = 25°C			2	μA
I_{VM}	VM active mode current	V_{VM} = 24 V, IN1 = IN2 = 1		4	8	mA
t_{WAKE}	Turn on time	Control signal to active mode			100	μs
t_{SLEEP}	Turn off time	Control signal to sleep mode	0.8		1.5	ms
LOGIC-LEVEL INPUTS (INx)						
V_{IL}	Input logic low voltage				0.7	V
V_{IH}	Input logic high voltage		1.8			V
V_{HYS}	Input hysteresis			300		mV
I_{IL}	Input logic low current	V_{IN} = 0 V	-1		1	μA
I_{IH}	Input logic high current	V_{IN} = 3.3 V		33	100	μA
R_{PD}	Input pulldown resistance	To GND		100		kΩ
DRIVER OUTPUTS (OUTx)						
$R_{DS(on)\_HS}$	High-side MOSFET on resistance	V_{VM} = 24 V, I = 1 A, f_{PWM} = 25 kHz		225		mΩ
$R_{DS(on)\_LS}$	Low-side MOSFET on resistance	V_{VM} = 24 V, I = 1 A, f_{PWM} = 25 kHz		225		mΩ
V_{SD}	Body diode forward voltage	I_{OUT} = 1 A		0.8		V
t_{RISE}	Output rise time	V_{VM} = 24 V, OUTx rising from 10% to 90%		250		ns
t_{FALL}	Output fall time	V_{VM} = 24 V, OUTx falling from 90% to 10%		250		ns
t_{PD}	Input to output propagation delay	INx to OUTx		0.4	1	μs
t_{DEAD}	Output dead time			200		ns
SHUNT CURRENT SENSE AND REGULATION (ISEN, VREF)						
A_V	ISEN gain	VREF = 2.5 V	9.6	10	10.4	V/V
t_{OFF}	Current regulation off time			25		μs
t_{BLANK}	Current regulation blanking time			2		μs
PROTECTION CIRCUITS						
V_{UVLO}	Supply undervoltage lockout (UVLO)	Supply rising	4.15	4.4	4.65	V
		Supply falling	4.05	4.3	4.55	V
V_{UVLO_HYS}	Supply UVLO hysteresis	Rising to falling threshold		100		mV
t_{UVLO}	Supply undervoltage deglitch time			10		us
I_{OCP}		4.5V≤V_{VM}<5.5V	3.7			A
	Overcurrent protection trip point	5.5V≤V_{VM}	4.1			
t_{OCP}	Overcurrent protection deglitch time			2		μs
t_{RETRY}	Overcurrent protection retry time			3		ms

8. Detailed Description

8.1 Overview

The HT8251B is an 8-pin device for driving brushed DC motors from a 4.5-V to 48-V supply rail. Two logic inputs control the H-bridge driver, which consists of four N-channel MOSFETs that have a typical RDS(on) of 450 mΩ (including one high-side and one low-side FET). A single power input, VM, serves as both device power and the motor winding bias voltage. The integrated charge pump of the device boosts VM internally and fully enhances the high-side FETs. Motor speed can be controlled with pulse-width modulation at frequencies between 0 to 200 kHz. The device enters a low-power sleep mode by bringing both inputs low.

The HT8251B also integrates current regulation using an external shunt resistor on the ISEN pin. This allows the device to limit the output current with a fixed off-time PWM chopping scheme to limit inrush and stall currents. The current regulation level can be configured during motor operation through the VREF pin to limit the load current accordingly to the system demands.

A variety of integrated protection features protect the device in the case of a system fault. These include undervoltage lockout (UVLO), overcurrent protection (OCP), and overtemperature shutdown (TSD).

8.2 Functional Block Diagram

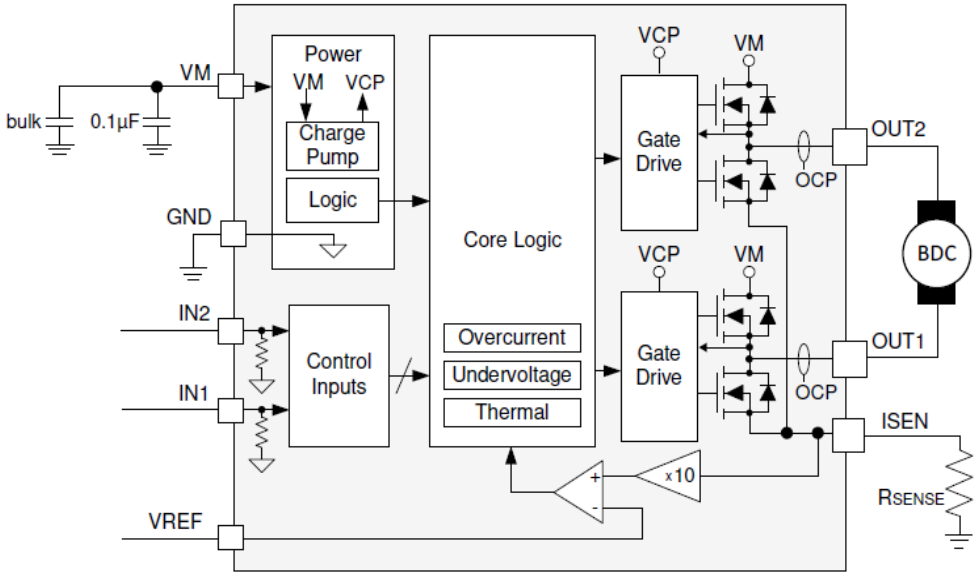


Figure 3. Function Block Diagram

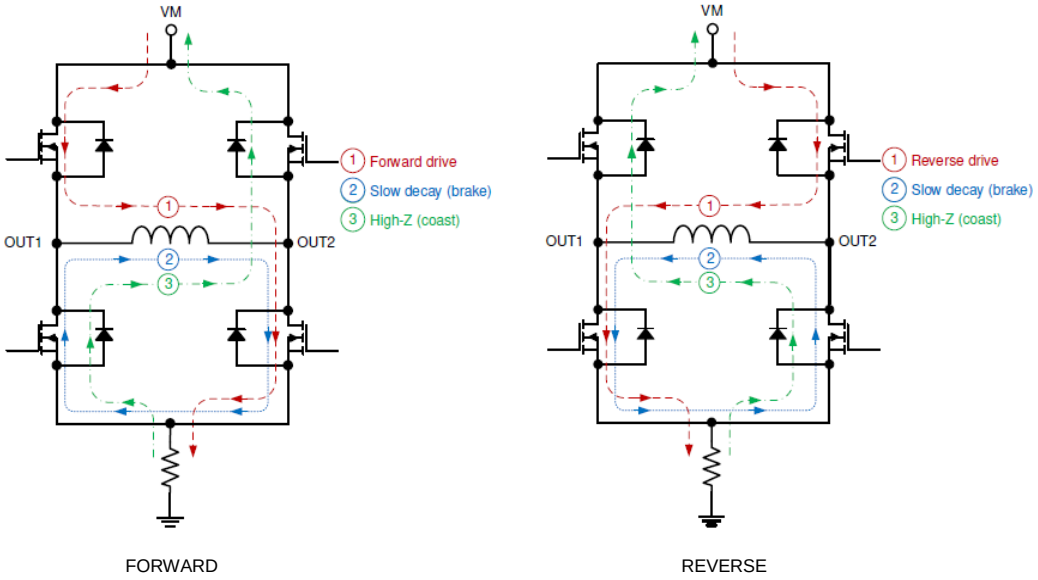
8.3 Bridge Control

The HT8251B output consists of four N-channel MOSFETs that are designed to drive high current. These outputs are controlled by the two logic inputs IN1 and IN2 as listed in table 5.

Table 5 H-Bridge Logic

IN1	IN2	OUT1	OUT2	DESCRIPTION
0	0	High-Z	High-Z	Coast; H-bridge disabled to High-Z (sleep entered after 1 ms)
0	1	L	H	Reverse (Current OUT2 → OUT1)
1	0	H	L	Forward (Current OUT1 → OUT2)
1	1	L	L	Brake; low-side slow decay

The inputs can be set to static voltages for 100% duty cycle drive, or they can be pulse-width modulated (PWM) for variable motor speed. When using PWM, switching between driving and braking typically works best. For example, to drive a motor forward with 50% of the maximum RPM, IN1 = 1 and IN2 = 0 during the driving period, and IN1 = 1 and IN2 = 0 during the other period. Alternatively, the coast mode (IN1 = 0, IN2 = 0) for fast current decay is also available. Figure 4 shows how the motor current flows through the H-bridge. The input pins can be powered before VM is applied.



FORWARD REVERSE

Figure 4. H-Bridge Current Paths

8.4 Current Regulation

The HT8251B device limits the output current based on the analog input, VREF, and the resistance of an external sense resistor on the ISEN pin, RSENSE, according to Equation as below:

$$I_{TRIP} = \frac{VREF}{A_V \times R_{SENSE}} = \frac{VREF}{10 \times R_{SENSE}}$$

By using current regulation, the device input pins can be set for 100% duty cycle, while the device switches the outputs to keep the motor current at the ITRIP level. For example, if VREF = 3.3 V and RSENSE = 0.15 Ω, the HT8251B limits motor current to 2.2 A during high torque conditions.

When ITRIP is reached, the device enforces slow current decay by enabling both low-side FETs, and it does this for a time of tOFF.

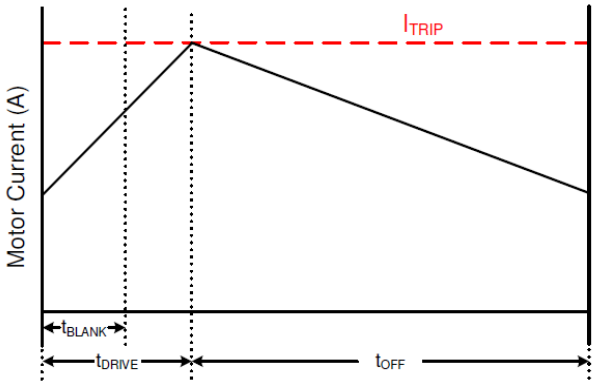


Figure 5. Current-Regulation Time Periods

After tOFF elapses, the output is re-enabled according to the two inputs, INx. The drive time (tDRIVE) until reaching another ITRIP event heavily depends on the VM voltage, the back-EMF of the motor, and the

inductance of the motor.
If current regulation is not required, the ISEN pin should be directly connected to the PCB ground plane. The VREF voltage must still be 0.3 V to 5 V, and larger voltages provide greater noise margin. This provides the highest-possible peak current which is up to $I_{OCP,min}$ for a few hundred milliseconds (depending on PCB characteristics and the ambient temperature). If current exceeds $I_{OCP,min}$, the device may enter the fault mode due to overcurrent protection (OCP) or overtemperature shutdown (TSD).

8.5 Protection Circuits

The HT8251B device is fully protected against VM undervoltage, overcurrent, and overtemperature events.

8.5.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive internally. If this analog current limit persists for longer than the OCP deglitch time (t_{OCP}), all FETs in the H-bridge will disable. The driver re-enables after the OCP retry period (t_{RETRY}) has passed. If the fault condition is still present, the cycle repeats.

8.5.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature has fallen to a safe level, operation automatically resumes.

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8.5.4 VM Undervoltage Lockout (UVLO)

Whenever the voltage on the VM pin falls below the UVLO falling threshold voltage, VUVLO, all circuitry in the device is disabled, the output FETS are disabled, and all internal logic is reset.

8.6 Device Functional Modes

Table 6 summarizes the HT8251B functional modes described in this section.

Table 6 Modes of Operation

MODE	CONDITION	H-BRIDGE	INTERNAL CIRCUITS
Active Mode	IN1 or IN2 = logic high	Operating	Operating
Low-Power Sleep Mode	IN1 = IN2 = logic low	Disabled	Disabled
Fault Mode	Any fault condition met	Disabled	See Table 7

8.6.1 Active Mode

After the supply voltage on the VM pin has crossed the undervoltage threshold V_{UVLO}, the INx pins are in a state other than IN1 = 0 & IN2 = 0, and t_{WAKE} has elapsed, the device enters active mode. In this mode, the H-bridge, charge pump, and internal logic are active and the device is ready to receive inputs.

8.6.2 Low-Power Sleep Mode

When the IN1 and IN2 pins are both low for time t_{SLEEP}, the HT8251B device enters a low-power sleep mode. In sleep mode, the outputs remain High-Z and the device draws minimal current from the supply pin (IVMQ). If the device is powered up while all inputs are low, it immediately enters sleep mode. After any of the input pins are set high for longer than the duration of t_{WAKE}, the device becomes fully operational. Figure 6 shows an example timing diagram for entering and leaving sleep mode.

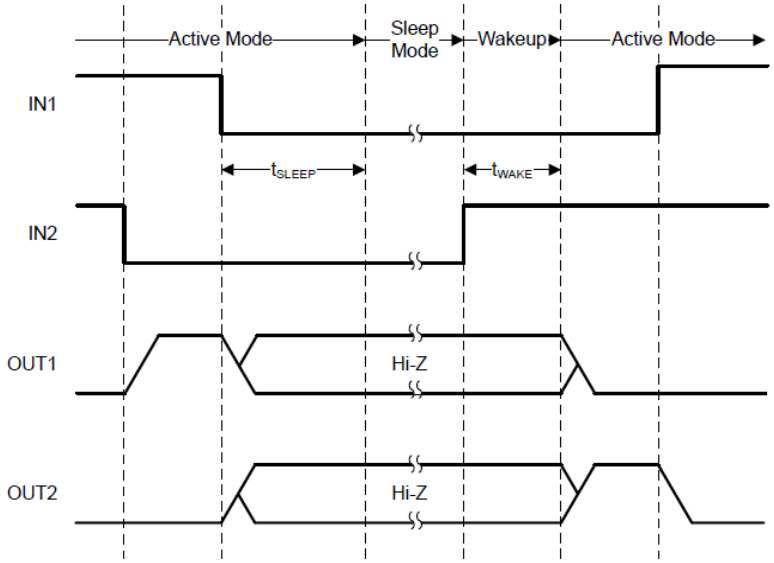


Figure 6. Sleep Mode Entry and Wakeup Timing Diagram

8.6.3 Fault Mode

The HT8251B device enters a fault mode when a fault is encountered. This is utilized to protect the device and the output load. The device behavior in the fault mode is described in and depends on the fault condition. The device will leave the fault mode and re-enter the active mode when the recovery condition is met.

Table 7 Fault Conditions Summary

FAULT	CONDITION	H-BRIDGE	INTERNAL CIRCUITS	RECOVERY
VM undervoltage (UVLO)	$V_M < V_{UVLO,falling}$	Disabled	Disabled	$V_M > V_{UVLO,rising}$
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$	Disabled	Operating	$I_{OUT} < I_{OCP}$
Thermal Shutdown (TSD)	$T_J > T_{TSD}$	Disabled	Operating	$T_J < T_{TSD} - T_{HYS}$

8.7 Typical Application

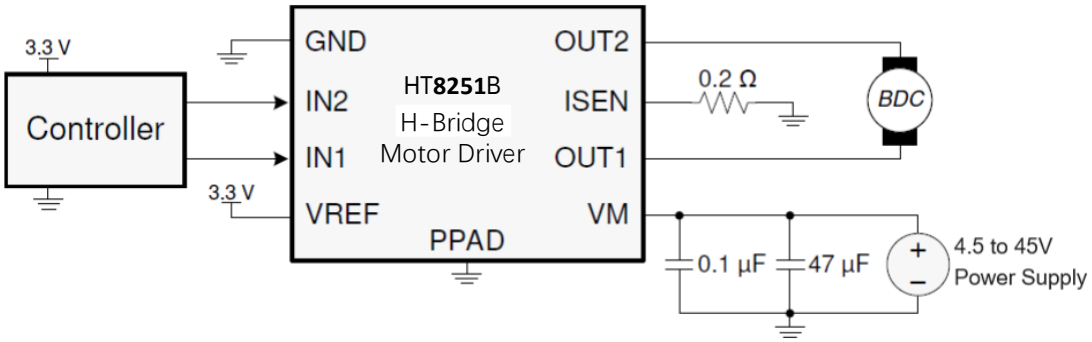
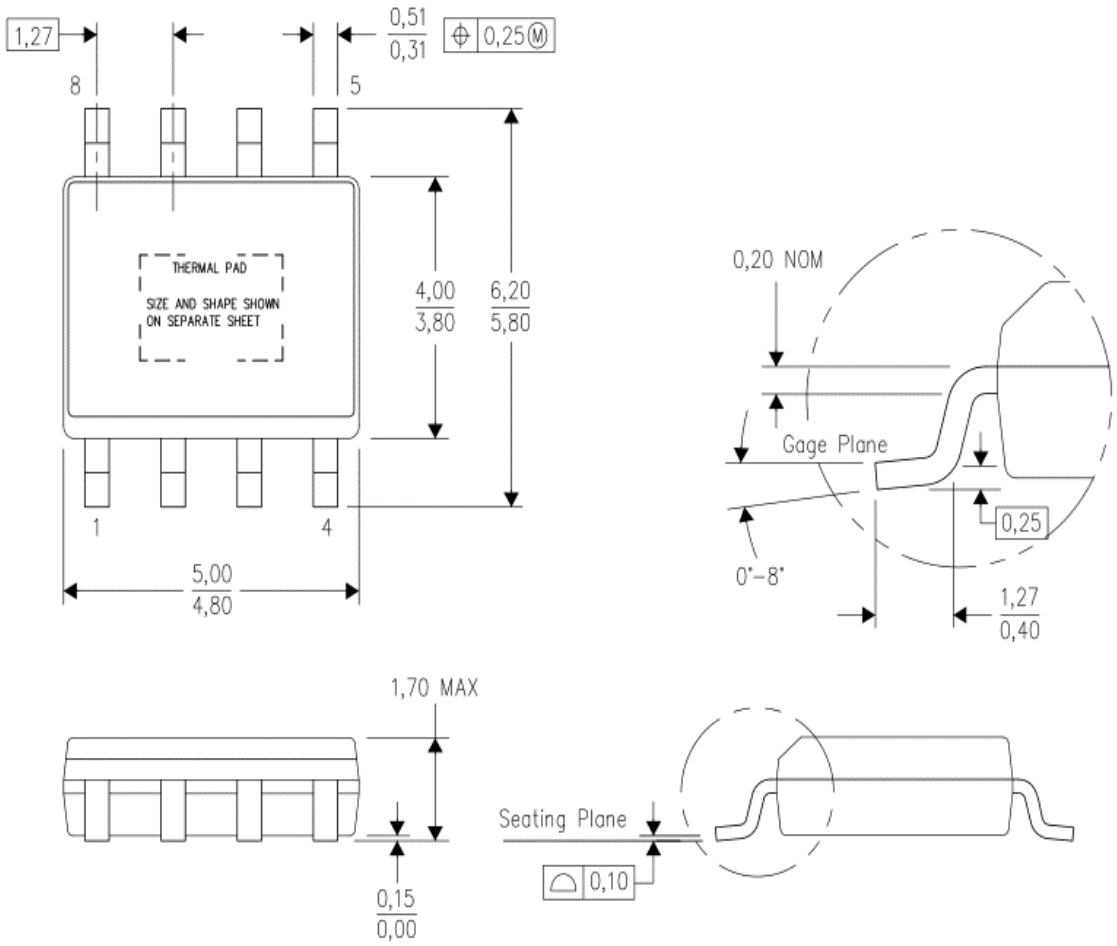


Figure 7. Typical Application Schematic

9. Package（ESOP 4.9*6.0-8）



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