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PRODUCT SPECIFICATION

Customer: _____

Product Name: Real Time Clock

Part NO: FRTC8563

Issue Date: _____

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Prepared	Checked	Customer Check
ChenTT	Zelig	

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1 Features

- - Uses an external 32.768 kHz quartz crystal
- - Supports the I2C bus high-speed mode (400 kHz)
- - Includes time (hour/minute/second) and calendar (year/month/date/day) counter functions (BCD code)
- - Programmable square wave output signal
- - Oscillator stop flag
- - Low backup current: typically 400 nA at VDD = 3.0 V and TA = 25° C
- - Operating range: 1.7 V to 5.5 V
- - Operating temperature range: -40 to 125° C

2 Applications

- Digital still camera
- Digital video camera
- Printers
- Copy machines
- Mobile equipment
- Battery powered devices

3 Description

The FRTC8563 serial real-time clock is a low-power clock/calendar featuring a programmable square-wave output.

Address and data are transferred serially through a two-wire bidirectional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of each month is automatically adjusted for months with fewer than 31 days, including leap-year corrections. The clock operates with a 24-hour format indicator.

Table 1 shows the basic functions of FRTC8563. More details are shown in section: overview of functions.

4 Ordering Information

Part Number	Package
FRTC8563S	SOP8
FRTC8563M	MSOP8

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Table 1. Basic functions of FRTC8563

Item	Function		FRTC8563
1	Oscillator	Source: Crystal: 32.768kHz	√
		Oscillator enable/disable	–
		Oscillator fail detect	√
2	Time	Time display 12-hour	–
		Time display 24-hour	√
		Century bit	√
		Time count chain enable/disable	√
3	Interrupt	Alarm interrupt	√
4	Programmable square wave output (Hz)		1, 32, 1.024k, 32.768k
5	Communication	2-wire I²C bus	√
		Burst mode	–
6	Control	Write protection	–
		External clock test mode	√
		Power-on reset override	√

5 Function Block

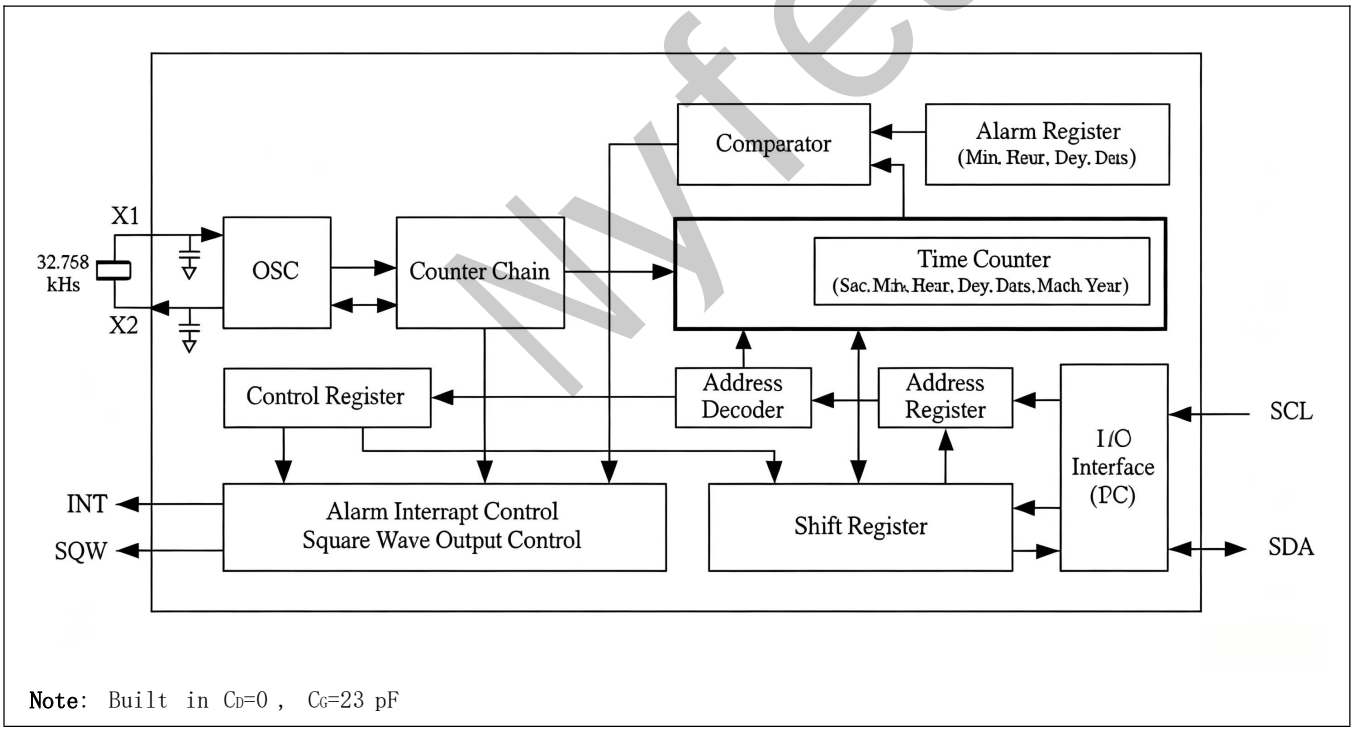


Figure 1. Function Block of FRTC8563

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6 Pin Configuration



6.1 Pin Description

Pin No.	Pin Name	Type	Description
1	X1	I	**Oscillator Circuit Input.** Together with X2, 32.768kHz crystal is connected between them.
2	X2	O	**Oscillator Circuit Output.** Together with X1, 32.768kHz crystal is connected between them.
3	/ INT	O	**Interrupt Output.** Open drain, active low.
4	GND	P	**Ground.**
5	SDA	I/O	**Serial Data Input/Output.** SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open-drain output and requires an external pull-up resistor.
6	SCL	I	**Serial Clock Input.** SCL is used to synchronize data movement on the I^2C serial interface.
7	SQW	O	**Clock Output.** Open drain. Four frequencies selectable: 32.768k, 1.024k, 32, 1Hz when SQWE bit is set to 1.
8	VCC	P	**Power.**

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7 Function Description

7.1 Clock function

The CPU can read or write data including the year (last two digits), month, date, day, hour, minute, and second. Any two-digit year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2100.

7.2 Alarm function

These devices feature one alarm system that outputs interrupt signals from the INT pin of the FRTC8563 when the date, day of the week, hour, minute, or second matches the configured setting.

Each of these parameters may independently trigger an interrupt signal at a specified time.

The alarm can be configured to be either enabled or disabled for a matching alarm or a repeating alarm.

7.3 Programmable square wave output

A square wave output enable bit controls square wave output at pin 7. 4 frequencies are selectable:1, 32, ,1.024k, 32.768k Hz.

7.4 Interface with CPU

Data is read and written through the I2C bus interface using two signal lines: SCL (clock) and SDA (data).

Since the output of the I/O pin SDA is open-drain, a pull-up resistor should be used on the circuit board if the CPU's output I/O is also open-drain.

The maximum clock frequency of SCL is 400 kHz, which supports the I2C bus's high-speed mode.

7.5 Oscillator fail detect

When oscillator fail, OSF bit will be set.

7.6 Oscillator enable/disable

Only time count chain can be enable or disable by STOP bit.

7.7 Reset function

The FRTC8563 includes an internal reset circuit that is active whenever the oscillator is stopped. In the reset state, the I2C bus logic is initialized and all registers, including the address pointer, are cleared, with the exception of bits FE, OSF, TD1, TD0, TESTC, and AE, which are set to logic 1.

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8 Registers

8.1 Allocation of registers

Addr. (hex) *1	Function (time range BCD format)	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Control/status 1	×	×	×	×	×	×	×	×
01	Control/ status 2	×	×	×	×	AF*2	×	AIE*3	×
02	Seconds (00-59)	OSF*4	S40	S20	S10	S8	S4	S2	S1
03	Minutes (00-59)	×	M40	M20	M10	M8	M4	M2	M1
04	Hours (00-23)	×	×	H20	H10	H8	H4	H2	H1
05	Dates (01-31)	×	×	D20	D10	D8	D4	D2	D1
06	Days of the week (00- 06)	×	×	×	×	×	W4	W2	W1
07	Months (01-12)	×	×	×	MO10	MO8	MO4	MO2	MO1
08	Years (00-99)	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
09	Alarm: Minutes (00-59)	AE*5	M40	M20	M10	M8	M4	M2	M1
0A	Alarm: Hours (01-12)	AE*5	×	H20	H10	H8	H4	H2	H1
0B	Alarm: Dates (01-31)	AE*5	×	D20	D10	D8	D4	D2	D1
0C	Alarm: Weekday (00-06)	AE*5	×	×	×	×	W4	W2	W1
0D	SQW control	SQWE	×	×	×	×	×	RS1	RS0

Caution points:

1. FRTC8563 uses 8 bits for address. For excess 0FH address, FRTC8563 will not respond.
2. Alarm interrupt flag bits.
3. Alarm interrupt enable bits.
4. Oscillator fail indicates. Indicate clock integrity.
5. Alarm enable bit. Alarm will be active when related time is matching if AE = 0 .
6. All bits marked with ″ ×″ are not implemented.

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8.1.1 Control and status register

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
00	Control/ status1	×	×	×	×	×	×	×	×
	(default)	0	Undefined	0	Undefined	1	Undefined	Undefined	Undefined
01	Control/ status2	×	×	×	×	AF	×	AIE	×
	(default)	Undefined	Undefined	Undefined	0	Undefined	Undefined	0	0
0D	SQW control	SQWE	×	×	×	×	×	RS1	RS0
	(default)	1	Undefined	Undefined	Undefined	Undefined	Undefined	0	0

a) **Alarm Interrupt**

AIE: Alarm Interrupt Enable bit.

AIE	Data	Description	
Read / Write	0	Alarm interrupt disabled	Default
	1	Alarm interrupt enabled	

AF: Alarm Flag

AF	Data	Description
Read	0	Alarm flag inactive
	1	Alarm flag active
Write	0	Alarm flag is cleared
	1	Alarm flag remains unchanged

b) **SQW control**

SQWE: SQW output clock enable bit.

SQWE	Data	Description	
Read / Write	0	the SQW output is inhibited and SQW output is set to high impedance	
	1	the SQW output is activated	Default

RS1 RS0: SQW output frequency select

RS1, RS0	Data	SQW output freq. (Hz)	
Read / Write	00	32.768k	Default
	01	1.024k	
	10	32	
	11	1	

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8.2 Time Counter

Time digit display (in BCD code):

1. - Second digits: Range from 00 to 59, and carried to minute digits when incremented from 59 to 00.
2. - Minute digits: Range from 00 to 59, and carried to hour digits when incremented from 59 to 00.
3. - Hour digits: See the description on the /12 and 24 bits. Carried to day and day-of-the-week digits when incremented from 11 p.m. to 12 a.m., or from 23 to 00.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
02	Seconds	OSF*1	S40	S20	S10	S8	S4	S2	S1
	(default)	1	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
03	Minutes	×	M40	M20	M10	M8	M4	M2	M1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
04	Hours	×	×	H20	H10	H8	H4	H2	H1
	(default)	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Note: Indicate clock integrity. When the bit is 1, the clock integrity is no longer guaranteed and the time need be adjusted.

8.3 Days of the week Counter

The day counter is a divide-by-7 counter that counts from 00 to 06, and after reaching 06, restarts from 00. The values corresponding to the day of the week are user-defined but must be sequential (i.e., if 0 equals Sunday, then 1 equals Monday, and so on). Illogical time and date entries result in undefined operation.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
06	Days of the week	×	×	×	×	×	W4	W2	W1
	(default)	0	0	0	0	0	Undefined	Undefined	Undefined

8.4 Calendar Counter

The data format is BCD format.

- Day digits: Range from 1 to 31 (for January, March, May, July, August, October, and December).
  Range from 1 to 30 (for April, June, September, and November).
  Range from 1 to 29 (for February in leap years).
  Range from 1 to 28 (for February in ordinary years).
  Carried to month digits when cycled to 1.
- Month digits: Range from 1 to 12, and carried to year digits when cycled to 1.
- Year digits: Range from 00 to 99, with 00, 04, 08, …, 92, and 96 counted as leap years.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
05	Dates	×	×	D20	D10	D8	D4	D2	D1
	(default)	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
07	Months	×	×	×	M10	M8	M4	M2	M1
	(default)	Undefined	0	0	Undefined	Undefined	Undefined	Undefined	Undefined
08	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

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8.5 Alarm Register

FRTC8563:

Addr.	Description	D7	D6	D5	D4	D3	D2	D1	D0
09	Alarm: Minutes	AE*1	M40	M20	M10	M8	M4	M2	M1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0A	Alarm: Hours	AE*2	×	H20	H10	H8	H4	H2	H1
	(default)	Undefined	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0B	Alarm: Dates	AE*3	×	D20	D10	D8	D4	D2	D1
	(default)	Undefined	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0C	Alarm: Weekday	AE*4	×	×	×	×	W4	W2	W1
	(default)	Undefined	0	0	0	0	Undefined	Undefined	Undefined

＊1 Note: Minute alarm enable bit. *2 Note: Hour alarm enable bit. *3 Note: Date alarm enable bit.
*4 Note: Weekday alarm enable bit.

8.6 Alarm Function

Related register

	Function	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01	Control/ status 2	×	×	×	×	AF	×	AIE	×
02	Seconds	OSF	S40	S20	S10	S8	S4	S2	S1
03	Minutes	×	M40	M20	M10	M8	M4	M2	M1
04	Hours	×	×	H20	H10	H8	H4	H2	H1
05	Dates	×	×	D20	D10	D8	D4	D2	D1
06	Days of the week	×	×	×	×	×	W4	W2	W1
09	Alarm: Minutes	AE	M40	M20	M10	M8	M4	M2	M1
0A	Alarm: Hours	AE	×	H20	H10	H8	H4	H2	H1
0B	Alarm: Dates	AE	×	D20	D10	D8	D4	D2	D1
0C	Alarm: Weekday	AE	×	×	×	×	W4	W2	W1

When one or more of these registers are loaded with a valid minute, hour, day, or weekday and its corresponding Alarm Enable (AE) bit is logic 0, that information will be compared with the current minute, hour, day, and weekday. When all enabled comparisons first match, the Alarm Flag (AF) is set. AF will remain set until cleared by software.

Once AF has been cleared, it will only be set again when the time increments to match the alarm condition once more. Alarm registers whose AE bit is at logic 1 will be ignored..

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9 I2C Bus Interface

9.1 I2C Bus Protocol

9.1.1 Overview of I2 C- BUS

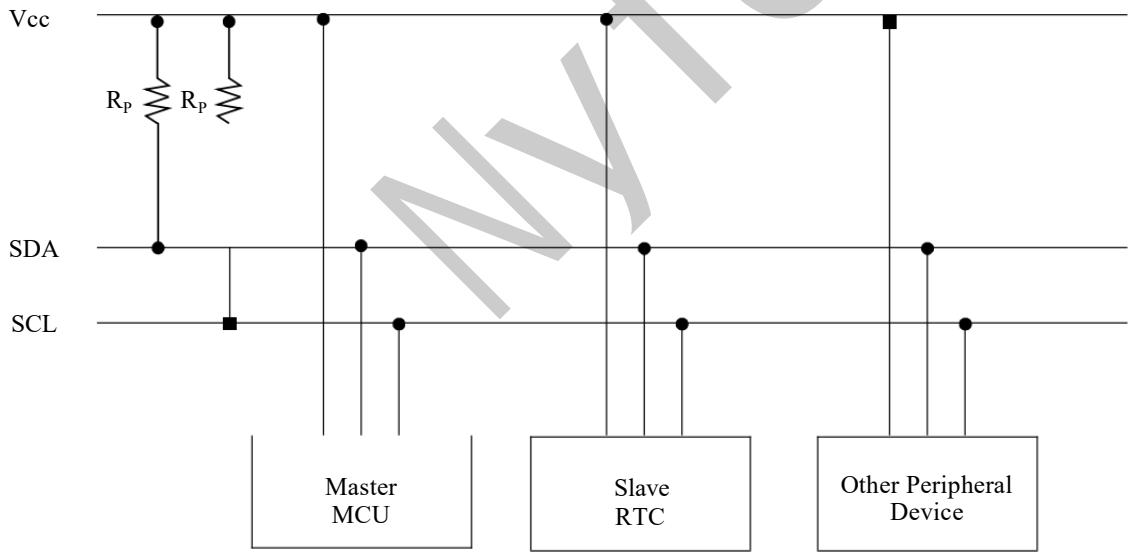
The I2C bus supports bidirectional communication via two signal lines: the SDA (data) line and the SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data signals, acknowledge signals, and so on.

Both the SCL and SDA signals are held at high level whenever communications are not being performed. The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level. During data transfers, data changes on the SDA line occur while the SCL line is at low level, and on the receiving side, the data is captured while the SCL line is at high level. In either case, data is transferred via the SCL line at a rate of one bit per clock pulse. The I2C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device, and the receiving device responds to communications only when its slave address matches the slave address in the received data.

9.1.2 System Configuration

All ports connected to the I2C bus must be either open-drain or open-collector ports in order to enable AND connections to multiple devices.

SCL and SDA are both connected to the VDD line via a pull-up resistor. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed) .



Note: When there is only one master, the MCU is ready for driving SCL to "H" and R_P of SCL may not required.

Fig.1 System configuration

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9.1.3 Starting and Stopping I2C Bus Communications

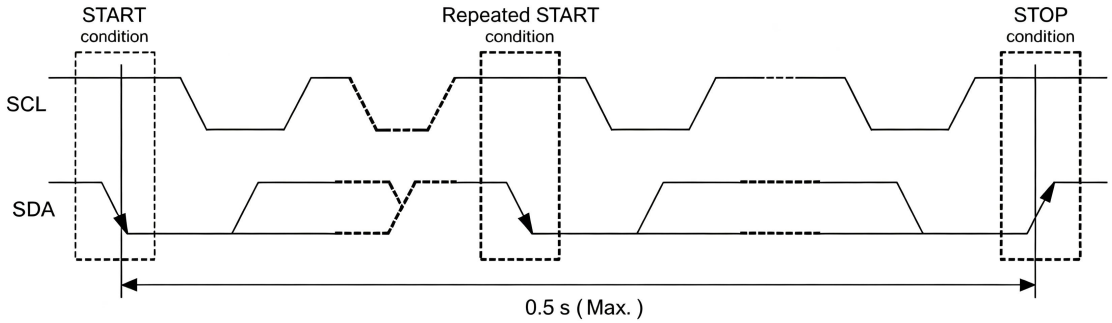


Fig.2 Starting and stopping on I2C bus START condition, repeated START condition, and STOP condition:

- START condition:

  SDA level changes from high to low while SCL is at high level.

- STOP condition:

  SDA level changes from low to high while SCL is at high level.

- Repeated START condition (RESTART condition):

  In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

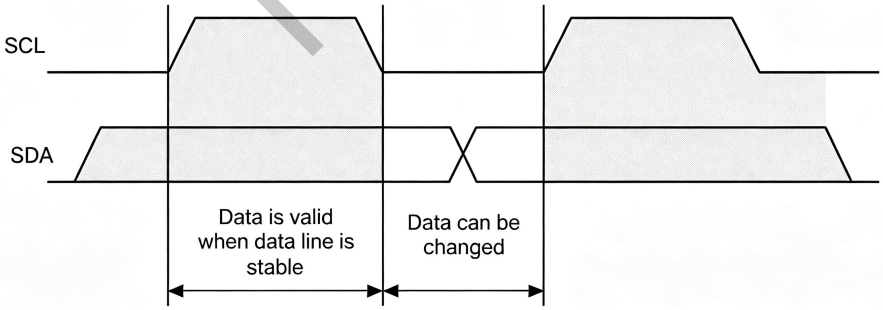
9.1.4 Data Transfers and Acknowledge Responses during I2C-BUS Communication

Data transfers

Data transfers are performed in 8-bit (1-byte) units once the START condition has occurred. There is no limit on the amount (number of bytes) of data transferred between the START condition and the STOP condition.

The address auto-increment function operates during both write and read operations.

Data on the transmitter (transmitting side)'s SDA line is updated while the SCL line is at low level. The receiver (receiving side) captures data while the SCL line is at high level.



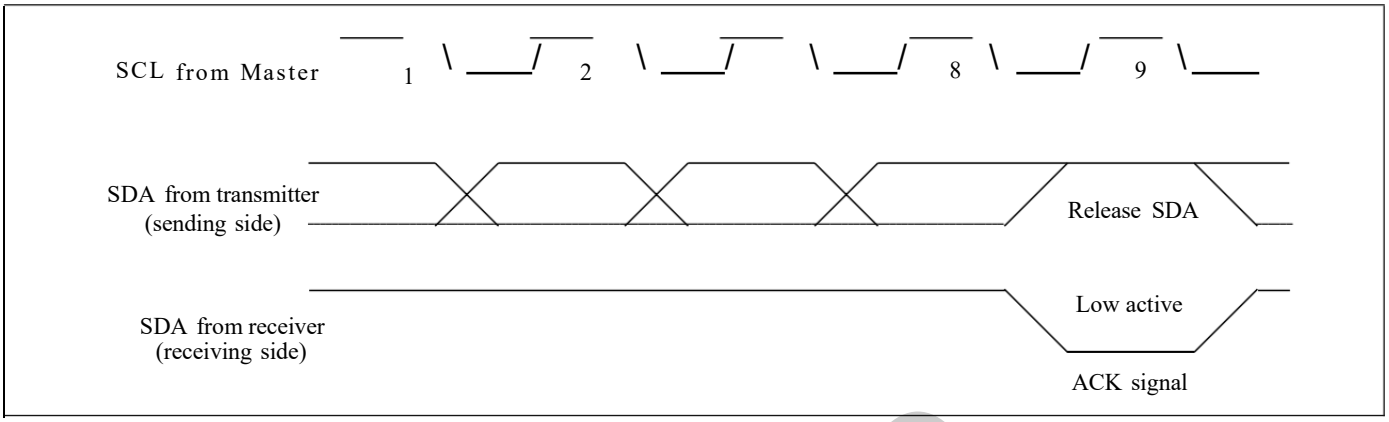
Note with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

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Data acknowledge response (ACK signal)

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line, and the receiver sets the SDA line to low (= acknowledge) level.



After transmitting the ACK signal, if the master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the master becomes the transmitter.
When the master is the receiver, if the master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the master.

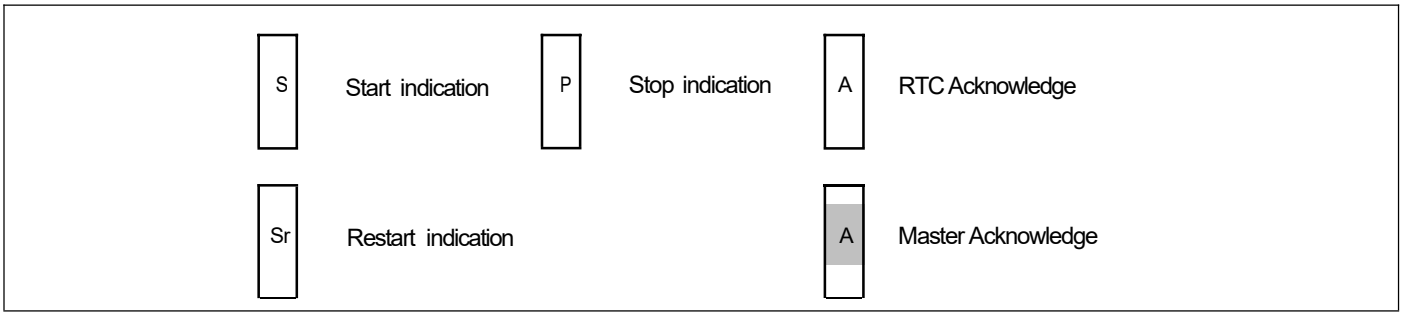
9.1.5 Slave Address

The I2C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.
All communications begin with transmitting the [START condition] + [slave address (+ R/W specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.
Slave addresses have a fixed length of 7 bits. See the table for details.
An R/W bit is added to each 7-bit slave address during 8-bit transfers..

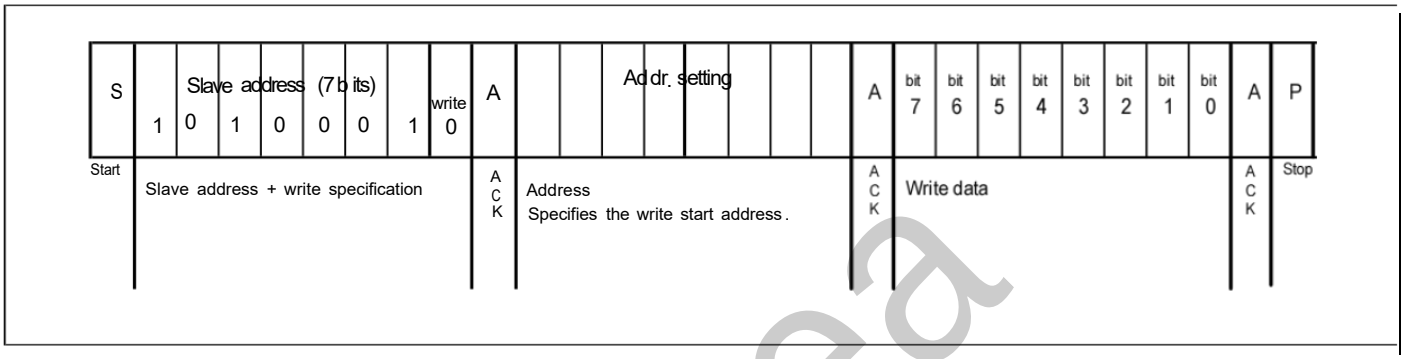
Operation	Transfer data	Slave address							R / W bit
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Read	A3 h	1	0	1	0	0	0	1	1 (= Read)
Write	A2 h								0(= Write)

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9.2 I2C Bus’s Basic Transfer Format

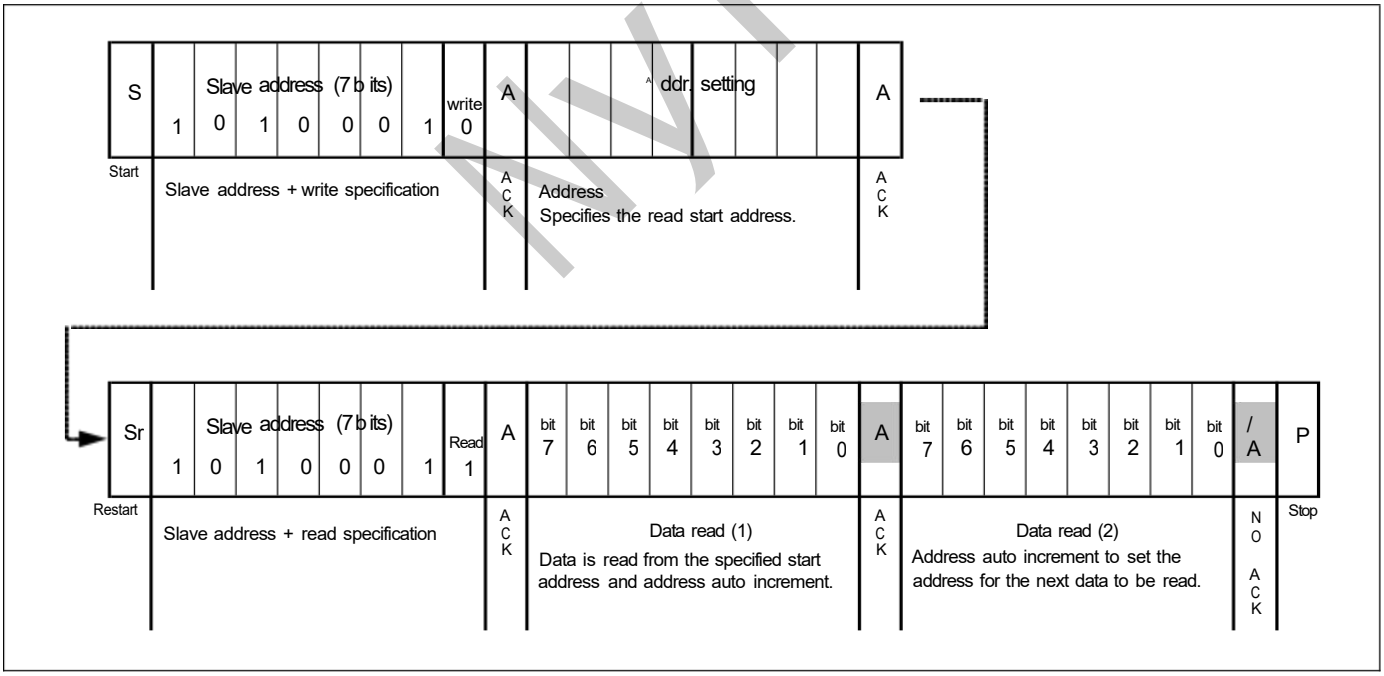


9.2.1 Write via I2 C bus



9.2.2 Read via I2C bus

Standard read



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Simplified read

S	1	Sla 0	address (7 bits) 1	0	0	0	1	Read 1	A	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	A	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	/A	P
Start	Slave address + read specification								ACK	Data read (1) Data is read from the address pointed by the internal address register and address auto increment.								ACK	Data read (2) Address register auto increment to set the address for the next data to be read.								NO ACK	Stop

Note:

The above steps are an example of transfers of only one or two bytes. There is no limit to the number of bytes transferred during actual communications. 49H and 4AH are used as test mode addresses. Customers should not use these addresses.

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10 Absolute Maximum Ratings

Storage Temperature	-65oCto +150oC
Ambient Temperaturewith PowerApplied	-40oCto +125oC
Supply Voltage to Ground Potential (VcctoGND)	-0.3V to +6.5V
DC Input (All Other Inputs exceptVcc& GND)	-0.3V to (V_{cc}+0.3V)
DC OutputVoltage (SDA,/INTA,/INTB pins)	-0.3V to +6.5V
Power Dissipation	320mW(Depend on package)

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

11 Recommended Operating Conditions

Symbol	Description	MIN	TYP	MAX	Unit
V_{CC}	Power voltage	1.7	_	5.5	V
V_{IH}	Input high level	0.7 V_{CC}	_	V_{CC}+0.3	
V_{IL}	Input low level	-0.3	_	0.3 V_{CC}	
T_A	Operating temperature	-40	_	125	°C

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12 DC Electrical Characteristics

Unless otherwise specified, GND =0V , V_{CC} = 1.7 ~ 5.5 V, T_A = -40 ° C to +125 ° C, f_{OSC} = 32.768kHz.

Symbol	Description	Pin	Conditions		MIN	TYP	MAX	Unit
V_{CC}	Supply voltage	V_{CC}	Interface inactive. T_A = 25 ° C 1)		1.5	_	5.5	V
			Interface active. f_{SCL} = 400kHz 1)		1.7	_	5.5	
	Supply voltage for clock data integrity	V_{CC}	_		1.5	_	5.5	
I_{CC}	Supply current	V_{CC}	Interface active	f_{SCL} = 400kHz	_	_	25	µA
				f_{SCL} = 100kHz	_	_	15	
			Interface inactive (f_{SCL} = 0 Hz) , pin 7 disabled T_A=- 40~ 125 ° C	V_{CC} = 5.0V	_	450	900	nA
				V_{CC} = 3.0V	_	400	800	
			Interface inactive (f_{SCL} = 0 Hz) , pin 7 enabled at 32kHz T_A=- 40~ 125 ° C	V_{CC} = 5.0V	_	650	900	nA
				V_{CC} = 3.0V	_	600	850	
V_{IL1}	Low-level input voltage	SCL	_		0	_	0.3V_{CC}	V
V_{IH1}	High-level input voltage	SCL	_		0.7V_{CC}	_	V_{CC}	
I_{OL}	Low-level output voltage	SDA	V_{OL} = 0.4V , V_{CC} = 5V		-3	_	_	mA
		/ INT, SQW	V_{OL} = 0.4V , V_{CC} = 5V		-1	_	_	
I_{IL}	Input leakage current	SCL	_		_	_	±1	µA
I_{OZ}	Output current when OFF	_	_		_	_	±1	µA

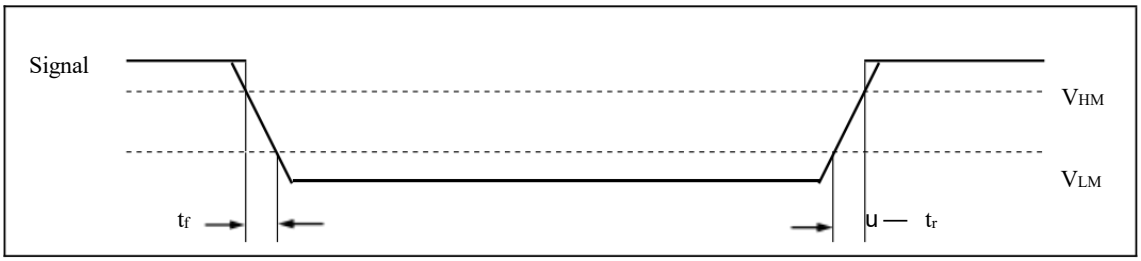
Note:

1) For reliable oscillator start-up at power-up: $V_{CC(min)\,power-up}$ = $V_{CC(min)}$ + 0.3 V

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13 AC Electrical Characteristics

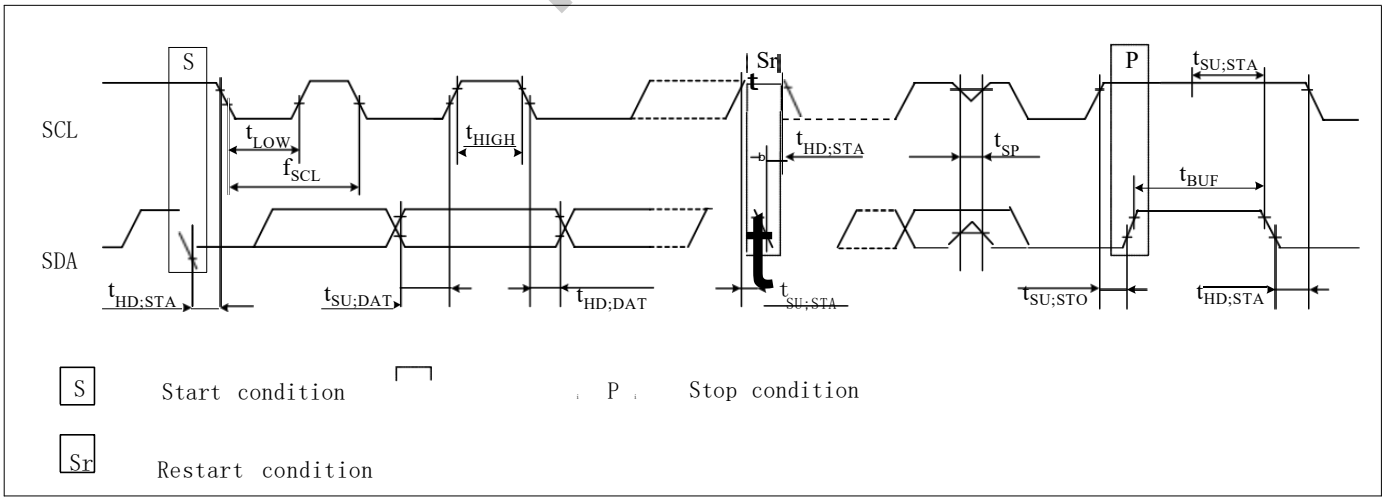
Symbol	Description	Value	Unit
V_{HM}	Rising and falling threshold voltage high	0.8 V_{CC}	V
V_{HL}	Rising and falling threshold voltage low	0.2 V_{CC}	V



Over the operating range

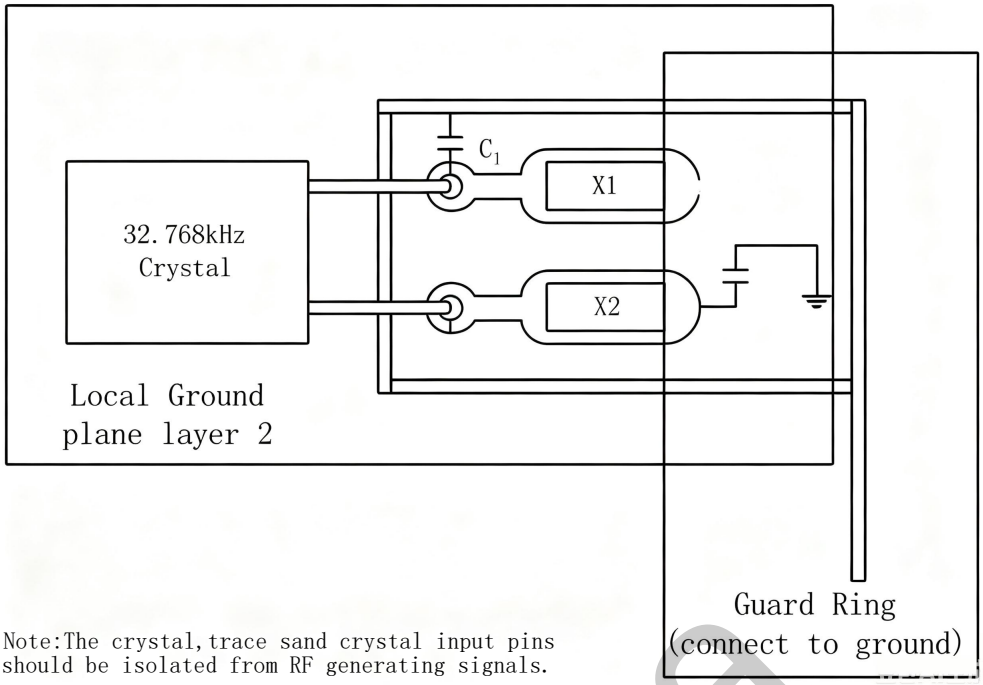
Symbol	Description	MIN	TYP	MAX	Unit
f_{SCL}	SCL clock frequency	_	_	400	kHz
$t_{SU;STA}$	START condition set-up time	0.6	_	_	μs
$t_{HD;STA}$	START condition hold time	0.6	_	_	μs
$t_{SU;DAT}$	Data set-up time (RTC read/write in Fast mode)	100	_	_	ns
$t_{HD;DAT1}$	Data hold time (RTC write)	35	_	_	ns
$t_{HD;DAT2}$	Data hold time (RTC read)	0	_	_	μs
$t_{SU;STO}$	STOP condition setup time	0.6	_	_	μs
t_{BUF}	Bus idle time between a START and STOP condition	1.3	_	_	μs
t_{LOW}	When SCL = "L"	1.3	_	_	μs
t_{HIGH}	When SCL = "H"	0.6	_	_	μs
t_r	Rise time for SCL and SDA	_	_	0.3	μs
t_f	Fall time for SCL and SDA	_	_	0.3	μs
t_{SP}*	Allowable spike time on bus	_	_	50	ns
C_B	Capacitance load for each bus line	_	_	400	pF

Note: Only reference for design.



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14 Recommended Layout for Crystal



Note:The crystal,trace sand crystal input pins should be isolated from RF generating signals.

15 Built-in Capacitors Specifications and Recommended External Capacitors

Symbol	Parameter		TYP	Unit
CD	Build-in capacitors	X1 to GND	0	pF
CG		X2 to GND	23	pF
C1	Recommended External capacitors for	X1 to GND	22	pF
C2	crystal CL= 12 .5 pF	X2 to GND	0	pF
C1	Recommended External capacitors for	X1 to GND	7	pF
C2	crystal CL= 6 pF	X2 to GND	0	pF

Note: The crystal frequency can be optimized using external capacitors C1 and C2. For a frequency of 32.768 Hz, C1 and C2 should satisfy the equation below:

Cpar + [(C1+CG)*(C2+CD)] / [(C1+CG)+(C2+CD)] = CL

Where Cpar is the total parasitic capacitance between X1 and X2, and CL is the crystal's load capacitance.

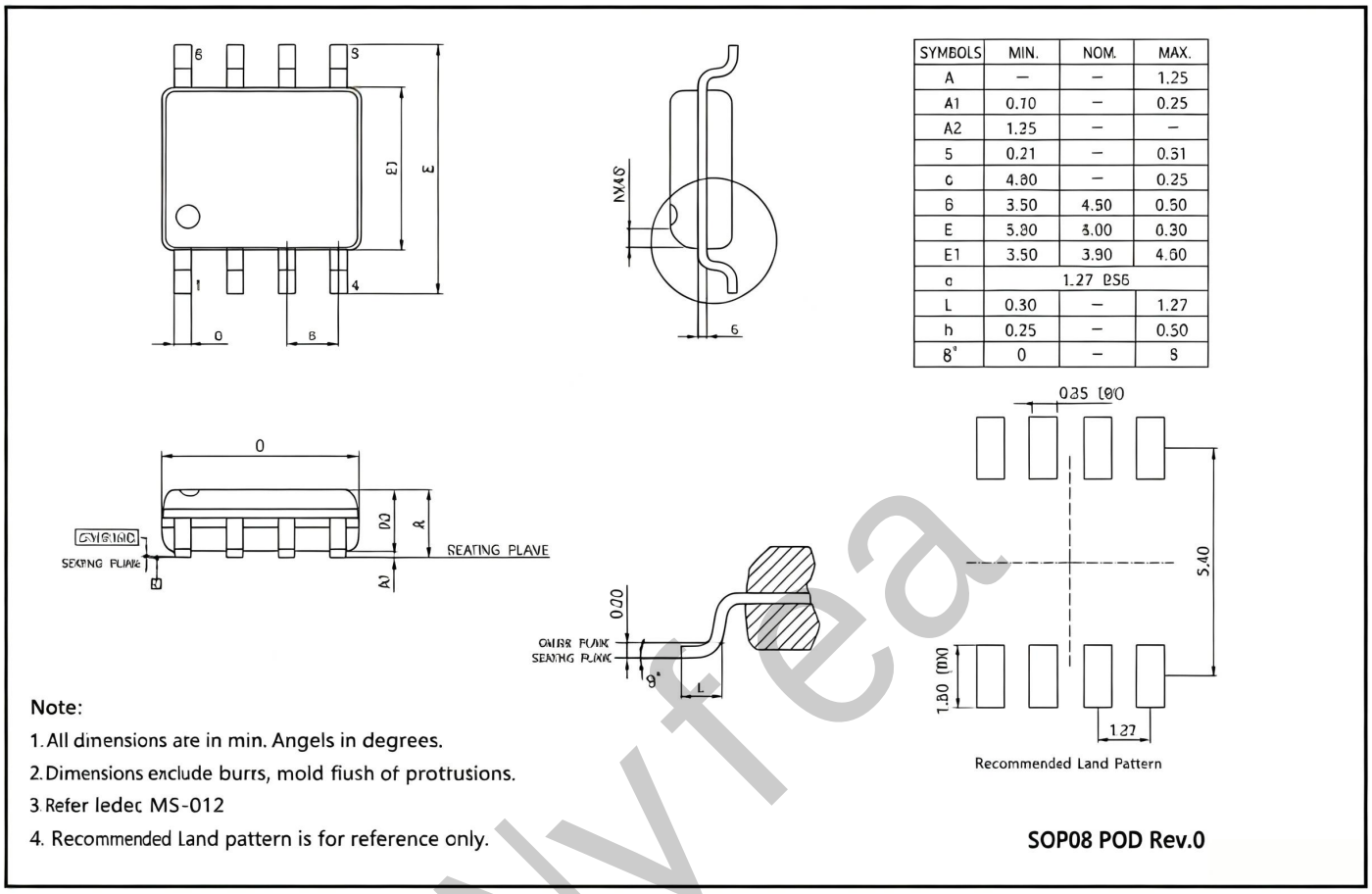
16 Crystal Specifications

Symbol	Parameter	MIN	TYP	MAX	Unit
f0	Nominal Frequency	_	32.768	_	kHz
ESR	Series Resistance	_	_	70	kΩ
CL	Load Capacitance	_	6/12.5	_	pF

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17 Package Information

17.1 FRTC8563S (SOP8) Package



SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.25
A1	0.10	—	0.25
A2	1.25	—	—
5	0.21	—	0.31
c	4.80	—	0.25
6	3.50	4.50	0.50
E	5.80	3.00	0.30
E1	3.50	3.90	4.60
a	1.27 BS6		
L	0.30	—	1.27
h	0.25	—	0.50
8°	0	—	8

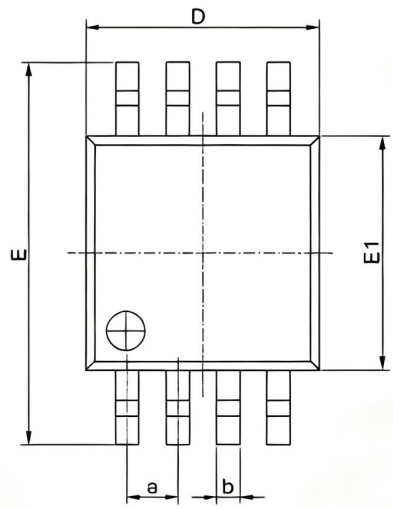
Note:

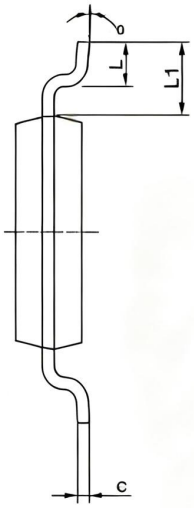
1. All dimensions are in min. Angels in degrees.
2. Dimensions exclude burrs, mold flush of protrusions.
3. Refer Iedec MS-012
4. Recommended Land pattern is for reference only.

SOP08 POD Rev.0

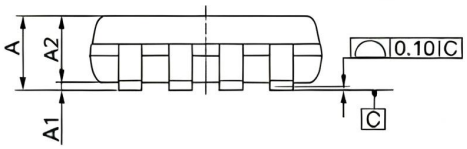
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17.2 FRTC8563M (MSOP-8) Package





PKG DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	–	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.80	3.20
E	2.65	5.15
E1	2.60	3.20
e	0.65 BSC	
L	0.40	0.80
L1	0.95 REF	
θ	0°	8°



Note:

1.All dimensions are in mm. Angels in degrees.

2.Refer Jedec MO-1873

3.Dimensions exclude burrs, mold flash or protrusions.

MSOP08 POD Rev.0

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