

Spread Spectrum Clock Generator

Ultra Low Power Mobile EMI Reduction IC

SSDCI3128AF



■ DESCRIPTION

The SSDCI3128AF is a versatile 1x spread spectrum frequency modulator designed to reduce electromagnetic interference (EMI) clock and data source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The SSDCI3128AF allows significant system cost savings by reducing the number of circuit board layers ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations. The SSDCI3128AF family of mobile active EMI management ICs are unique in their design by eliminating the use of conventional PLLs. This allows operation on aperiodic as well periodic signals. The peak energy is distributed over a wider and controlled energy band thereby significantly lowering system

EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is known as "Spread Spectrum" or active EMI management.

3128 has an input frequency range of 1 MHz to 40 MHz over a wide voltage range of 1.65V to 3.6V and generates a 1x spread spectrum output. The device can be placed in "power save mode" by setting the PDB pin to GND where in it draws typically 0.1uA and also steers the MODOUT pin to a High-Z state. The device has two "Spreading Range control pins" SS1 and SS0 to allow flexibility and optimization of both EMI compliance as well in system design.

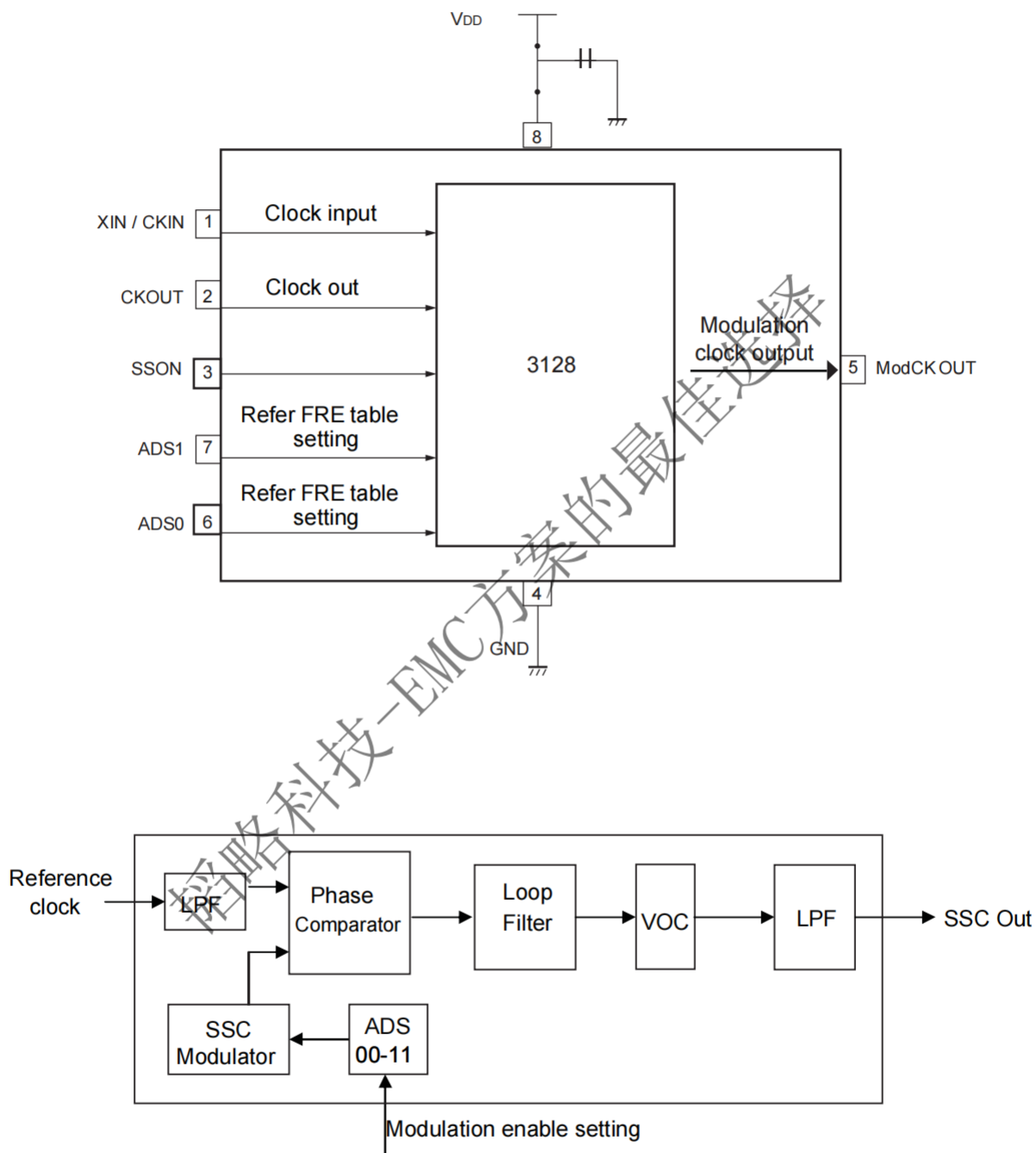
■ FEATURE

- FCC approved method of EMI attenuation.
- Generates a 1X low EMI spread spectrum clock of the input frequency.
- Input / Output frequency 1 MHz to 40 MHz
- VDD 1.65V - 3.6V
- Multiple Spreading Range Selections(Refer product table)
- Power save mode
- 8-pin TDFN package
- Operating Temperature -40°C to 85°C

■ Application

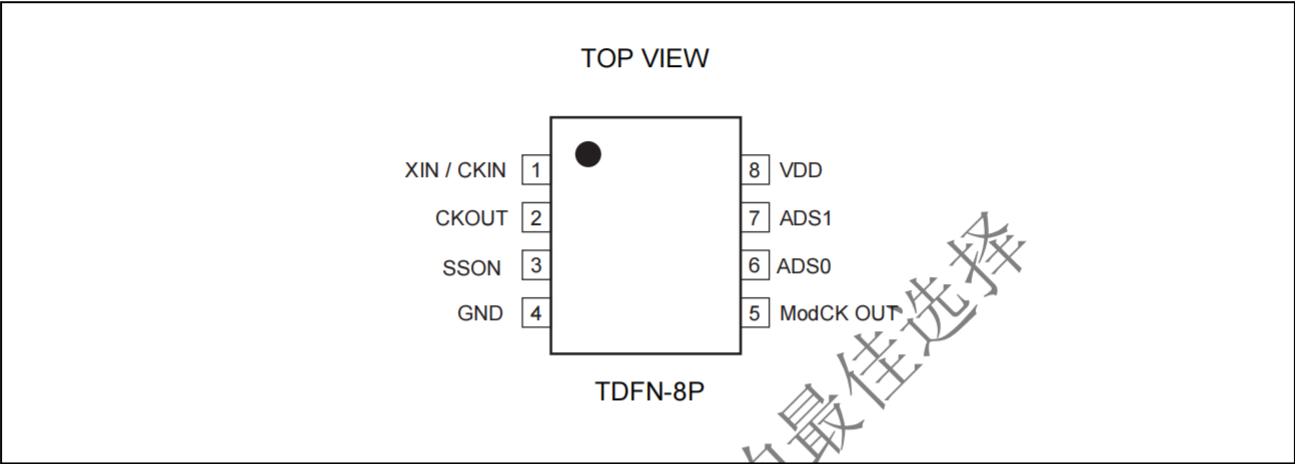
3128 is targeted for consumer electronics application such as MFP, STB, DSC, MID, HDMI, LCD panel Camcorder, and other timing sensitive analog video imaging applications. Applications of HDMI, RJ45 port has good compatibility

■ BLOCK DIAGRAM



SSDCI3128AF block

PIN ASSIGNMENT



PIN DESCRIPTION

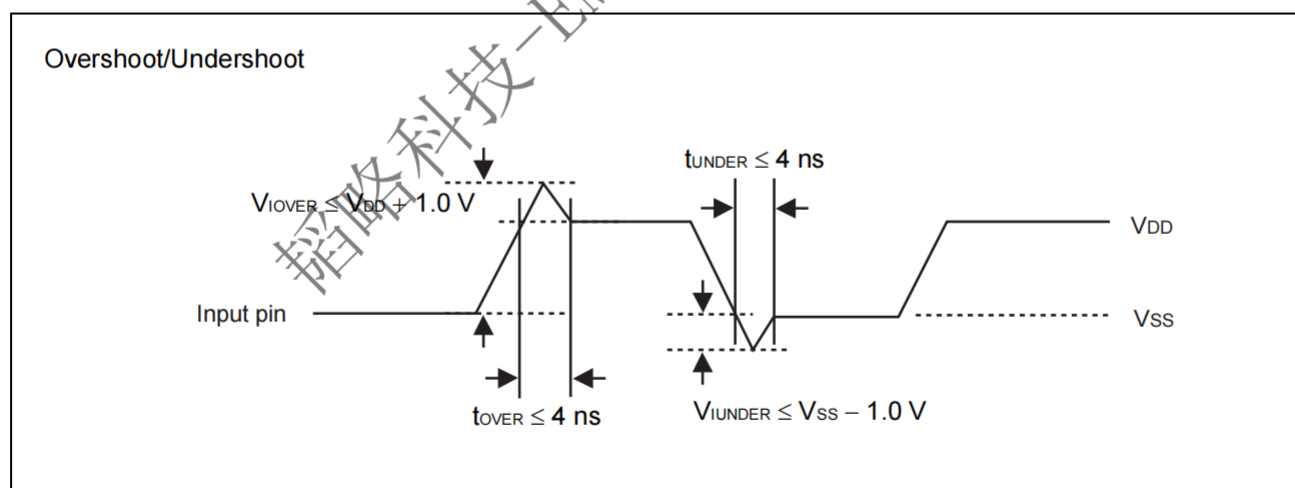
Pin name	I/O	Pin no.	Description
XIN / CKIN	I	1	Clock input pin (or External reference clock input).
CKOUT	O	2	Crystal connection(external reference, this pin should be left open)
SSON	I	3	ModCK OUT ON/OFF 1=ON 0=OFF
GND	---	4	GND pin
ModCK OUT	O	5	Modulation clock output
ADS0	I	6	Analog Spreading Range Selection(refer Functionality Table)
ADS1	I	7	Analog Spreading Range Selection(refer Functionality Table)
VDD	---	8	Power supply voltage pin

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	- 0.5	+ 4.5	V
Input voltage*	V_I	$V_{SS} - 0.5$	$V_{DD} + 0.5$	V
Output voltage*	V_O	$V_{SS} - 0.5$	$V_{DD} + 0.5$	V
Storage temperature	T_{ST}	- 55	+ 125	°C
Operation junction temperature	T_J	-40	+85	°C
Output current	I_O	4		mA
Static Discharge Voltage (As per JEDEC STD22-A114-B)	T_{DV}	—	2000	V
Overshoot	V_{IOVER}	—	$V_{DD} + 1.0$ ($t_{OVER} \leq 4ns$)	V
Undershoot	V_{IUNDER}	$V_{SS} - 1.0$ ($t_{UNDER} \leq 4ns$)	—	V

* : The parameter is based on $V_{SS} = 0.0$ V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.



■ ELECTRICAL CHARACTERISTICS

• DC Characteristics

(Ta = -40°C to +85 °C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V)

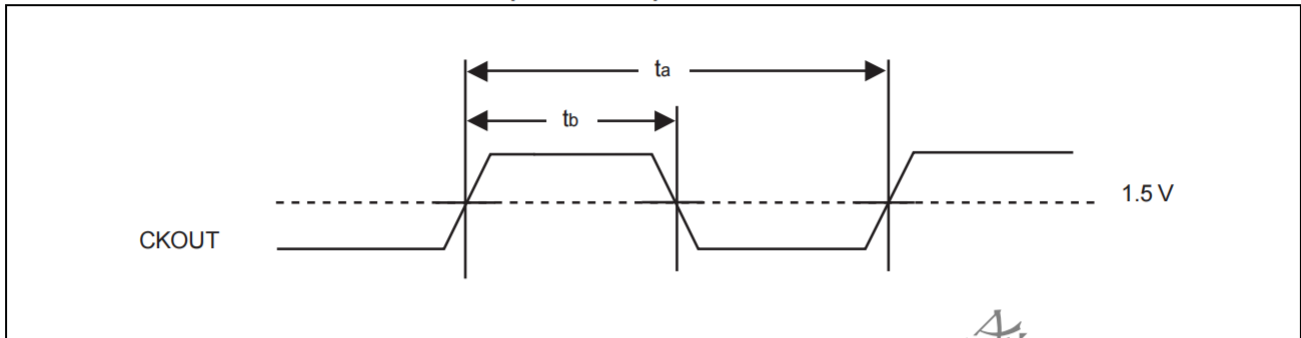
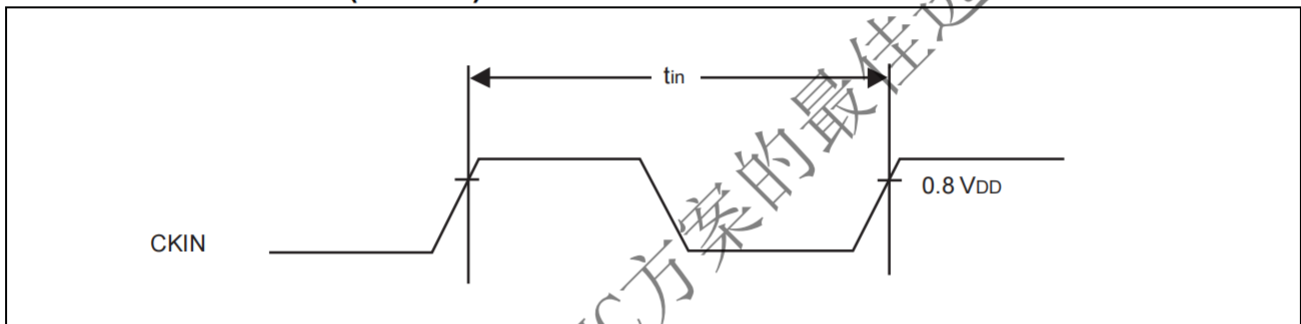
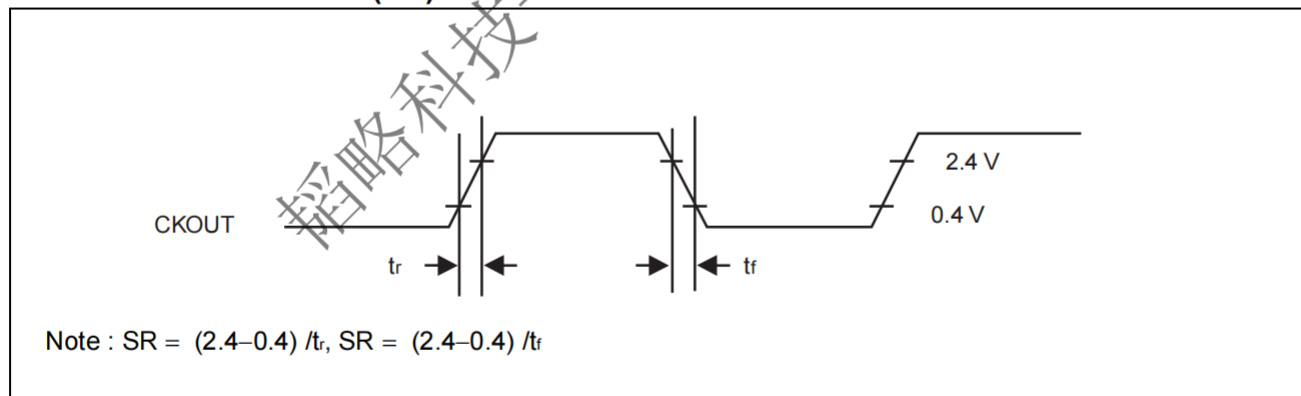
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Output voltage	V _{OH}	CKOUT	"H" level output I _{OH} = -4 mA	0.66V _{DD}	—	V _{DD}	V
	V _{OL}	CKOUT	"L" level output I _{OL} = 4 mA	V _{SS}	—	0.33V _{DD}	V
Output impedance	Z _O	CKOUT	1 MHz to 40 MHz	—	30	—	Ω
Input capacitance	C _{IN}	CKIN,	Ta = +25 °C, V _{DD} = V _I = 0.0 V, f = 1 MHz	—	—	16	pF
Load capacitance	C _L	CKOUT	1 MHz to 40 MHz	—	—	10	pF
Power supply current	I _{CC}	V _{DD}	No load capacitance at 27 MHz	—	3.0	4	mA
Power down current	I _{PD}	V _{DD}	Input clock stopping	—	4	—	μA

• AC Characteristics

(Ta = -40°C to +85 °C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Input frequency	f _{in}	CKIN	—	1.0	—	40	MHz
Output frequency	f _{OUT}	CKOUT	—	1.0	—	40	MHz
Output slew rate	SR	CKOUT	Load capacitance 15 pF 0.4 V to 2.4 V	0.4	—	4.0	V/ns
Output clock duty cycle	t _{DCC}	CKOUT	1.5 V	45	—	55	%
Output Rise Time			between 20% to 80%		0.9		nS
Output Fall Time			between 80% to 20%		0.9		nS
Cycle-cycle jitter	t _{JC}	CKOUT	No load capacitance, Ta = +25 °C, V _{DD} = 3.3 V	—	—	40	ps-rms

Note : The modulation clock stabilization wait time is required after the power is turned on, the IC recovers from power saving, or after ENS (modulation ON/OFF) setting is changed. For the modulation clock stabilization wait time, assign the maximum value for lock-up time.

■ OUTPUT CLOCK DUTY CYCLE ($t_{DCC} = t_b/t_a$)**■ INPUT FREQUENCY ($f_{in} = 1/t_{in}$)****■ OUTPUT SLEW RATE (SR)**

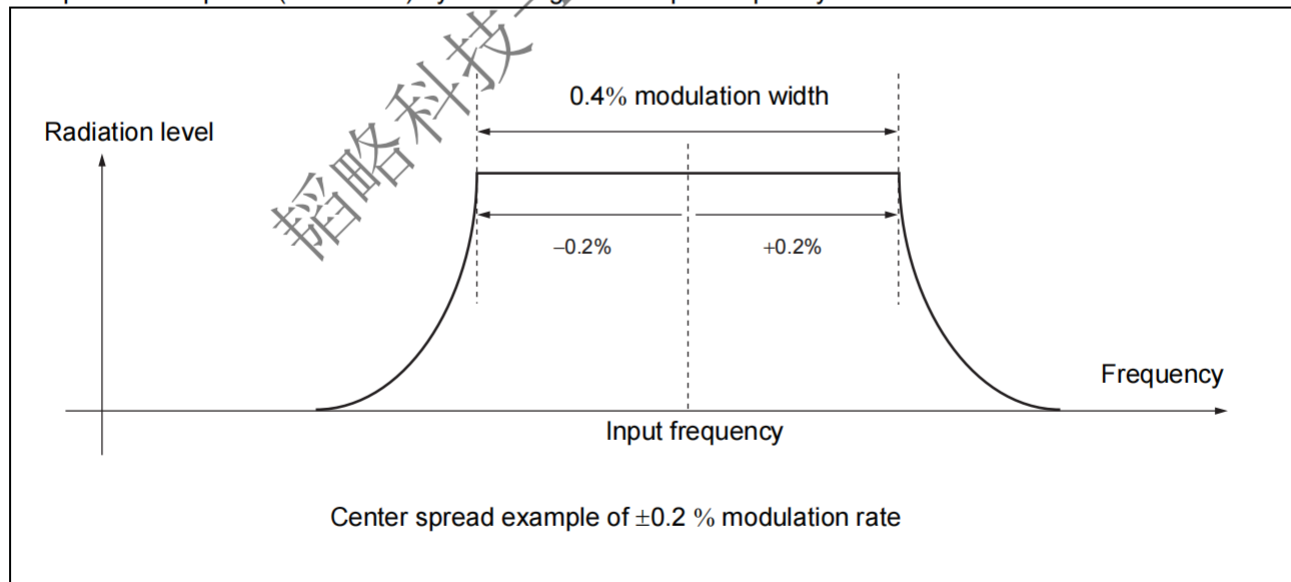
Functional Table

Vdd(V)	Freq. Range	Freq(MHz)	Spreading Range (%)							
			ADS1	ADS0	ADS1	ADS0	ADS1	ADS0	ADS1	ADS0
			0	0	0	1	1	0	1	1
3.3	1~40	12	± 0.06		± 0.12		± 0.18		± 0.22	
		24	± 0.10		± 0.19		± 0.26		± 0.32	
		27	± 0.12		± 0.23		± 0.31		± 0.37	
		32	± 0.11		± 0.23		± 0.29		± 0.33	

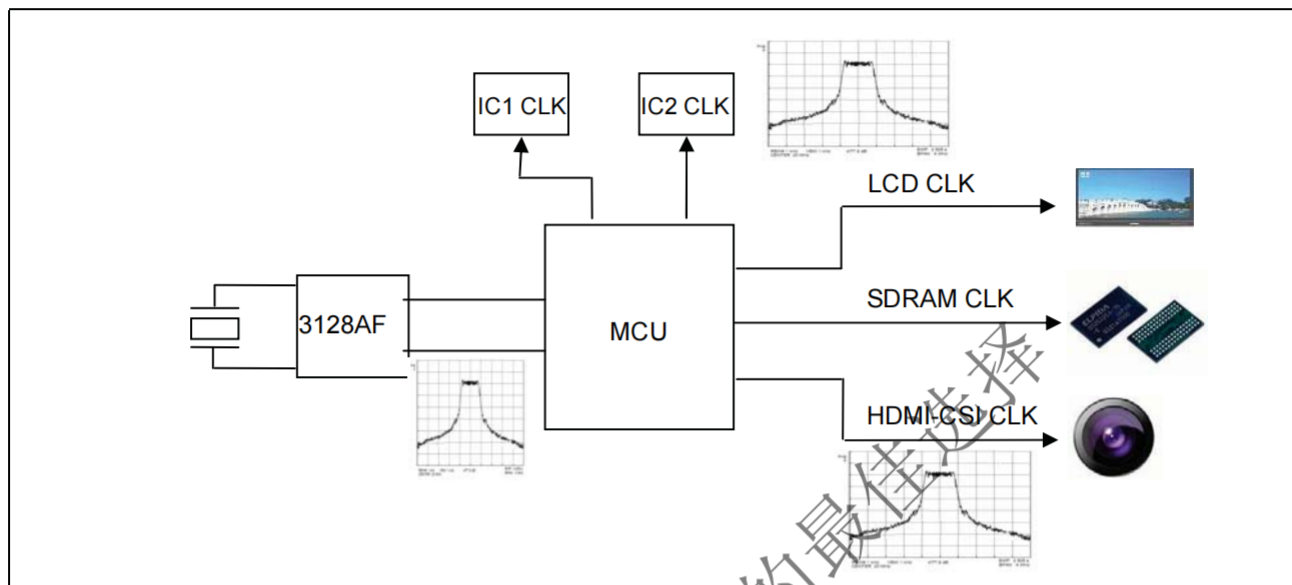
Note: Frequency Spreading Range can vary over voltage and temperature by 5%

- Center spread

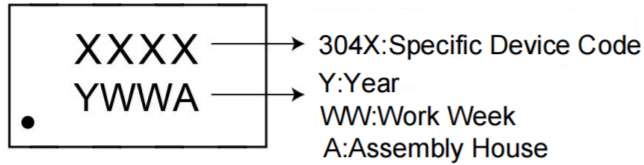
Spectrum is spread (modulated) by centering on the input frequency.



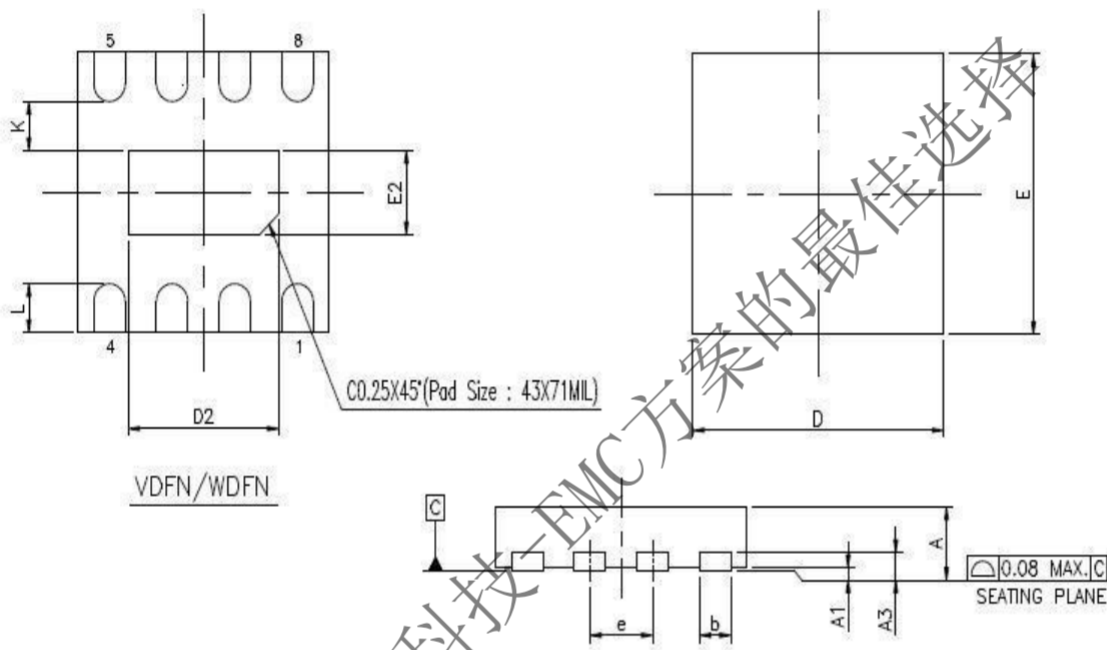
- Diagram of CLK spread



Marking Information



TDFN-2×2-8L



JEDEC OUTLINE	MO-229		
PKG CODE	WDFN(X208)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.20	0.25	0.30
D	1.95	2.00	2.05
E	1.95	2.00	2.05
e	.5 BSC		
K	0.20	...	...

NOTES

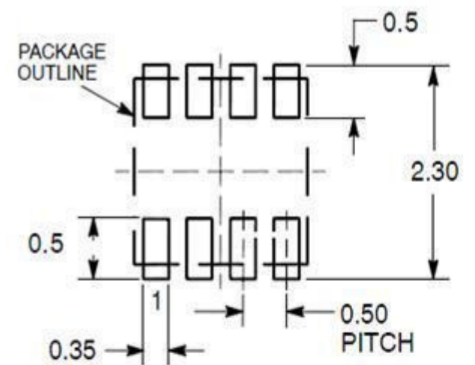
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

	D2			E2			L			LEAD FINISH		JEDEC CODE	VDFN	WDFN
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure	PPF	N/A	V	V
43*71*MIL	1.55	1.60	1.65	0.85	0.90	0.95	0.25	0.30	0.35	V	X	N/A	V	V

“*”表示汎用字元，此汎用字元可能被其它不同字元所取代，实际的字元请参照bonding diagram所示。

**is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

RECOMMENDED SOLDERING FOOTPRINT*



Ordering Code

Part Number	Package	Temperature
SSDCI3128AF-08-CT	8- pin 2-mm TDFN COL - TAPE & REEL, Green	-40°C to +85 °C

Device Ordering Information

SSDCI 3128AF - 08 - CT

T = Tape & Reel, R = Tube or Tray

O = TSOT23	U = MSOP	J=TSOT26
S = SOIC	E = TQFP	C=TDFN (2X2) COL
T = TSSOP	L = LQFP	
A = SSOP	U = MSOP	
V = TVSOP	P = PDIP	
B = BGA	D = QSOP	
Q = QFN	X = SC-70	

DEVICE PIN COUNT

F = LEAD FREE AND RoHS COMPLIANT PART
G = GREEN PACKAGE, LEAD FREE, and RoHS

PART NUMBER

A=Automotive (-40°C to +125°C)	I= Industrial (-40°C to +85°C)	P or n/c = Commercial (0°C to +70°C)
A = Clock Generator	F = Power Management	
B = Non PLL based	G = Power Management	
C = EMI Reduction	H = Power Management	
D = DDR support products	I = Hi Performance	
E = STD Zero Delay Buffer	J = Reserved	

Spread Spectrum Device