



Description

The NTMD4820NR2G uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



SOP-8
(SOIC-8)

General Features

$V_{DS} = 30V$ $I_D = 8.5A$

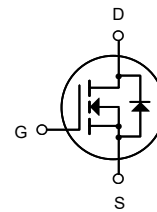
$R_{DS(ON)} < 18m\Omega$ @ $V_{GS}=10V$

Application

Battery protection

Load switch

Uninterruptible power supply



N-Channel MOSFET

Ordering Information

Product ID	Pack	Brand	Qty(PCS)
NTMD4820NR2G	SOP-8(SOIC-8)	HXY MOSFET	3000

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current ¹	8.5	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current ¹	5.6	A
I_{DM}	Pulsed Drain Current ²	35	A
EAS	Single Pulse Avalanche Energy ³	20	mJ
I_{AS}	Avalanche Current	20	A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation ⁴	1.5	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹ ($t \leq 10s$)	85	$^\circ C/W$
	Thermal Resistance Junction-ambient ¹	25	$^\circ C/W$



Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.034	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =7A	---	14	18	mΩ
		V _{GS} =4.5V, I _D =4A	---	20	26	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.2	1.5	2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-3.84	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =24V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =7A	---	6.2	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	1.04	2.1	Ω
Q _g	Total Gate Charge (4.5V)	V _{DS} =15V, V _{GS} =4.5V, I _D =7A	---	6	8.4	nC
Q _{gs}	Gate-Source Charge		---	2.2	3.1	
Q _{gd}	Gate-Drain Charge		---	2	2.8	
T _{d(on)}	Turn-On Delay Time	V _{DD} =15V, V _{GS} =10V, R _G =3.3Ω I _D =7A	---	1.2	2.4	ns
T _r	Rise Time		---	40	72.0	
T _{d(off)}	Turn-Off Delay Time		---	18	36.0	
T _f	Fall Time		---	7.2	14.4	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	583	816.2	pF
C _{oss}	Output Capacitance		---	77	107.8	
C _{rss}	Reverse Transfer Capacitance		---	59	82.6	
I _S	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	7	A
I _{SM}	Pulsed Source Current ^{2,5}		---	---	35	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.2	V
t _{rr}	Reverse Recovery Time	I _F =7A, dI/dt=100A/μs, T _J =25°C	---	7.2	---	nS
Q _{rr}	Reverse Recovery Charge		---	2.9	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=20A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



Typical Characteristics

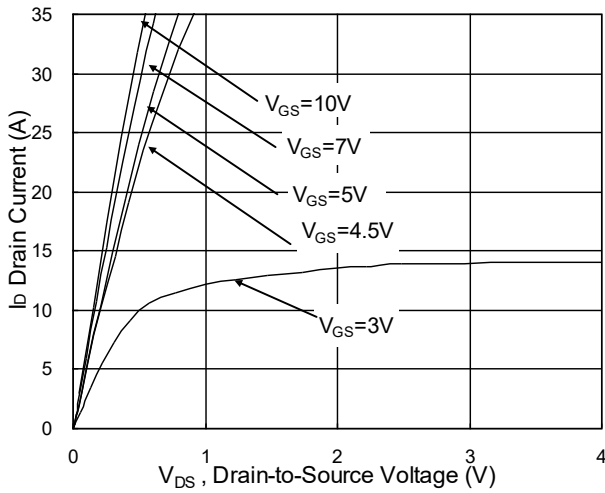


Fig.1 Typical Output Characteristics

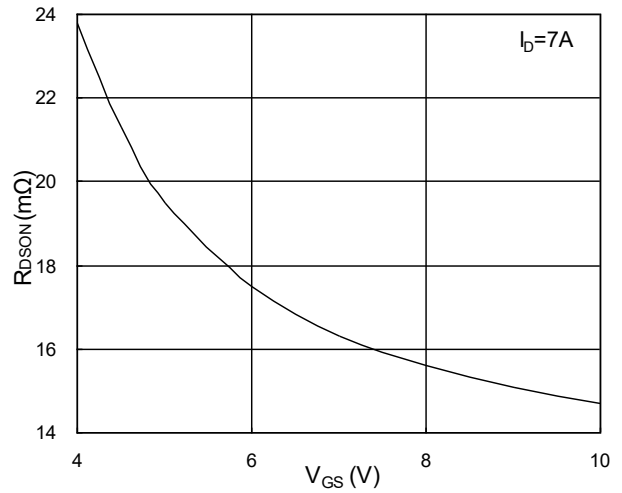


Fig.2 On-Resistance vs. Gate-Source

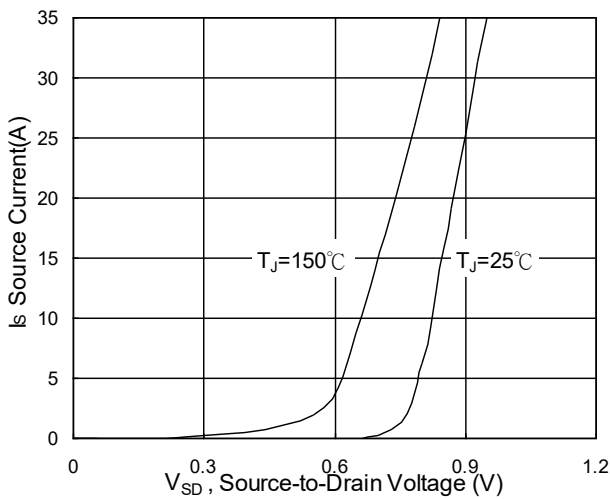


Fig.3 Forward Characteristics Of Reverse

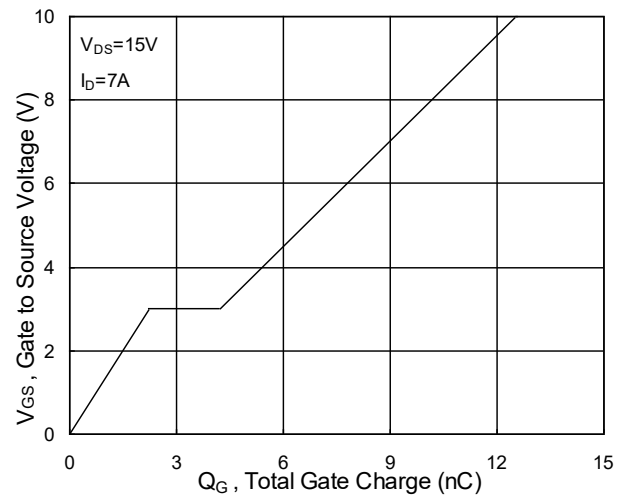


Fig.4 Gate-Charge Characteristics

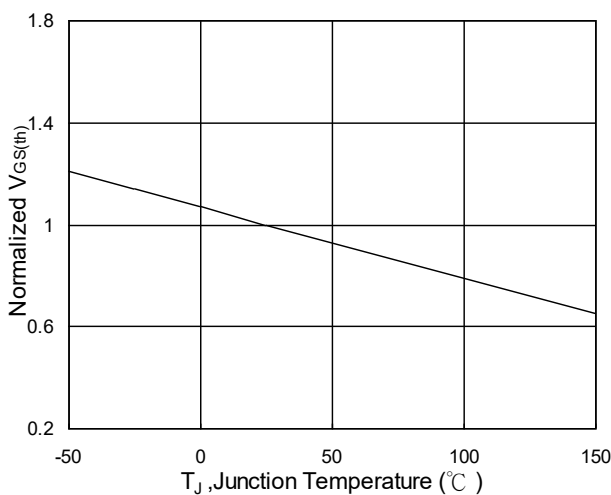


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

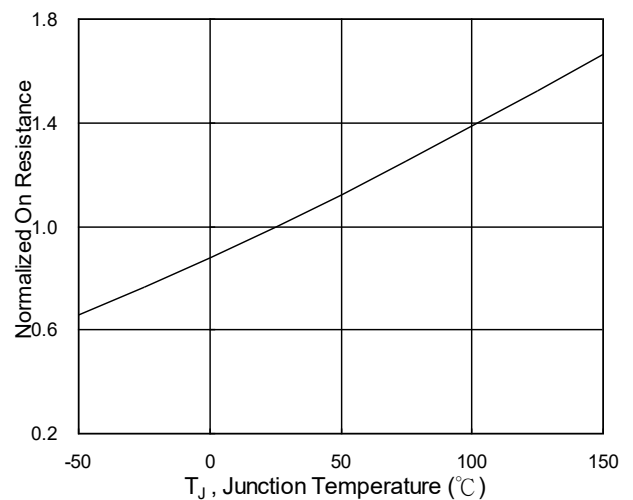


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

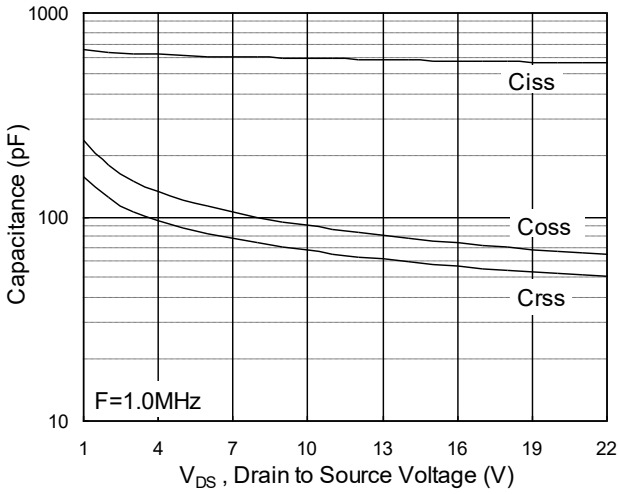


Fig.7 Capacitance

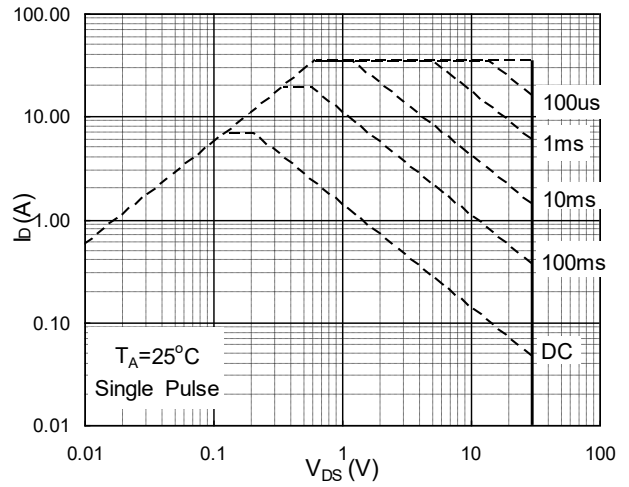


Fig.8 Safe Operating Area

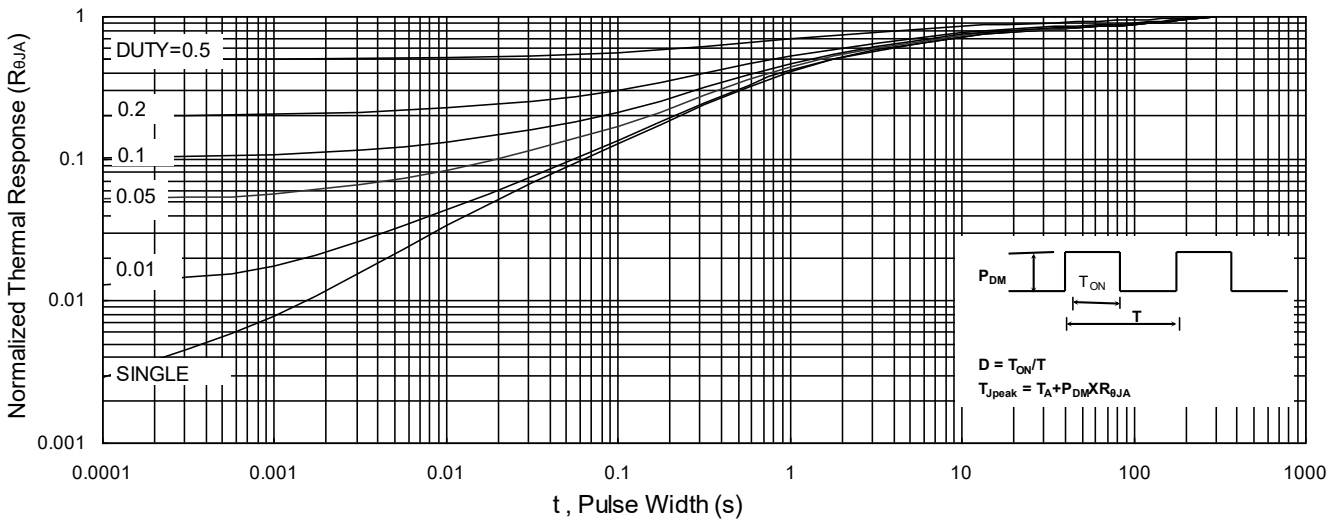


Fig.9 Normalized Maximum Transient Thermal Impedance

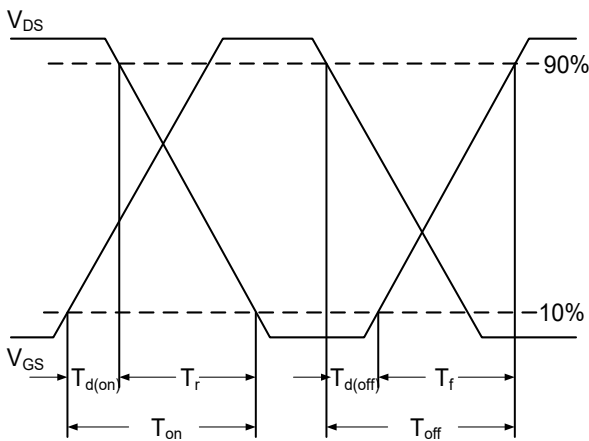


Fig.10 Switching Time Waveform



Fig.11 Unclamped Inductive Switching Waveform



SOP-8(SOIC-8) Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.05\text{mm}$.
 3. The pad layout is for reference purposes only.



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