# Broadband Low Noise Gain Block
# 0.03 - 8 GHz

**MAAM-011252-DIE**
**Rev. V2**

## Features

- 20 dB Flat Broadband Gain to 8 GHz
- Low Noise Figure:
  - 1.2 dB Noise Figure to 1.5 GHz
  - 1.7 dB Noise Figure @ 6 GHz
  - 2.3 dB Noise Figure @ 8 GHz
- High Linearity OIP3:
  - 36 dBm @ 1.5 GHz
  - 33 dBm @ 6 GHz
  - 30 dBm @ 8 GHz
- Internal Matching to 50 Ω
- Single Voltage Bias: 3 - 5 V
- Integrated Active Bias Circuit
- RoHS* Compliant

## Applications

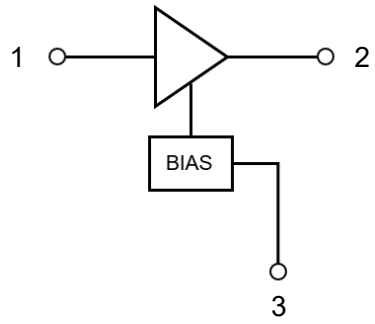
- ISM/MM

## Description

The MAAM-011252-DIE is a broadband high dynamic range, single stage MMIC LNA. This bare die is 0.795 x 0.715 mm. The amplifier is internally matched to provide flat gain and good return losses to 8 GHz without any external matching components. Only DC blocking capacitors and an RF choke with bypass capacitance is required.

This low noise amplifier has an integrated active bias circuit allowing direct connection to 3 V or 5 V bias and minimizing variations over temperature and process.

## Functional Block Diagram




## Pin Configuration[1]

| Pin # | Pin Name | Description |
|---|---|---|
| 1 | $RF_{IN}$ | RF Input |
| 2 | $RF_{OUT}$ / $V_{DD}$ | RF Output / Drain Voltage |
| 3 | NC | No Connection |

1. Bottom of die is RF and thermal ground.

## Ordering Information

| Part Number | Package |
|---|---|
| MAAM-011252-DIE | Bare Die |

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.



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## Electrical Specifications: $V_{DD}$ = 5 V, +25ºC, $Z_0$ = 50 Ω (all data is GSG probed)

| Parameter | Test Conditions | Units | Min. | Typ. | Max. |
|---|---|---|---|---|---|
| Gain | 0.03 - 8 GHz | dB | 18 | 20 | — |
| Noise Figure | 0.1 - 1.5 GHz<br>6.0 GHz<br>8.0 GHz | dB | — | 1.2<br>1.7<br>2.3 | — |
| Input Return Loss | 0.03 - 8 GHz | dB | — | 12 | — |
| Output Return Loss | 0.03 - 8 GHz | dB | — | 12 | — |
| Output IP3 | $P_{IN}$ = -15 dBm per tone, 6 MHz spacing<br>0.03 - 3 GHz<br>6 GHz<br>8 GHz | dBm | — | 34<br>33<br>30 | — |
| Output IP2 | $P_{IN}$ = -15 dBm per tone, 6 MHz spacing<br>0.03 - 3 GHz<br>6 GHz<br>8 GHz | dBm | — | 44<br>48<br>50 | — |
| Output P1dB | 0.03 - 3 GHz<br>6 GHz<br>8 GHz | dBm | — | 20<br>18<br>14 | — |
| Current | $I_{DD}$ | mA | — | 60 | 75 |

## Maximum Operating Ratings

| Parameter | Maximum |
|---|---|
| RF Input Power CW | 5 dBm |
| $V_{DD}$ | 6 V |
| $I_{DQ}$ | 100 mA |
| Operating Temperature | -40ºC to +85ºC |
| Junction Temperature[4,5] | +150ºC |

## Absolute Maximum Ratings[2,3]

| Parameter | Absolute Maximum |
|---|---|
| RF Input Power CW | 24 dBm |
| $V_{DD}$ | 7 V |
| Storage Temperature | -55ºC to +150ºC |

2. Exceeding any one or combination of these limits may cause permanent damage to this device.
3. MACOM does not recommend sustained operation near these survivability limits.
4. Operating at nominal conditions with $T_J \leq 150°C$ will ensure MTTF > 1 x $10^6$ hours.
5. Junction Temperature ($T_J$) = $T_C$ + $\Theta_{JC}$ * ((V * I) - ($P_{OUT}$ - $P_{IN}$))
   Typical thermal resistance ($\Theta_{JC}$) = 40°C/W
   a) For $T_C$ = 25°C,
   $T_J$ = 38°C @ 5 V, 60 mA
   b) For $T_C$ = 85°C,
   $T_J$ = 99°C @ 5 V, 70 mA

## Handling Procedures

Please observe the following precautions to avoid damage:

## Static Sensitivity

Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1B devices.

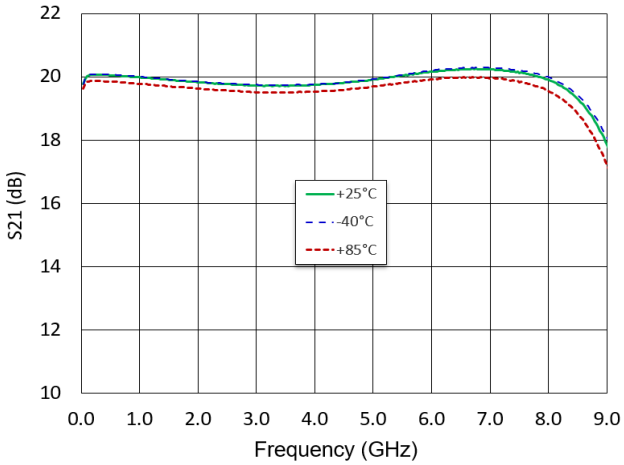


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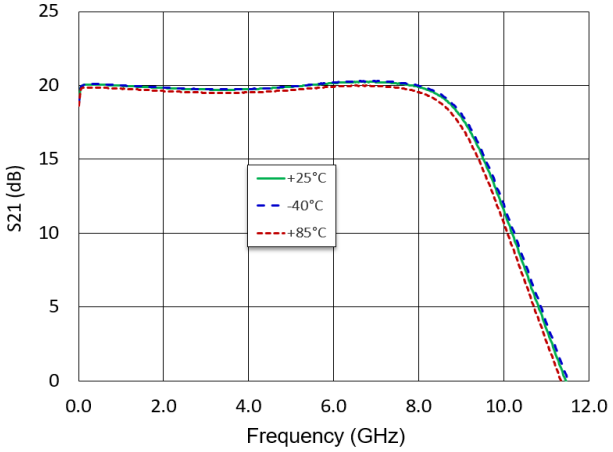
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## Typical Performance Curves @ 5 V / 60 mA, $Z_0$ = 50 Ω (all data is GSG probed)

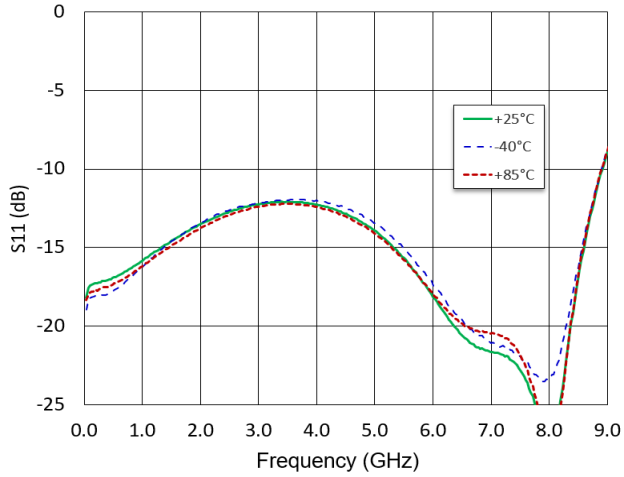
***Gain***



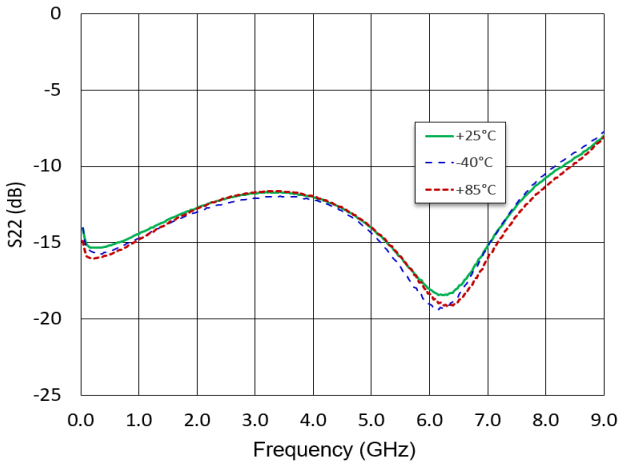

***Gain to 12 GHz***



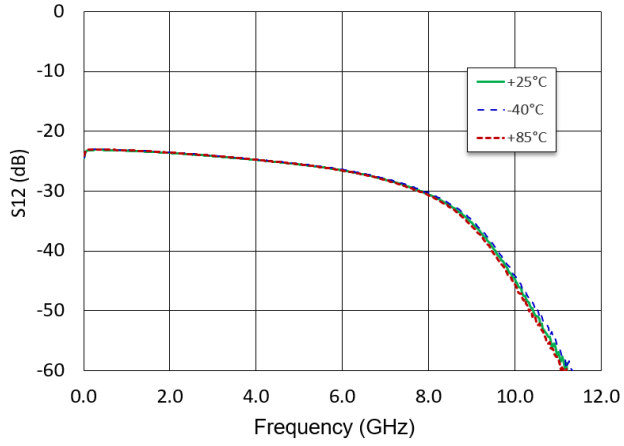

***Input Return Loss***



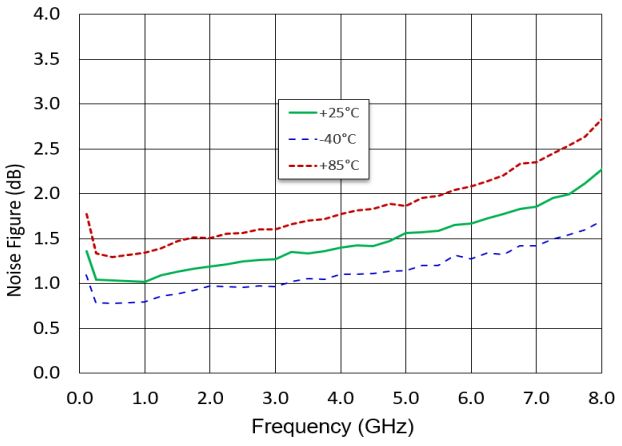

***Output Return Loss***




***Reverse Isolation***




***Noise Figure***



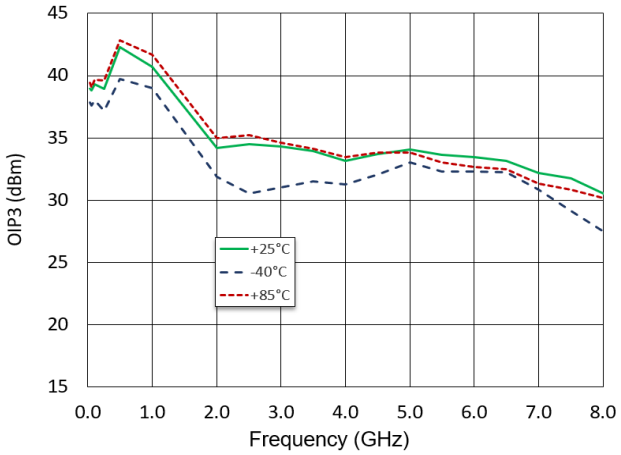



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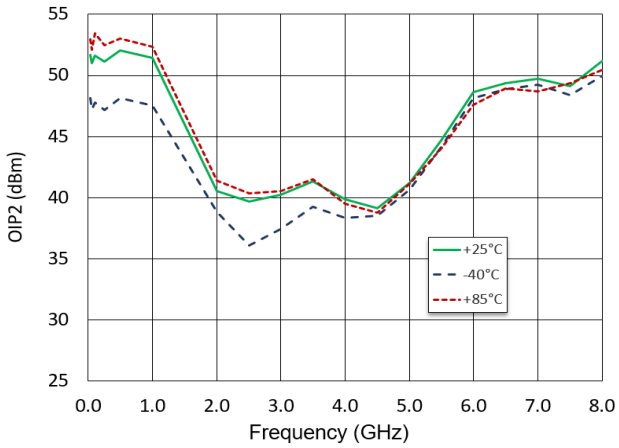
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## Typical Performance Curves @ 5 V / 60 mA, $Z_0$ = 50 Ω (all data is GSG probed)

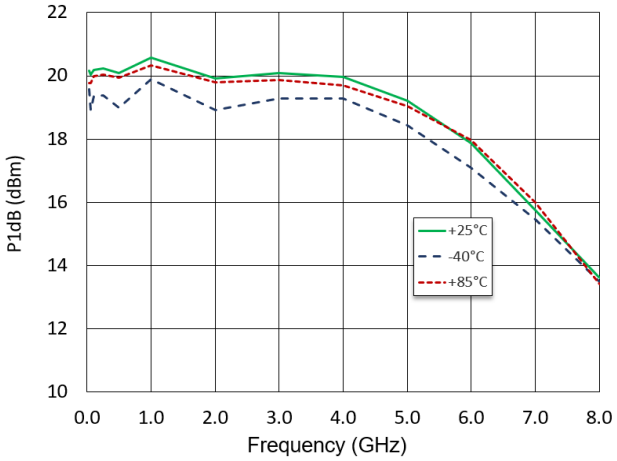
***OIP3 at $P_{IN}$ = -15 dBm/tone, 6MHz Spacing***




***OIP2 at $P_{IN}$ = -15 dBm/tone, 6MHz Spacing***




***P1dB***

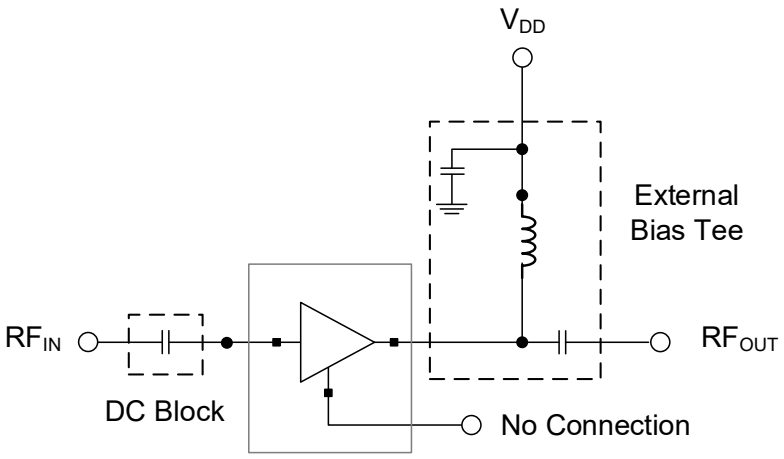




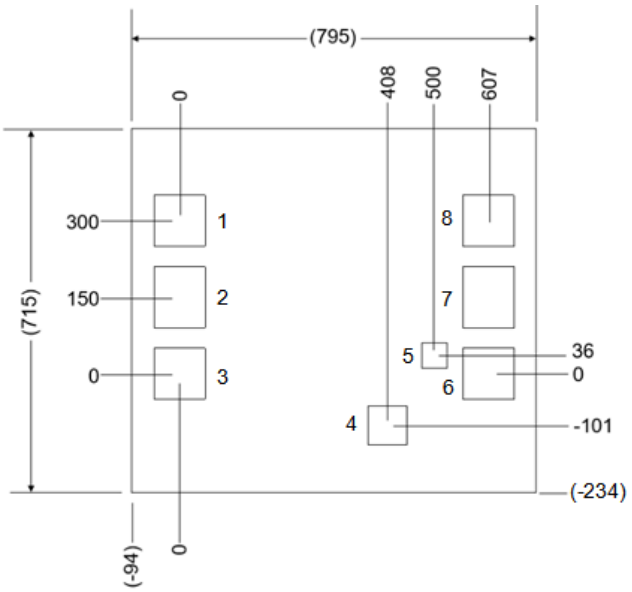

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## Typical Application Circuit




## Die Outline[6,7] (0.795 x 0.715 mm)




## *Bond Pad Dimensions (µm)*

| Pad # | Size (x) | Size (y) | Description |
|---|---|---|---|
| 1, 3, 6, 8 | 100 | 100 | GND |
| 2 | 100 | 120 | $RF_{IN}$ |
| 7 | 100 | 120 | $RF_{OUT}$ / $V_{DD}$ |
| 4 | 76 | 76 | No Connection |
| 5 | 50 | 50 | GND |

6. Dimensions are in microns.
7. GND bond pads 1, 3, 5, 6 and 8 are connected to the backside of the die through via holes. These bond pads do not require bond wires. Only pin 2 and 7 require bond wires.



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