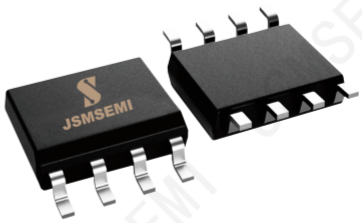
1 Description

The KP85302SGA is a high voltage, high speed power MOSFET drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 650 V.



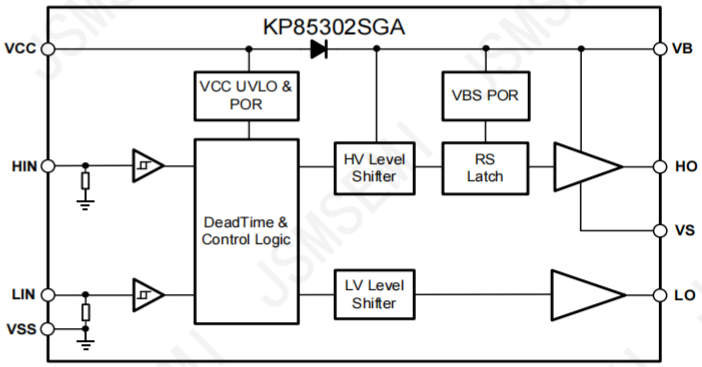
2 Features

- Floating channel designed for bootstrap operation
- Fully operational to +650 V
- 3.3V, 5V and 15V input logic compatible
- dV/dt noise Immunity ±50 V/ns
- Allowable negative Vs capability: -9V
- Undervoltage lockout for both channels
  --VCC UVLO threshold 8.7V/8.0V
  --VBS UVLO threshold 8.2V/7.4V
- Propagation delay
  --Ton/Toff = 250ns/150ns
  --Matching delay time 50ns
- Cross-conduction prevention logic
  --Deadtime 130ns
- Wide operating temperature range -40°C ~125°C
- Typically output Source/Sink current capability: 0.6A/1A
- RoSH compatible

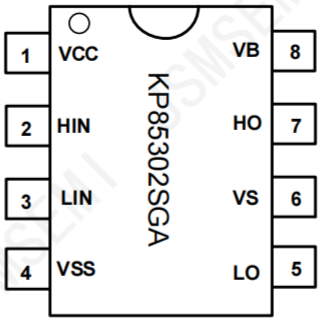
3 Application

- Motor Control
- Air Conditioners/ Washing Machines
- General Purpose Inverters
- Micro/Mini Inverter Drives

Functional Block Diagram



4 Function Pin Description



Lead Definitions

Number	Symbol	Description
1	V_{CC}	Low side and logic fixed supply
2	HIN	Logic input for high side gate driver output (HO), in phase
3	LIN	Logic input for low side gate driver output (LO), in phase
4	V_{SS}	Low side return
5	LO	Low side gate drive output
6	V_S	High side floating supply return
7	HO	High side gate drive output
8	V_B	High side floating supply

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship, Quantity	Green
KP85302SGA	SOP-8	85302	-40 to 125°C	3	T&R,4000	Rohs

5 Product Specifications

Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to VSS and an ambient temperature of 25°C.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	-0.3	650	V
V_S	High side floating supply return	V_B – 25	V_B + 0.3	
V_{HO}	High side gate drive output	V_S -0.3	V_B + 0.3	
V_{CC}	Low side and main power supply	-0.3	25	
V_{LO}	Low side gate drive output	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input of HIN & LIN	-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns

ESD Rating

Symbol	Definition	MIN.	MAX.	Units
ESD	HBM Model	2000	—	V
	Machine Model	1000	—	V

Rated Power

Symbol	Definition	MIN.	MAX.	Units
P_D	Package Power Dissipation @ TA ≤25°C	—	625	mW

Thermal Information

Symbol	Definition	MIN.	MAX.	Units
Rth_{JA}	Thermal Resistance, Junction to Ambient	--	200	°C/W
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and VSS are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to VSS and the ambient temperature is 25°C.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	VS + 10	VS + 20	V
V_S	High side floating supply return	-9	600	
V_{HO}	High side gate drive output	V_S	V_B	
V_{CC}	Low side and main power supply	10	20	
V_{LO}	Low side gate drive output	0	V_{CC}	
V_{IN}	Logic input of HIN & LIN	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note1：Transient negative VS can be used for VSS-50V with a pulse width of 50ns, guaranteed by design.

Electrical Characteristics

Valid for temperature range at T_A= 25°C, V_{CC}=V_B= 15V, C_L=1nF, unless otherwise specified

Dynamical Electrical Characteristics

t_{ON}	Turn-on propagation delay	—	250	300	ns	V_S=0V
t_{OFF}	Turn-off propagation delay	—	150	200	ns	V_S=600V
t_R	Turn-on rise time	—	50	100	ns	
t_F	Turn-off fall time	—	35	90	ns	
DT	Deadtime	—	130	260	ns	
MT	Matching delay(t_{ON},t_{OFF})	—	—	50	ns	
MT	Matching delay(t_{ON},t_{OFF})	—	—	60	ns	

Static Electrical Characteristics

Valid for temperature range at T_A= 25°C, V_{CC}=V_B= 15V, C_L=1nF, unless otherwise specified.

V_{CCUV+}	VCC supply UVLO threshold	7.7	8.7	9.7	V	
V_{CCUV-}		6.7	8.0	9.2	V	
$V_{CCUVHYS}$	hysteresis of V_{CC} UVLO	—	1	—	V	
V_{BSUV+}	VBS supply UVLO threshold	7.2	8.2	9.3	V	
V_{BSUV-}		6.3	7.3	8.4	V	
$V_{BSUVHYS}$	hysteresis of V_{BS} UVLO	—	0.9	—	V	
I_{LK}	High-side floating supply leakage current	—	—	50	μA	V_B=V_S=600V
I_{QBS}	Quiescent VB supply current	—	35	100	μA	V_{IN}=0V
I_{QCC}	Quiescent VCC supply current	—	60	150	μA	V_{IN}=0V
V_{IH}	Logic “1”(HIN&LIN) input voltage	2.5	—	—	V	VCC=10Vto 20V
V_{IL}	Logic “0” (HIN&LIN) input voltage	—	—	0.8	V	VCC=10Vto 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	0.2	V	I_O=0A
V_{OL}	Low level output voltage, V_O	—	—	0.2	V	I_O=0A
I_{IN+}	Logic “1” Input bias current	—	25	60	μA	HIN=5V, LIN=5V
I_{IN-}	Logic “0” Input bias current	—	—	5	μA	HIN=0V, LIN=0V
I_{O+}	Output high short circuit pulsed current	0.45	0.6	—	A	V_O=0V PW≤10us
I_{O-}	Output low short circuit pulsed current	0.8	1	—	A	V_O=15V PW≤10us

6 Function Description

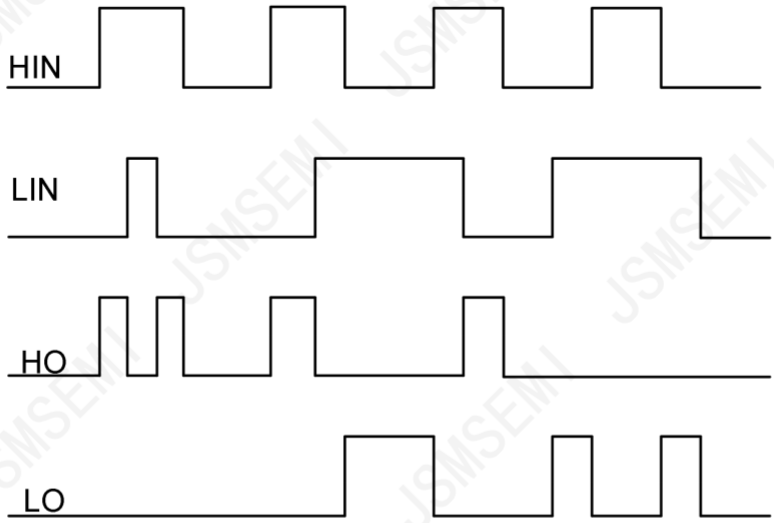


Figure 6-1 KP85302SGA Input and output timing waveform

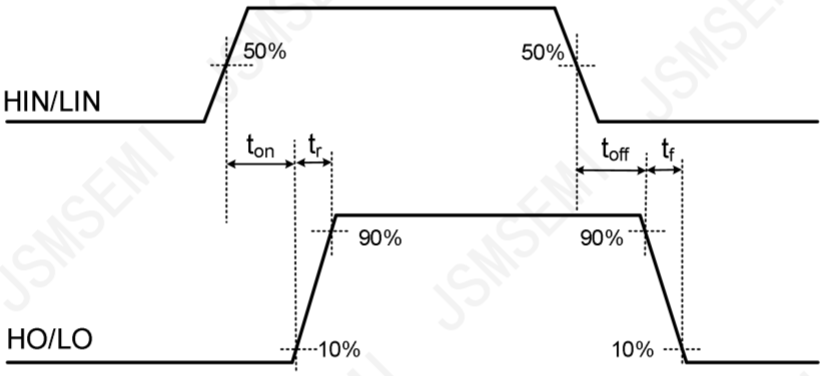


Figure 6-2 Propagation Time Waveform Definition

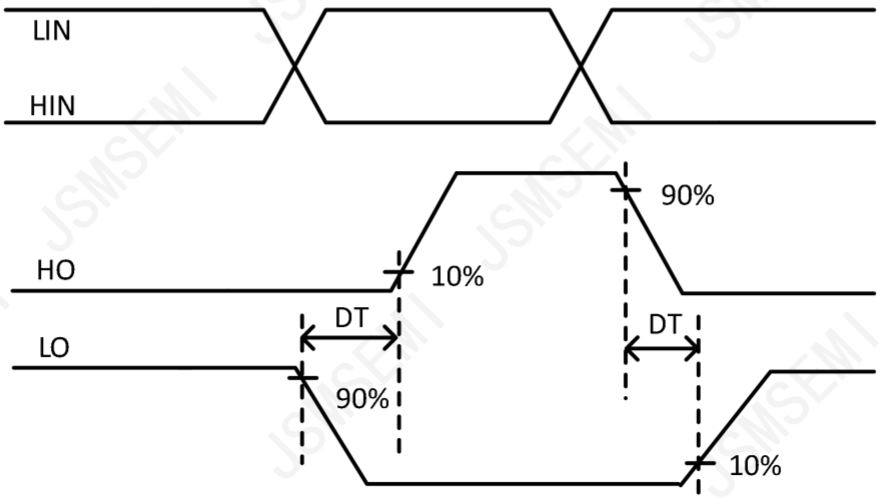


Figure 6-3 Cross Conduction Prevention Delay Time Waveform Definition

7 KP85302SGA

DescriptionFunction Block Diagram

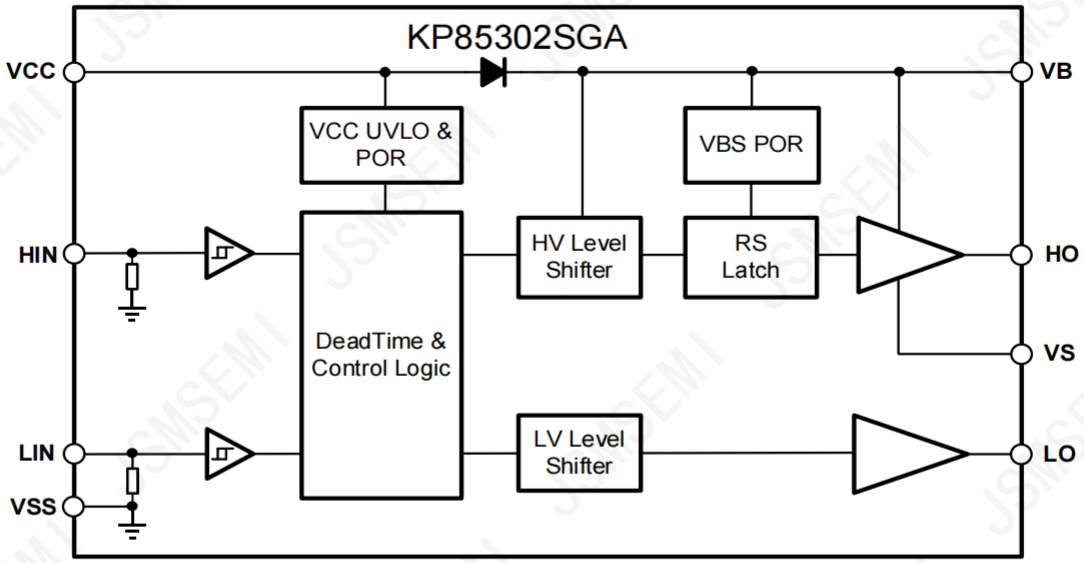


Figure7-1 Function Block Diagram of KP85302SGA

Application Diagram

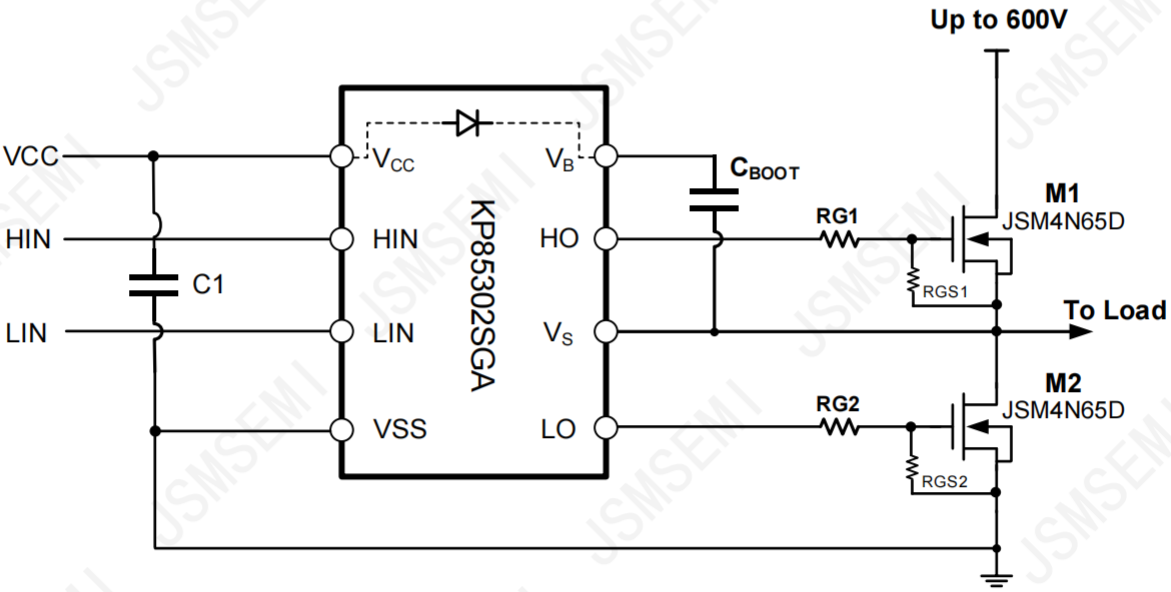


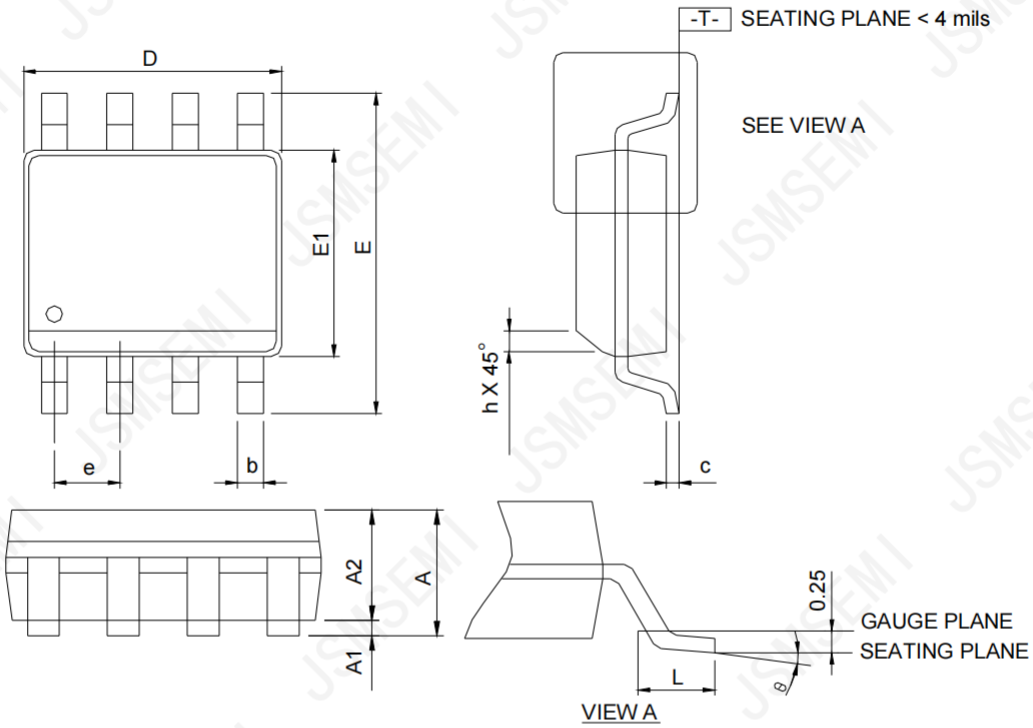
Figure7-2 Typical application circuit of KP85302SGA

Note:

For external bootstrap diodes, it is recommended to use FRD such as ES1J, and the bootstrap capacitance should not be less than 4.7UF.

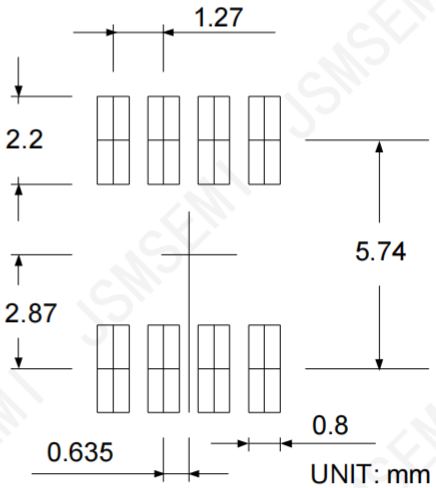
8 Package Information

SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

RECOMMENDED LAND PATTERN



Note: 1. Follow JEDEC MS-012 AA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Revision History

Rev.	Change	Date
V1.0	Initial version	2/23/2024

Important Notice

JSMSEMI Semiconductor (JSMSEMI) PRODUCTS ARE NEITHER DESIGNED NOR INTENDED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS UNLESS THE SPECIFIC JSMSEMI PRODUCTS ARE SPECIFICALLY DESIGNATED BY JSMSEMI FOR SUCH USE. BUYERS ACKNOWLEDGE AND AGREE THAT ANY SUCH USE OF JSMSEMI PRODUCTS WHICH JSMSEMI HAS NOT DESIGNATED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS IS SOLELY AT THE BUYER’S RISK.

JSMSEMI assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using JSMSEMI products.

Resale of JSMSEMI products or services with statements diferent from or beyond the parameters stated by JSMSEMI for that product or service voids all express and any implied warranties for the associated JSMSEMI product or s ervice. JSMSEMI is not responsible or liable for any such statements.

Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc.When designing equipment, refer to the "Delivery Specification" for the JSMSEMI product that you intend to use.

For additional information please contact Kevin@ jsmsemi.com or visit www.jsmsemi.com