MMBF170

N-Channel Enhancement Mode MOSFET

Features

- Surface-mounted package
- Advanced trench cell design
- Extremely low threshold voltage
- ESD protected (HBM > 2KV)

Quick reference

- BV ≧ 60 V
- P_{tot} ≦ 0.83 W
- I_D ≦ 0.5 A
- $R_{DS(ON)}$ ≦ 3 Ω @ V_{GS} = 10 V
- $R_{DS(ON)}$ ≦ 4 Ω @ V_{GS} = 4.5 V

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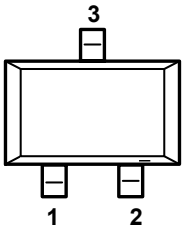
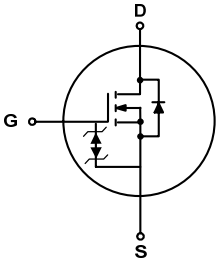




Top View

1 Gate(G) 2 Source(S) 3 Drain(D)

Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	T_A = 25 ℃	-	60	V
V_{GS}	Gate-Source Voltage	T_A = 25 ℃	-	± 20	V
I_D*	Drain Current	T_A = 25 ℃, V_{GS} = 10 V	-	0.5	A
I_{DM}*,**	Pulsed Drain Current	T_A = 25 ℃, V_{GS} = 10 V	-	1.7	A
P_{tot}*	Total Power Dissipation	T_A = 25 ℃	-	0.83	W
		T_A = 100 ℃	-	0.33	
T_{stg}	Storage Temperature		- 55	150	℃
T_J	Junction Temperature		-	150	℃
I_S*	Diode Forward Current	T_A = 25 ℃	-	0.4	A
$R_{\theta JA}$*	Thermal Resistance- Junction to Ambient		-	150	℃ / W

Notes : * Surface Mounted on 1 in$_2$ pad area, t ≤ 10 sec ** Pulse width ≤ 300 μs, duty cycle ≤ 2 %

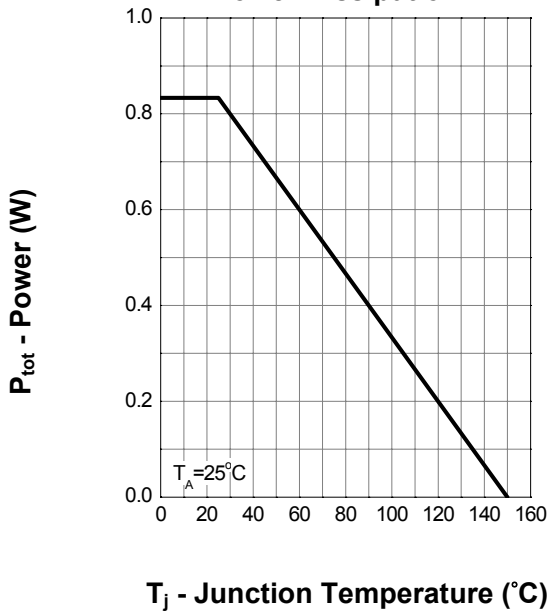
Electrical Characteristics (T_A = 25 °C Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 250 µA	60	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	1.0	1.6	2.5	V
I_{DSS}	Drain Leakage Current	V_{DS} = 48 V, V_{GS} = 0 V	-	-	1	µA
		T_J = 85 °C	-	-	30	µA
I_{GSS}	Gate Leakage Current	V_{GS} = ± 20 V, V_{DS} = 0 V	-	-	± 10	µA
$R_{DS(ON)}$[a]	On-State Resistance	V_{GS} = 10 V, I_{DS} = 0.4 A		1.9	3.0	Ω
		V_{GS} = 4.5 V, I_{DS} = 0.3 A	-	2.4	4.0	
Diode Characteristics						
V_{SD}[a]	Diode Forward Voltage	I_{SD} = 0.4 A, V_{GS} = 0 V	-	0.7	1.3	V
t_{rr}	Reverse Recovery Time	I_{SD} = 0.4 A, dI_{SD} / dt = 100 A / µs	-	40	-	ns
Q_{rr}	Reverse Recovery Charge		-	40	-	nC
Dynamic Characteristics[b]						
R_G	Gate Resistance	V_{GS} = V_{DS} = 0 V, F = 1 MHz	-	130	-	Ω
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 25 V Frequency = 1 MHz	-	30	-	pF
C_{oss}	Output Capacitance		-	4.2	-	
C_{rss}	Reverse Transfer Capacitance		-	3	-	
t_d(on)	Turn-on Delay Time	V_{DS} = 30 V, V_{GEN} = 10 V, R_G = 25 Ω, R_L = 150 Ω, I_{DS} = 0.2 A	-	3.9	9	ns
t_r	Turn-on Rise Time		-	3.5	8	
t_d(off)	Turn-off Delay Time		-	16	40	
t_f	Turn-off Fall Time		-	10	20	
Q_g	Total Gate Charge	V_{GS} = 4.5 V, V_{DS} = 10 V, I_{DS} = 0.4 A	-	305	-	pC
Q_{gs}	Gate-Source Charge		-	85	-	
Q_{gd}	Gate-Drain Charge		-	205	-	

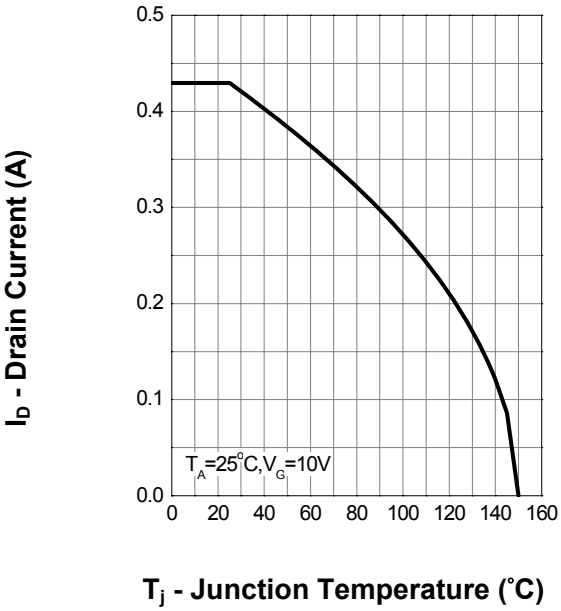
Notes：a : Pulse test ; pulse width ≤ 300 µs, duty cycle ≤ 2 % b : Guaranteed by design, not subject to production testing

Typical Characteristics

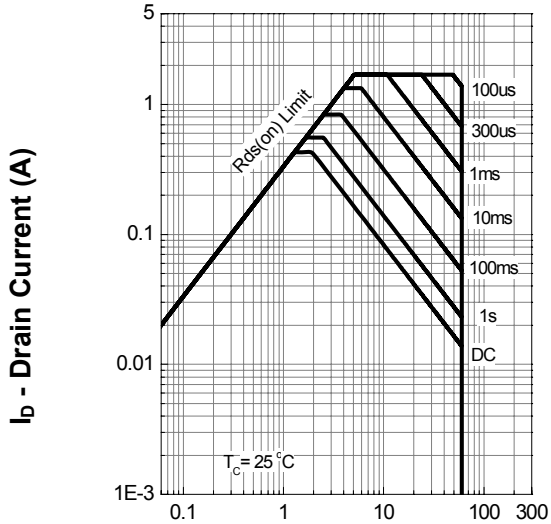
Power Dissipation



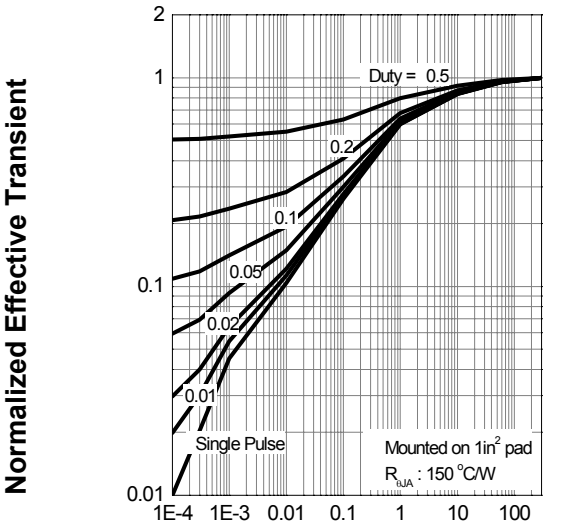
Drain Current



Safe Operation Area

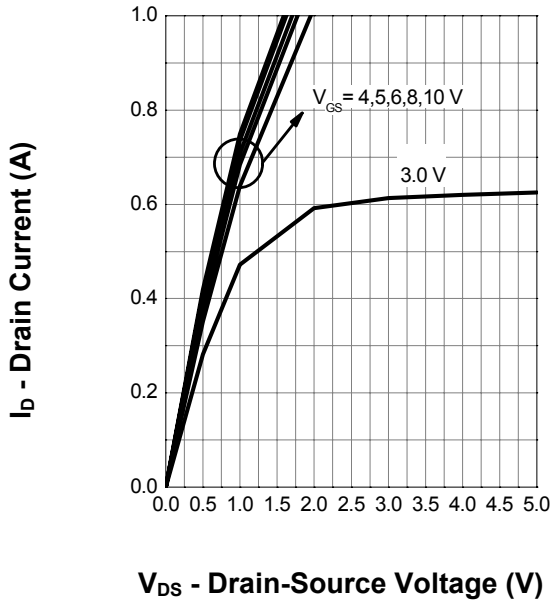


Thermal Transient Impedance

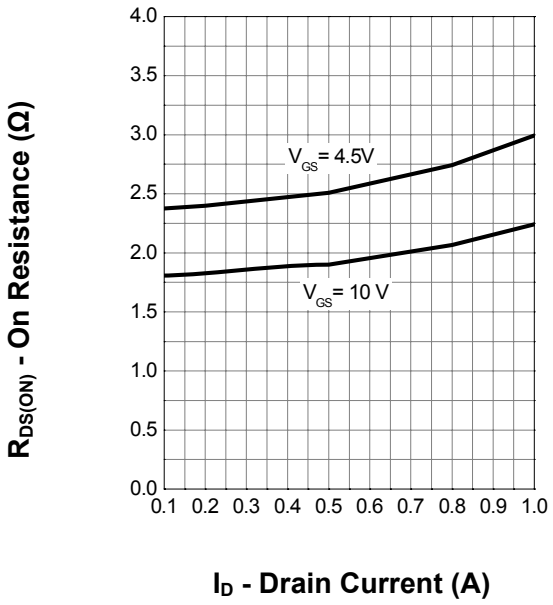


Typical Characteristics (cont.)

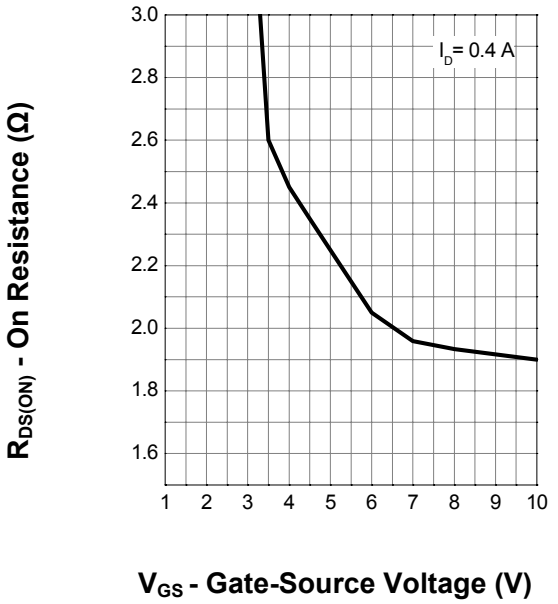
Output Characteristics



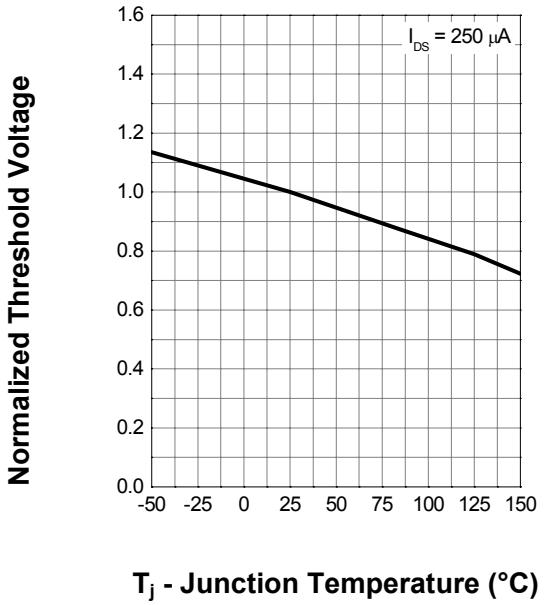
Drain-Source On Resistance



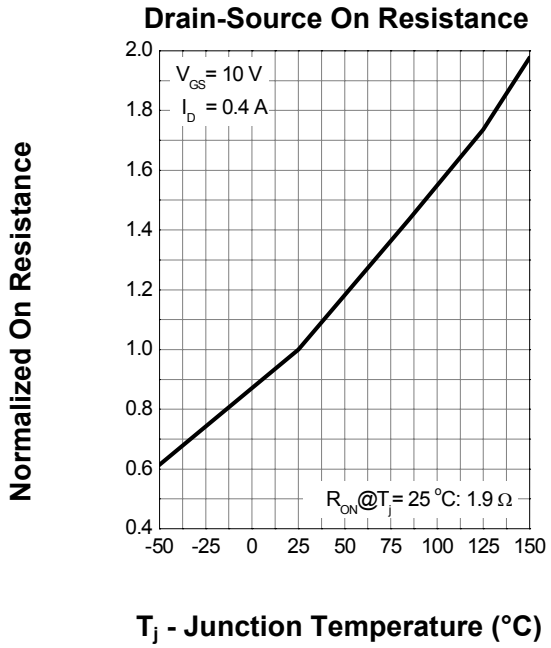
Transfer Characteristics

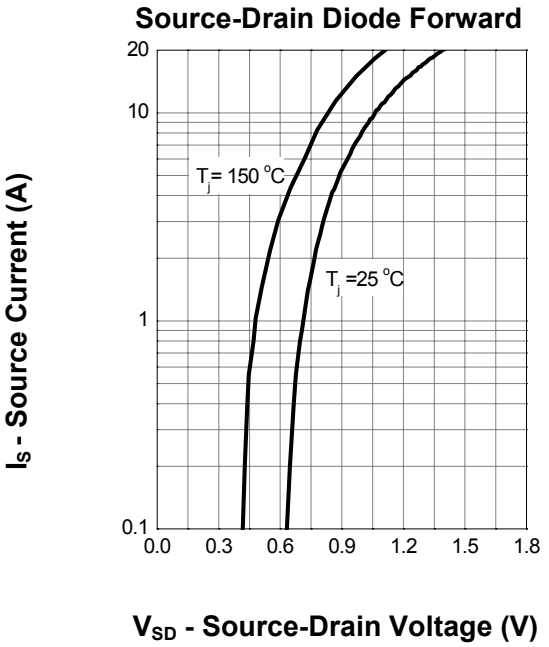


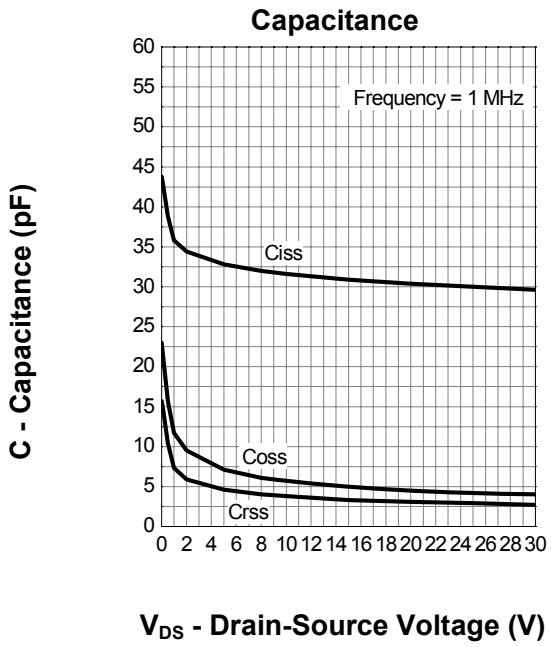
Gate Threshold Voltage

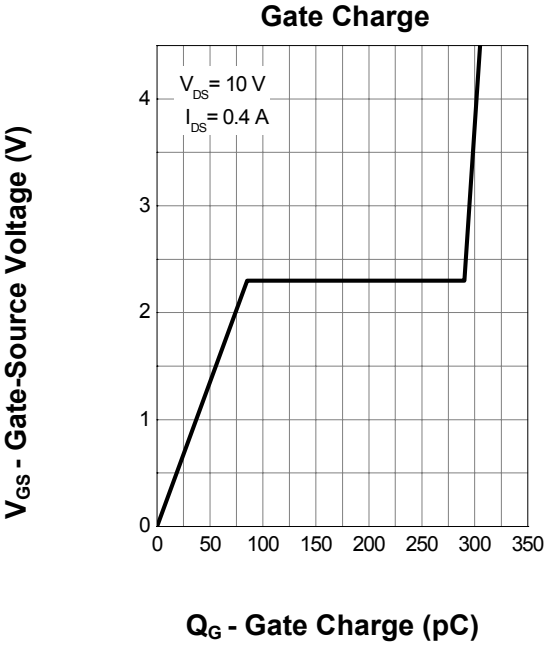


Typical Characteristics (cont.)









Package Dimensions

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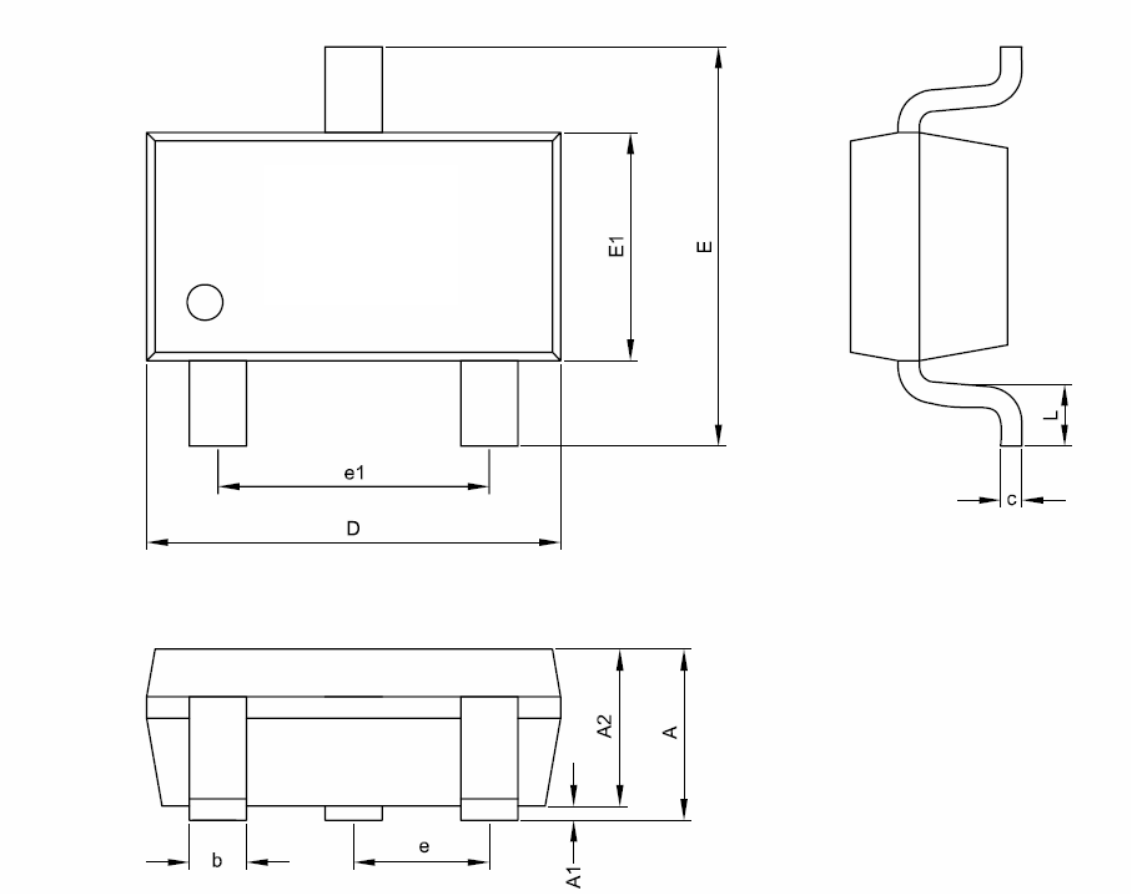

Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	—	1.12
A1	0.00	0.1
A2	0.90	1.02
D	2.90 BSC	
E	2.40 BSC	
E1	1.20	1.40
c	0.08	0.25
b	0.30	0.50
e	0.95 BSC	
e1	1.90 BSC	
L	0.20	0.60