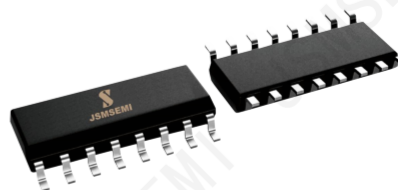


1、General Description

The 74HC40103D,653-JSM is an 8-bit synchronous down counter. It has control inputs for enabling or disabling the clock (CP), for clearing the counter to its maximum count and for presetting the counter either synchronously or asynchronously. In normal operation, the counter is decremented by one count on each positive-going transition of the clock (CP). Counting is inhibited when the terminal enable input (TE) is HIGH. The terminal count output (TC) goes LOW when the count reaches zero if TE is LOW, and remains LOW for one full clock period. When the synchronous preset enable input (PE) is LOW, data at the jam input (P0 to P7) is clocked into the counter on the next positive-going clock transition regardless of the state of TE. When the asynchronous preset enable input (PL) is LOW, data at the jam input (P0 to P7) is asynchronously forced into the counter regardless of the state of PE, TE, or CP. The jam inputs (P0 to P7) represent a single 8-bit binary word. When the master reset input (MR) is LOW, the counter is asynchronously cleared to its maximum count (decimal 255) regardless of the state of any other input. If all control inputs except TE are HIGH at the time of zero count, the counters will jump to the maximum count, giving accounting sequence of 256 clock pulses long. Device may be cascaded using the TE input and the TC output, in either a synchronous or ripple mode. Input include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .



SOP-16

Features:

- Cascadable
- Synchronous or asynchronous preset
- Low-power dissipation
- CMOS input levels
- Specified from -40°C to +125°C
- Packaging information: SOP16

Ordering Information

Order number	Package	Operation Temperature Range	MSL Grade	Ship, Quantity	Green
74HC40103D,653-JSM	SOP-16	-40 to 125°C	3	T&R,2500	Rohs

2、Block Diagram And Pin Description

2.1、Block Diagram

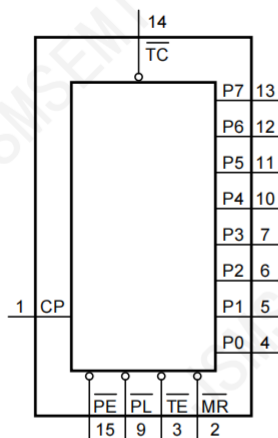


Figure 1. Functional diagram

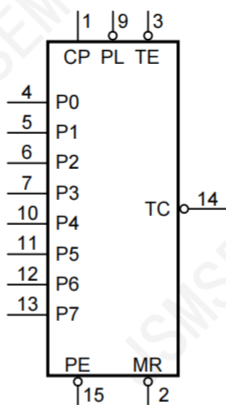


Figure 2. Logic symbol

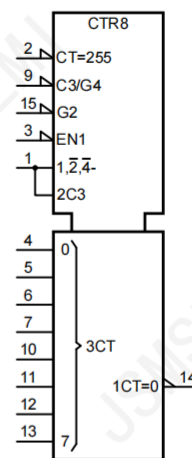


Figure 3. IEC logic symbol

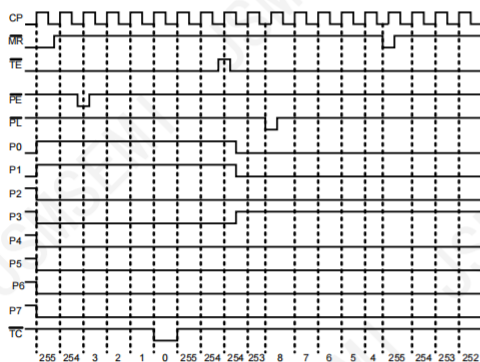


Figure 4. Timing diagram

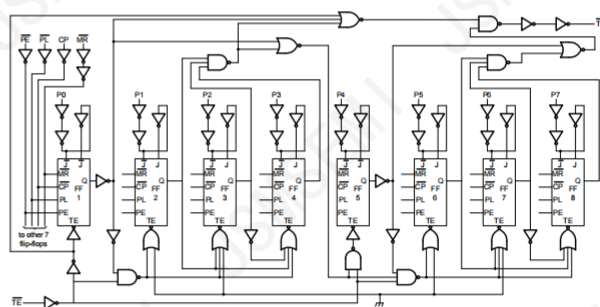
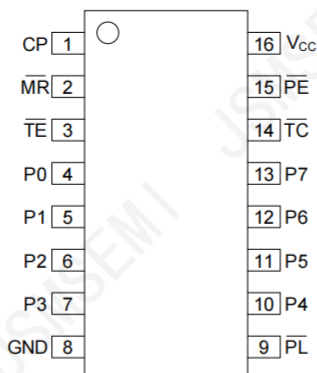


Figure 5. Logic diagram

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	CP	clock input (LOW-to-HIGH, edge-triggered)
2	$\overline{\text{MR}}$	asynchronous master reset input (active LOW)
3	$\overline{\text{TE}}$	terminal enable input (active LOW)
4	P0	jam input 0
5	P1	jam input 1
6	P2	jam input 2
7	P3	jam input 3
8	GND	ground (0 V)
9	$\overline{\text{PL}}$	asynchronous preset enable input (active LOW)
10	P4	jam input 4
11	P5	jam input 5
12	P6	jam input 6
13	P7	jam input 7
14	$\overline{\text{TC}}$	terminal count output (active LOW)
15	$\overline{\text{PE}}$	synchronous preset enable input (active LOW)
16	V _{CC}	positive supply voltage

2.4、Function table

Control inputs				Preset mode	Action
$\overline{\text{MR}}$	$\overline{\text{PL}}$	$\overline{\text{PE}}$	$\overline{\text{TE}}$		
L	X	X	X	asynchronous	clear to maximum count
H	L	X	X	asynchronous	preset asynchronously
	H	L	X	synchronous	preset on next LOW-to HIGH clock transition
		H	L	synchronous	count down
			H	synchronous	inhibit counter

Note:

H=HIGH voltage level; L=LOW voltage level; X=don't care.

Clock connected to CP.

Synchronous operation: changes occur on the LOW-to-HIGH CP transition.

Jam inputs: MSD=P7, LSD=P0.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

($T_{amb}=25^{\circ}\text{C}$, voltage are referenced to GND (ground=0V), unless otherwise specified)

Characteristic	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+7.0	V
input clamping current	I_{IK}	$V_I < -0.5\text{V}$ or $V_I > V_{CC} + 0.5\text{V}^{[1]}$	-	± 20	mA
output clamping current	I_{OK}	$V_O < -0.5\text{V}$ or $V_O > V_{CC} + 0.5\text{V}^{[1]}$	-	± 20	mA
output current	I_O	$V_O = -0.5\text{V}$ to $V_{CC} + 0.5\text{V}$	-	± 25	mA
supply current	I_{CC}	-	-	+50	mA
ground current	I_{GND}	-	-50	-	mA
storage temperature	T_{stg}	-	-65	+150	$^{\circ}\text{C}$
total power dissipation	P_{tot}	-	-	500	mW
soldering temperature	T_L	10s	260		$^{\circ}\text{C}$

Note:

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{CC}=2.0\text{V}$	-	-	625	ns/V
		$V_{CC}=4.5\text{V}$	-	1.67	139	ns/V
		$V_{CC}=6.0\text{V}$	-	-	83	ns/V
ambient temperature	T_{amb}	-	-40	-	+125	$^{\circ}\text{C}$

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	$V_{CC}=2.0V$		1.5	1.2	-	V
		$V_{CC}=4.5V$		3.15	2.4	-	V
		$V_{CC}=6.0V$		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	$V_{CC}=2.0V$		-	0.8	0.5	V
		$V_{CC}=4.5V$		-	2.1	1.35	V
		$V_{CC}=6.0V$		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	$V_I=V_{IH}$ or V_{IL}	$I_O=-20\mu A$; $V_{CC}=2.0V$	1.9	2.0	-	V
			$I_O=-20\mu A$; $V_{CC}=4.5V$	4.4	4.5	-	V
			$I_O=-20\mu A$; $V_{CC}=6.0V$	5.9	6.0	-	V
			$I_O=-4.0mA$; $V_{CC}=4.5V$	3.98	4.32	-	V
			$I_O=-5.2mA$; $V_{CC}=6.0V$	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	$V_I=V_{IH}$ or V_{IL}	$I_O=20\mu A$; $V_{CC}=2.0V$	-	0	0.1	V
			$I_O=20\mu A$; $V_{CC}=4.5V$	-	0	0.1	V
			$I_O=20\mu A$; $V_{CC}=6.0V$	-	0	0.1	V
			$I_O=4.0mA$; $V_{CC}=4.5V$	-	0.15	0.26	V
			$I_O=5.2mA$; $V_{CC}=6.0V$	-	0.16	0.26	V
input leakage current	I_I	$V_I=V_{CC}$ or GND; $V_{CC}=6.0V$		-	-	± 1.0	μA
supply current	I_{CC}	$V_I=V_{CC}$ or GND; $I_O=0A$; $V_{CC}=6.0V$		-	-	8.0	μA
input capacitance	C_I	-		-	3.5	-	pF

3.3.2、DC Characteristics 2

($T_{amb}=-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	$V_{CC}=2.0V$		1.5	-	-	V
		$V_{CC}=4.5V$		3.15	-	-	V
		$V_{CC}=6.0V$		4.2	-	-	V
LOW-level input voltage	V_{IL}	$V_{CC}=2.0V$		-	-	0.5	V
		$V_{CC}=4.5V$		-	-	1.35	V
		$V_{CC}=6.0V$		-	-	1.8	V
HIGH-level output voltage	V_{OH}	$V_I=V_{IH}$ or V_{IL}	$I_O=-20\mu A; V_{CC}=2.0V$	1.9	-	-	V
			$I_O=-20\mu A; V_{CC}=4.5V$	4.4	-	-	V
			$I_O=-20\mu A; V_{CC}=6.0V$	5.9	-	-	V
			$I_O=-4.0mA; V_{CC}=4.5V$	3.84	-	-	V
			$I_O=-5.2mA; V_{CC}=6.0V$	5.34	-	-	V
LOW-level output voltage	V_{OL}	$V_I=V_{IH}$ or V_{IL}	$I_O=20\mu A; V_{CC}=2.0V$	-	-	0.1	V
			$I_O=20\mu A; V_{CC}=4.5V$	-	-	0.1	V
			$I_O=20\mu A; V_{CC}=6.0V$	-	-	0.1	V
			$I_O=4.0mA; V_{CC}=4.5V$	-	-	0.33	V
			$I_O=5.2mA; V_{CC}=6.0V$	-	-	0.33	V
input leakage current	I_I	$V_I=V_{CC}$ or GND; $V_{CC}=6.0V$		-	-	± 1.0	μA
supply current	I_{CC}	$V_I=V_{CC}$ or GND; $I_O=0A; V_{CC}=6.0V$		-	-	80	μA

3.3.3、DC Characteristics 3

($T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	$V_{CC}=2.0V$		1.5	-	-	V
		$V_{CC}=4.5V$		3.15	-	-	V
		$V_{CC}=6.0V$		4.2	-	-	V
LOW-level input voltage	V_{IL}	$V_{CC}=2.0V$		-	-	0.5	V
		$V_{CC}=4.5V$		-	-	1.35	V
		$V_{CC}=6.0V$		-	-	1.8	V
HIGH-level output voltage	V_{OH}	$V_I=V_{IH}$ or V_{IL}	$I_O=-20\mu A$; $V_{CC}=2.0V$	1.9	-	-	V
			$I_O=-20\mu A$; $V_{CC}=4.5V$	4.4	-	-	V
			$I_O=-20\mu A$; $V_{CC}=6.0V$	5.9	-	-	V
			$I_O=-4.0mA$; $V_{CC}=4.5V$	3.7	-	-	V
			$I_O=-5.2mA$; $V_{CC}=6.0V$	5.2	-	-	V
LOW-level output voltage	V_{OL}	$V_I=V_{IH}$ or V_{IL}	$I_O=20\mu A$; $V_{CC}=2.0V$	-	-	0.1	V
			$I_O=20\mu A$; $V_{CC}=4.5V$	-	-	0.1	V
			$I_O=20\mu A$; $V_{CC}=6.0V$	-	-	0.1	V
			$I_O=4.0mA$; $V_{CC}=4.5V$	-	-	0.4	V
			$I_O=5.2mA$; $V_{CC}=6.0V$	-	-	0.4	V
input leakage current	I_I	$V_I=V_{CC}$ or GND; $V_{CC}=6.0V$		-	-	± 1.0	μA
supply current	I_{CC}	$V_I=V_{CC}$ or GND; $I_O=0A$; $V_{CC}=6.0V$		-	-	160	μA

3.3.4、AC Characteristics 1

($T_{amb} = 25^{\circ}\text{C}$, $\text{GND} = 0\text{V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
propagation delay	t _{pd}	CP to $\overline{\text{TC}}$; see Figure 6 ^[1]	V _{CC} =2.0V	-	96	300	ns
			V _{CC} =4.5V	-	35	60	ns
			V _{CC} =5.0V; C _L =15pF	-	30	-	ns
			V _{CC} =6.0V	-	28	51	ns
		$\overline{\text{TE}}$ to $\overline{\text{TC}}$; see Figure 7	V _{CC} =2.0V	-	50	175	ns
			V _{CC} =4.5V	-	18	35	ns
			V _{CC} =6.0V	-	14	30	ns
		$\overline{\text{PL}}$ to $\overline{\text{TC}}$; see Figure 8	V _{CC} =2.0V	-	102	315	ns
			V _{CC} =4.5V	-	37	63	ns
			V _{CC} =6.0V	-	30	53	ns
HIGH to LOW propagation delay	t _{PHL}	$\overline{\text{MR}}$ to $\overline{\text{TC}}$; see Figure 8	V _{CC} =2.0V	-	83	275	ns
			V _{CC} =4.5V	-	30	55	ns
			V _{CC} =6.0V	-	24	47	ns
transition time	t _t	see Figure 7 ^[2]	V _{CC} =2.0V	-	19	75	ns
			V _{CC} =4.5V	-	7	15	ns
			V _{CC} =6.0V	-	6	13	ns

pulse width	t_w	CP HIGH or LOW; see Figure 6	$V_{CC}=2.0V$	165	22	-	ns
			$V_{CC}=4.5V$	33	8	-	ns
			$V_{CC}=6.0V$	28	6	-	ns
		$\overline{MR}$ LOW; see Figure 8	$V_{CC}=2.0V$	125	39	-	ns
			$V_{CC}=4.5V$	25	14	-	ns
			$V_{CC}=6.0V$	21	11	-	ns
		$\overline{PL}$ LOW; see Figure 8	$V_{CC}=2.0V$	125	33	-	ns
			$V_{CC}=4.5V$	25	12	-	ns
			$V_{CC}=6.0V$	21	10	-	ns
recovery time	t_{rec}	$\overline{MR}$ to CP, $\overline{PL}$ to CP; see Figure 9	$V_{CC}=2.0V$	100	-	-	ns
			$V_{CC}=4.5V$	20	-	-	ns
			$V_{CC}=6.0V$	18	-	-	ns
set-up time	t_{su}	$\overline{PE}$ to CP; see Figure 10	$V_{CC}=2.0V$	75	-	-	ns
			$V_{CC}=4.5V$	15	-	-	ns
			$V_{CC}=6.0V$	13	-	-	ns
		$\overline{TE}$ to CP; see Figure 11	$V_{CC}=2.0V$	150	-	-	ns
			$V_{CC}=4.5V$	30	-	-	ns
			$V_{CC}=6.0V$	26	-	-	ns
		Pn to CP; see Figure 10	$V_{CC}=2.0V$	75	-	-	ns
			$V_{CC}=4.5V$	15	-	-	ns
			$V_{CC}=6.0V$	13	-	-	ns
hold time	t_h	$\overline{PE}$ to CP; see Figure 10	$V_{CC}=2.0V$	0	-	-	ns
			$V_{CC}=4.5V$	0	-	-	ns
			$V_{CC}=6.0V$	0	-	-	ns
		$\overline{TE}$ to CP; see Figure 11	$V_{CC}=2.0V$	0	-	-	ns
		see Figure 11	$V_{CC}=4.5V$	0	-	-	ns
			$V_{CC}=6.0V$	0	-	-	ns
		Pn to CP; see Figure 10	$V_{CC}=2.0V$	0	-	-	ns
			$V_{CC}=4.5V$	0	-	-	ns
			$V_{CC}=6.0V$	0	-	-	ns
maximum frequency	f_{max}	see Figure 6	$V_{CC}=2.0V$	3.0	10	-	MHz
			$V_{CC}=4.5V$	15	29	-	MHz
			$V_{CC}=5.0V; C_L=15pF$	-	32	-	MHz
			$V_{CC}=6.0V$	18	35	-	MHz
power dissipation capacitance	C_{PD}	$V_I=GND$ to $V_{CC}^{[3]}$		-	24	-	pF

Note: [1] t_{pd} is the same as t_{PHL} , t_{PLH} .

[2] t_t is the same as t_{THL} , t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

3.3.5、AC Characteristics 2

($T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $GND=0V$; $t_r=t_f=6\text{ ns}$; $C_L=50\text{ pF}$, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	t_{pd}	CP to $\overline{T}C$; see Figure 6 ^[1]	$V_{CC}=2.0V$	-	-	375	ns
			$V_{CC}=4.5V$	-	-	75	ns
			$V_{CC}=6.0V$	-	-	64	ns
		$\overline{T}E$ to $\overline{T}C$; see Figure 7	$V_{CC}=2.0V$	-	-	220	ns
			$V_{CC}=4.5V$	-	-	44	ns
			$V_{CC}=6.0V$	-	-	37	ns
		$\overline{P}L$ to $\overline{T}C$; see Figure 8	$V_{CC}=2.0V$	-	-	395	ns
			$V_{CC}=4.5V$	-	-	79	ns
			$V_{CC}=6.0V$	-	-	40	ns
HIGH to LOW propagation delay	t_{PHL}	$\overline{MR}$ to $\overline{T}C$; see Figure 8	$V_{CC}=2.0V$	-	-	345	ns
			$V_{CC}=4.5V$	-	-	69	ns
			$V_{CC}=6.0V$	-	-	59	ns
transition time	t_t	see Figure 7 ^[2]	$V_{CC}=2.0V$	-	-	95	ns
			$V_{CC}=4.5V$	-	-	19	ns
			$V_{CC}=6.0V$	-	-	16	ns
pulse width	t_w	CP HIGH or LOW; see Figure 6	$V_{CC}=2.0V$	205	-	-	ns
			$V_{CC}=4.5V$	41	-	-	ns
			$V_{CC}=6.0V$	35	-	-	ns
		$\overline{MR}$ LOW; see Figure 8	$V_{CC}=2.0V$	155	-	-	ns
			$V_{CC}=4.5V$	31	-	-	ns
			$V_{CC}=6.0V$	26	-	-	ns
		$\overline{P}L$ LOW; see Figure 8	$V_{CC}=2.0V$	155	-	-	ns
			$V_{CC}=4.5V$	31	-	-	ns
			$V_{CC}=6.0V$	26	-	-	ns
recovery time	t_{rec}	$\overline{MR}$ to CP, $\overline{P}L$ to CP; see Figure 9	$V_{CC}=2.0V$	120	-	-	ns
			$V_{CC}=4.5V$	24	-	-	ns
			$V_{CC}=6.0V$	22	-	-	ns
set-up time	t_{su}	$\overline{P}E$ to CP; see Figure 10	$V_{CC}=2.0V$	95	-	-	ns
			$V_{CC}=4.5V$	19	-	-	ns
		$\overline{T}E$ to CP; see Figure 11	$V_{CC}=6.0V$	16	-	-	ns
			$V_{CC}=2.0V$	190	-	-	ns
			$V_{CC}=4.5V$	38	-	-	ns
			$V_{CC}=6.0V$	33	-	-	ns
		P_n to CP; see Figure 10	$V_{CC}=2.0V$	95	-	-	ns
			$V_{CC}=4.5V$	19	-	-	ns
			$V_{CC}=6.0V$	16	-	-	ns
hold time	t_h	$\overline{P}E$ to CP; see Figure 10	$V_{CC}=2.0V$	0	-	-	ns
			$V_{CC}=4.5V$	0	-	-	ns
			$V_{CC}=6.0V$	0	-	-	ns
		$\overline{T}E$ to CP; see Figure 11	$V_{CC}=2.0V$	0	-	-	ns
			$V_{CC}=4.5V$	0	-	-	ns
			$V_{CC}=6.0V$	0	-	-	ns
		P_n to CP; see Figure 10	$V_{CC}=2.0V$	0	-	-	ns
			$V_{CC}=4.5V$	0	-	-	ns
			$V_{CC}=6.0V$	0	-	-	ns

maximum frequency	$f_{\max}$	see Figure 6	$V_{CC}=2.0V$	2.4	-	-	MHz
			$V_{CC}=4.5V$	12	-	-	MHz
			$V_{CC}=6.0V$	14	-	-	MHz

Note: [1] t_{pd} is the same as t_{PHL} , t_{PLH} .

[2] t_t is the same as t_{THL} , t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i =input frequency in MHz;

f_o =output frequency in MHz;

C_L =output load capacitance in pF;

V_{CC} =supply voltage in V;

N =number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ =sum of outputs.

3.3.6、AC Characteristics 3

($T_{amb}=-40^{\circ}C$ to $+125^{\circ}C$, GND=0V; $t_r=t_f=6$ ns; $C_L=50$ pF, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
propagation delay	t_{pd}	CP to $\overline{TC}$; see Figure 6 ^[1]	$V_{CC}=2.0V$	-	-	450 ns
			$V_{CC}=4.5V$	-	-	90 ns
			$V_{CC}=6.0V$	-	-	77 ns
		$\overline{TE}$ to $\overline{TC}$; see Figure 7	$V_{CC}=2.0V$	-	-	265 ns
			$V_{CC}=4.5V$	-	-	53 ns
			$V_{CC}=6.0V$	-	-	45 ns
		$\overline{PL}$ to $\overline{TC}$; see Figure 8	$V_{CC}=2.0V$	-	-	475 ns
			$V_{CC}=4.5V$	-	-	95 ns
			$V_{CC}=6.0V$	-	-	81 ns
HIGH to LOW propagation delay	t_{PHL}	$\overline{MR}$ to $\overline{TC}$; see Figure 8	$V_{CC}=2.0V$	-	-	415 ns
			$V_{CC}=4.5V$	-	-	83 ns
			$V_{CC}=6.0V$	-	-	71 ns
transition time	t_t	see Figure 7 ^[2]	$V_{CC}=2.0V$	-	-	110 ns
			$V_{CC}=4.5V$	-	-	22 ns
			$V_{CC}=6.0V$	-	-	19 ns
pulse width	t_w	CP HIGH or LOW; see Figure 6	$V_{CC}=2.0V$	250	-	- ns
			$V_{CC}=4.5V$	50	-	- ns
			$V_{CC}=6.0V$	43	-	- ns
		$\overline{MR}$ LOW; see Figure 8	$V_{CC}=2.0V$	190	-	- ns
			$V_{CC}=4.5V$	38	-	- ns
			$V_{CC}=6.0V$	32	-	- ns
		$\overline{PL}$ LOW;	$V_{CC}=2.0V$	190	-	- ns

		see Figure 8	$V_{CC}=4.5V$	38	-	-	ns
			$V_{CC}=6.0V$	32	-	-	ns
			$V_{CC}=2.0V$	132	-	-	ns
recovery time	t_{rec}	$\overline{MR}$ to CP, $\overline{PL}$ to CP; see Figure 9	$V_{CC}=4.5V$	26	-	-	ns
			$V_{CC}=6.0V$	24	-	-	ns
set-up time	t_{su}	$\overline{PE}$ to CP; see Figure 10	$V_{CC}=2.0V$	110	-	-	ns
			$V_{CC}=4.5V$	22	-	-	ns
			$V_{CC}=6.0V$	19	-	-	ns
		$\overline{TE}$ to CP; see Figure 11	$V_{CC}=2.0V$	225	-	-	ns
			$V_{CC}=4.5V$	45	-	-	ns
			$V_{CC}=6.0V$	38	-	-	ns
		Pn to CP; see Figure 10	$V_{CC}=2.0V$	110	-	-	ns
			$V_{CC}=4.5V$	22	-	-	ns
			$V_{CC}=6.0V$	19	-	-	ns
hold time	t_h	$\overline{PE}$ to CP; see Figure 10	$V_{CC}=2.0V$	0	-	-	ns
			$V_{CC}=4.5V$	0	-	-	ns
			$V_{CC}=6.0V$	0	-	-	ns
		$\overline{TE}$ to CP; see Figure 11	$V_{CC}=2.0V$	0	-	-	ns
			$V_{CC}=4.5V$	0	-	-	ns
			$V_{CC}=6.0V$	0	-	-	ns
		Pn to CP; see Figure 10	$V_{CC}=2.0V$	0	-	-	ns
			$V_{CC}=4.5V$	0	-	-	ns
			$V_{CC}=6.0V$	0	-	-	ns
maximum frequency	f_{max}	see Figure 6	$V_{CC}=2.0V$	2.0	-	-	MHz
			$V_{CC}=4.5V$	10	-	-	MHz
			$V_{CC}=6.0V$	12	-	-	MHz

Note:

[1] t_{pd} is the same as t_{PHL} , t_{PLH} .

[2] t_t is the same as t_{THL} , t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i =input frequency in MHz;

f_o =output frequency in MHz;

C_L =output load capacitance in pF;

V_{CC} =supply voltage in V;

N =number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ =sum of outputs.

4、Testing Circuit

4.1、AC Testing Waveforms

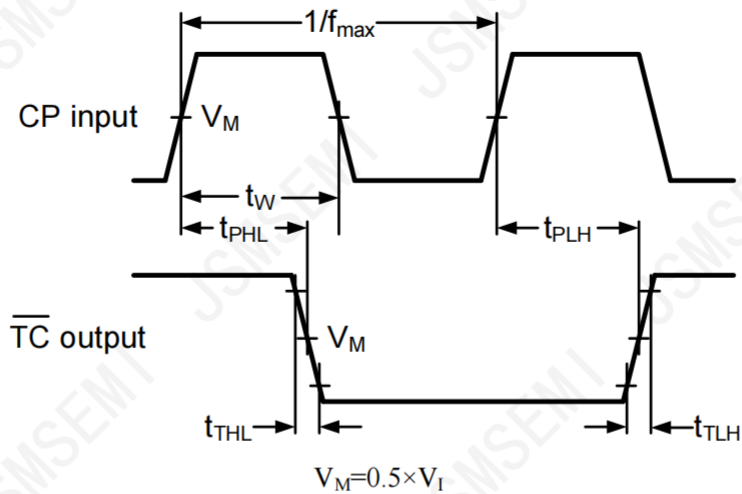


Figure 6. Waveforms showing the clock input (CP) to $\overline{T}C$ propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency

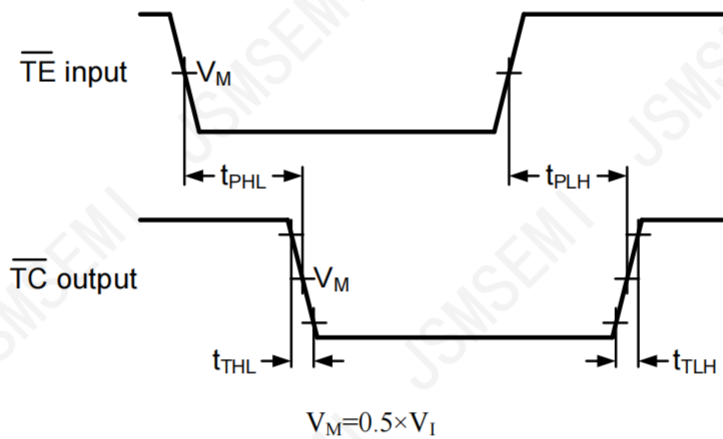


Figure 7. Waveforms showing the $\overline{T}E$ to $\overline{T}C$ propagation delays

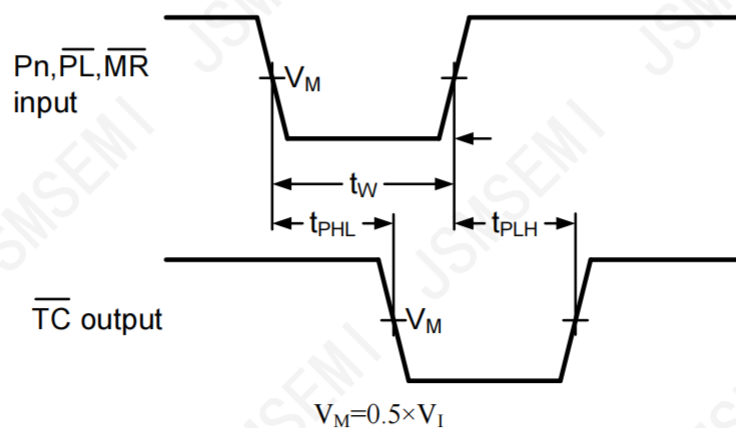


Figure 8. Waveforms showing $\overline{P}L, \overline{M}R, P_n$ to $\overline{T}C$ propagation delays

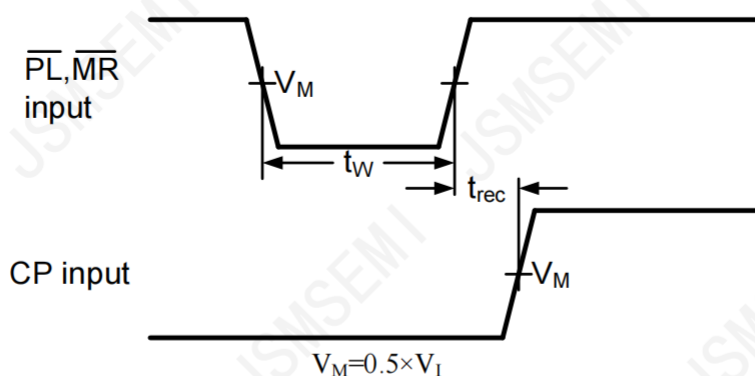
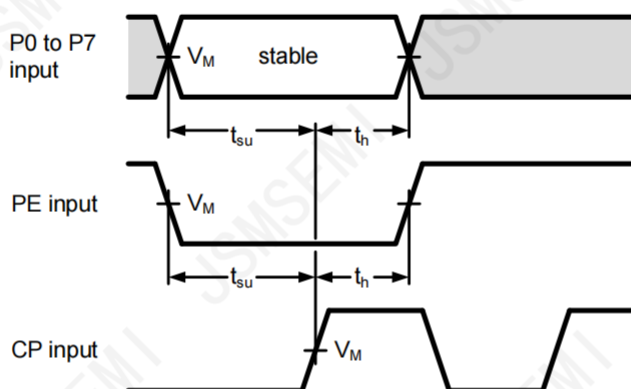


Figure 9. Waveforms showing removal time for $\overline{MR}$ and $\overline{PL}$



The shaded areas indicate when the input is permitted to change for predictable output performance.

$$V_M = 0.5 \times V_I$$

Figure 10. Waveforms showing hold and set-up times for $P_n, \overline{PE}$ to CP

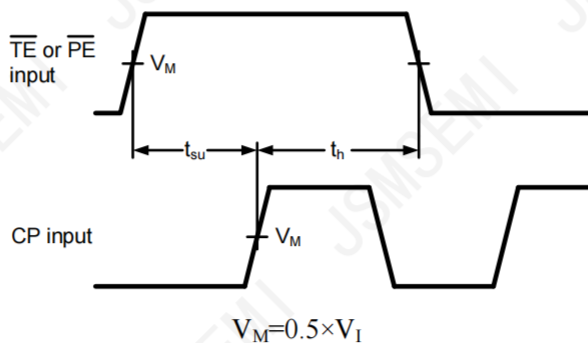
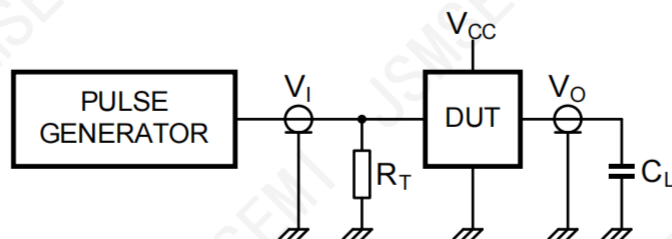


Figure 11. Waveforms showing hold and set-up times for $\overline{MR}$ or $\overline{PE}$ to CP

4.2、AC Testing Circuit



Definitions for test circuit:

R_T =Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L =Load capacitance including jig and probe capacitance.

Figure 12. Test circuit for measuring switching times

4.3、Test Data

Supply	Input		Load
V_{CC}	V_I	t_r, t_f	C_L
2.0V	V_{CC}	6ns	50pF
4.5V	V_{CC}	6ns	50pF
5.0V	V_{CC}	6ns	15pF
6.0V	V_{CC}	6ns	50pF

5、Typical Application Circuit And Application Note

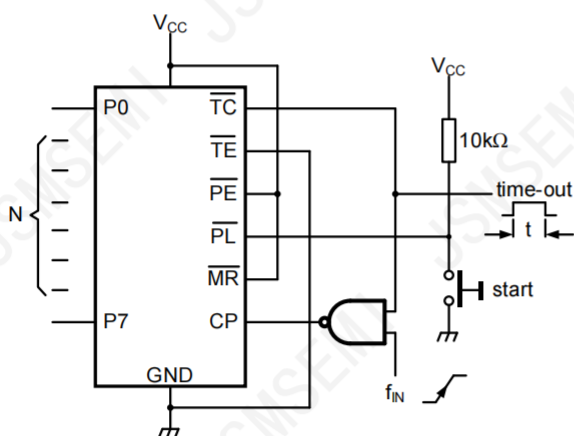


Figure 13. Programmable timer

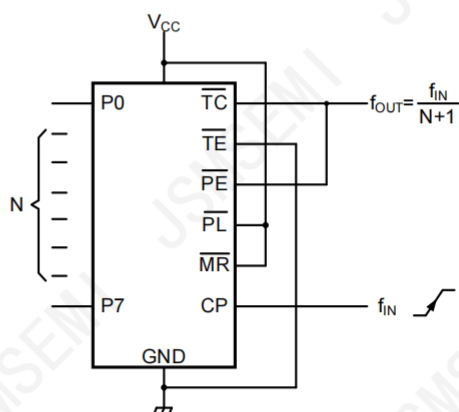
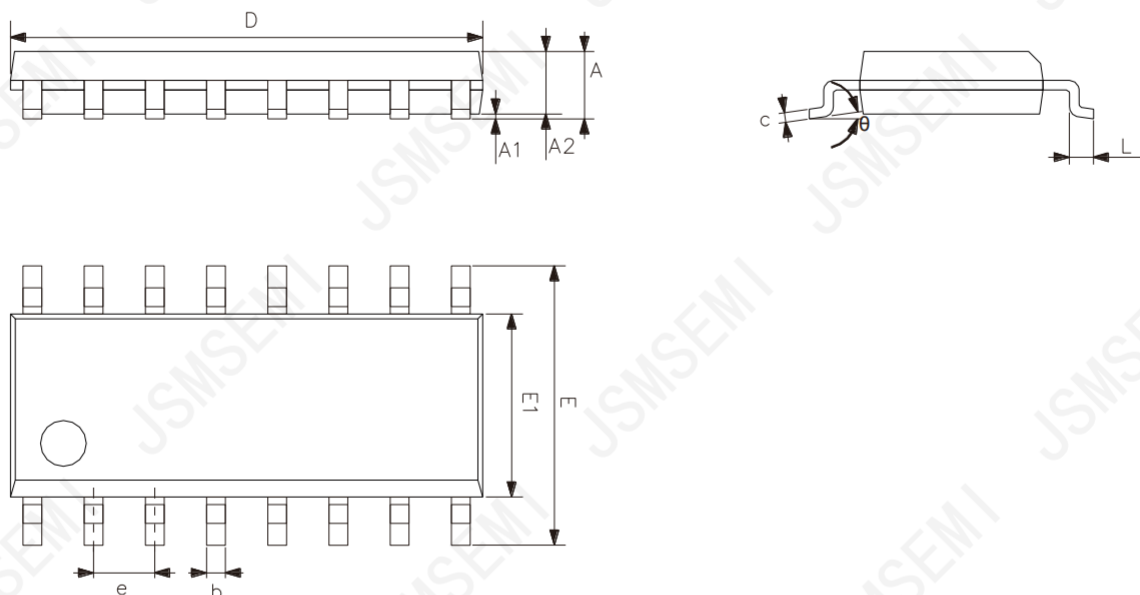


Figure 14. Divide-by-N counter

6、Package Information

6.1、SOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°

7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

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