NSG2065Q 250V Integrated BSD Three-Phase Half Bridge MOSFET/IGBT Gate Driver

1 Features and Benefits

- Floating channel designed for bootstrap operation
- Fully operational to +250 V
- 3.3V, 5V input logic compatible
- dV/dt noise Immunity ±50 V/nsec
- Allowable negative Vs capability: -9V
- Gate drive supply range from 5 V to 20V
- Non-inverting logic
- Undervoltage lockout for both channels
  --UVLO forward 4.5V
  --UVLO reverse 4.3V
- Propagation delay
  --Ton/Toff =150ns/150ns
- Cross-conduction prevention logic
  -- Deadtime:200ns
- Wide operating temperature range -40°C ~125°C
- Typically output Source/Sink current capability: 1.2A/1.5A
- RoSH compatible
- QFN24

2 Application

- Motor Control

3 Description

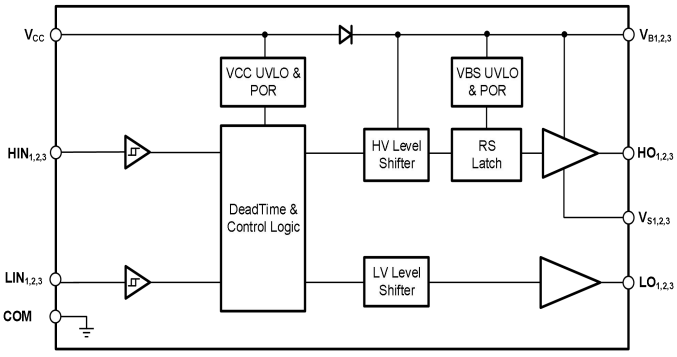
The NSG2065Q is a three-phase high-voltage power MOSFET and IGBT gate driver. Its floating channel drive design supports bus voltages of up to 250V. The NSG2065Q output provides significant drive capability, with output source/sink currents reaching 1.2A/1.5A.

The NSG2065Q features a wide operating voltage range, and both high-side and low-side gate drive voltages can be optimized for optimal driving efficiency. Internal shoot-through protection and dead-time circuitry prevent simultaneous conduction of both transistors, further reducing switching losses. The NSG2065Q's under voltage lockout (UVLO) function ensures that both driver outputs remain low when the supply voltage is insufficient. Furthermore, the NSG2065Q integrates a bootstrap diode, which helps to optimize the external circuitry around the chip.

Device information

Part Number	Package	Body size
NSG2065Q	QFN24	4mm*4mm

Functional Block Diagram



4 Selection Guide

Part Number	Input logic	BSD	Shout-though prevention	Dead time	VBS UVLO	Ton/Toff (ns)	IO+/IO- (A)
NSG2065Q	$HIN_{1,2,3}$, $LIN_{1,2,3}$	YES	YES	200ns	YES	150/150	1.2/1.5

5 Ordering Guide

Part Number	LOGO	Package	Package	SPQ
NSG2065Q	NSG2065Q XXXXXX	QFN24	Tape & Reel	4000

6 Revision history

Version	Content	Time
V1.0	Create	2023.08.31

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7 Function Pin Description

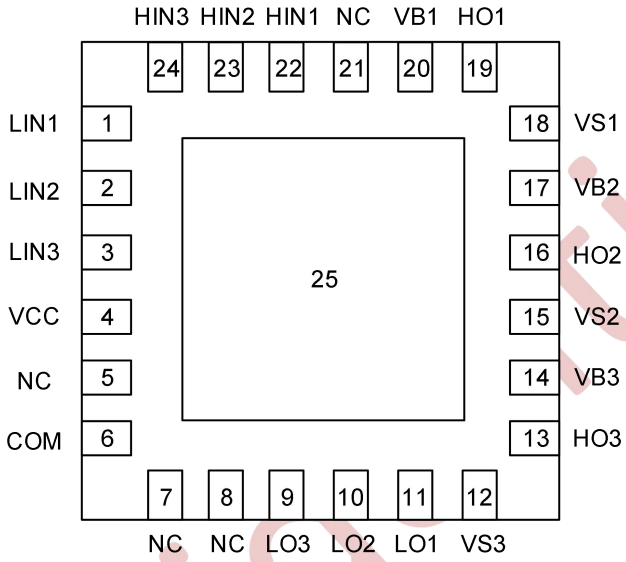


Figure7-1 24-Pin QFN Top view

Table7-1 Lead Definitions

Number	Symbol	Description
1	LIN1	Logic inputs for low side gate driver output , in phase
2	LIN2	Logic inputs for low side gate driver output , in phase
3	LIN3	Logic inputs for low side gate driver output , in phase
4	V_{CC}	Low side and logic fixed supply
6, 25	COM	High voltage floating supply return
9	LO3	Low side gate driver output
10	LO2	Low side gate driver output
11	LO1	Low side gate driver output
12	VS3	High voltage floating supply return
13	HO3	High side gate driver output
14	VB3	High side floating supply
15	VS2	High voltage floating supply return
16	HO2	High side gate driver output
17	VB2	High side floating supply
18	VS1	High voltage floating supply return
19	HO1	High side gate driver output
20	VB1	High side floating supply
22	HIN1	Logic inputs for high side gate driver output , in phase
23	HIN2	Logic inputs for high side gate driver output , in phase
24	HIN3	Logic inputs for high side gate driver output , in phase

8 Product specifications

8.1 Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to COM and an ambient temperature of 25°C.

Symbol	Definition	MIN.	MAX.	Units
$V_{B1,2,3}$	High side floating supply	-0.3	275	V
$V_{S1,2,3}$	High side floating supply return	V_B – 25	V_B + 0.3	
$V_{HO1,2,3}$	High side gate drive output	V_S -0.3	V_B + 0.3	
V_{CC}	Low side and main power supply	-0.3	25	
$V_{LO1,2,3}$	Low side gate drive output	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input of HIN & LIN	-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns

8.2 ESD rating

Symbol	Definition	TYP.	Units
ESD	HBM Model	1500	V
	Machine Model	500	V

8.3 Rated power

Symbol	Definition	MIN.	MAX.	Units
P_D	Package Power Dissipation @ TA ≤25°C	—	1.25	W

8.4 Thermal information

Symbol	Definition	MIN.	MAX.	Units
Rth_{JA}	Thermal Resistance, Junction to Ambient	--	100	°C/W
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

8.5 Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and COM are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to COM and the ambient temperature is 25°C.

Symbol	Definition	MIN.	MAX.	Units
$V_{B1,2,3,}$	High side floating supply	VS + 6	VS + 20	V
$V_{S1,2,3}$	High side floating supply return	-9	250	
$V_{HO1,2,3}$	High side gate drive output	V_S	V_B	
V_{CC}	Low side and main power supply	8	20	
$V_{LO1,2,3}$	Low side gate drive output	0	V_{CC}	
V_{IN}	Logic input of HIN & LIN	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note1：Transient negative VS can be used for COM-50V with a pulse width of 50ns, guaranteed by design..

Note2：When the input pulse width is less than 1us, the input pulse cannot be transmitted normally .

8.6 Electrical Characteristics

Valid for temperature range at T_A= 25ºC, V_{CC}=V_B= 15V, C_L=1nF, unless otherwise specified

8.6.1 Dynamical electrical characteristics

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
t_{ON}	Turn-on propagation delay	—	150	300	ns	V_S=0V
t_{OFF}	Turn-off propagation delay	—	150	300	ns	V_S=250V
t_R	Turn-on rise time	—	40	60	ns	
t_F	Turn-off fall time	—	15	30	ns	
DT	Deadtime	100	200	300	ns	
MT	Matching delay ON and OFF	—	—	50	ns	

8.6.2 Static electrical characteristics

Valid for temperature range at T_A= 25ºC, V_{CC}=V_B= 15V, C_L=1nF, unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
V_{CCUV+}	VCC supply UVLO threshold	-	4.5	4.9	V	
$V_{CCUVHYS}$	VCC supply undervoltage lockout hysteresis	-	0.2	-	V	
V_{BSUV+}	VBS supply UVLO threshold	-	4.5	4.9	V	
$V_{BSUVHYS}$	VBS supply undervoltage lockout hysteresis	-	0.2	-	V	
I_{LK}	High-side floating supply leakage current	-	-	10	μA	V_B=V_S=250V
I_{QBS}	Quiescent VB supply current	-	-	60	μA	V_{IN}=0V or 5V
I_{QCC}	Quiescent VCC supply current	-	-	700	μA	V_{IN}=0V or 5V
V_{IH}	Logic “1”(HIN & LIN) input voltage	2.5	-	-	V	
V_{IL}	Logic “0” (HIN &LIN) input voltage	-	-	0.8	V	
V_{OH}	High level output voltage, VBIAS - VO	-	-	0.2	V	I_O=0A
V_{OL}	Low level output voltage, VO	-	-	0.1	V	I_O=0A
I_{IN+}	Logic “1” Input bias current	-	25	50	μA	HIN=5V, LIN=0V
I_{IN-}	Logic “0” Input bias current	-	-	2	μA	HIN=0V, LIN=5V
I_{O+}	Output high short circuit pulsed current	-	1.2	-	A	V_O=0V PW≤10us
I_{O-}	Output low short circuit pulsed current	-	1.5	-	A	V_O=15V PW≤10us
R_{BSD}	Equivalent Resistance of BSD	-	-	300	Ω	

9 Function Description

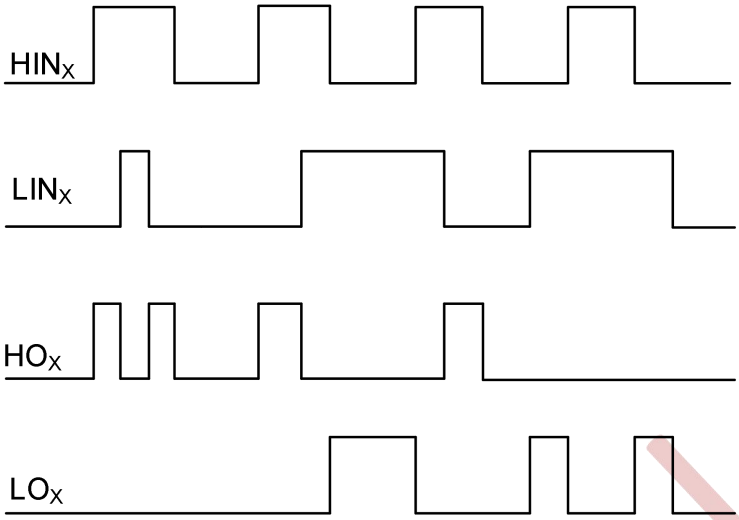


Figure 9-1 Input logic

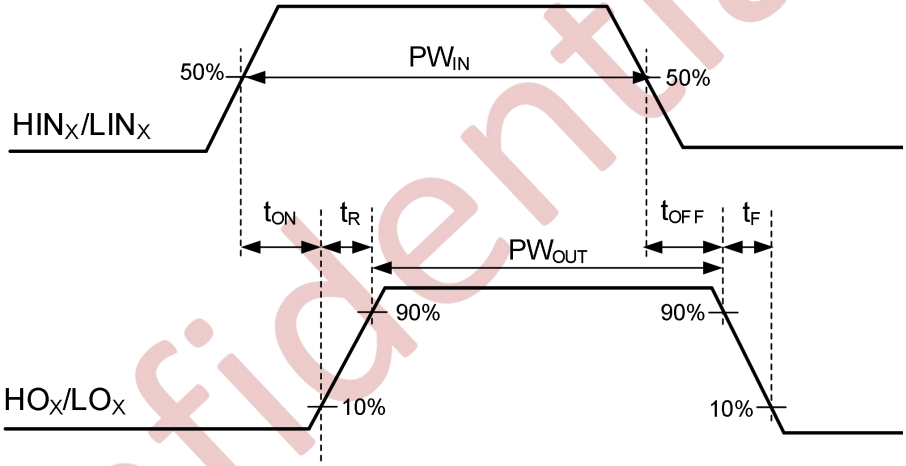


Figure 9-2 NSG2065Q Input and output timing waveform

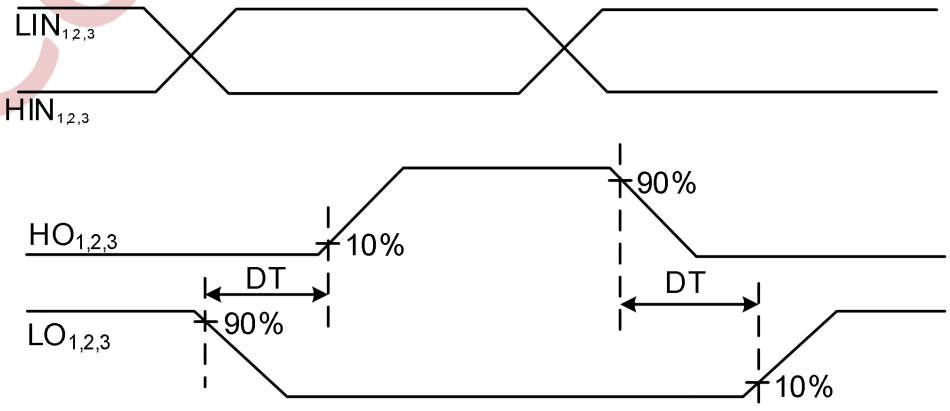


Figure 9-3 Propagation Time Waveform Definition

10 NSG2065Q Description

10.1 Function Block Diagram

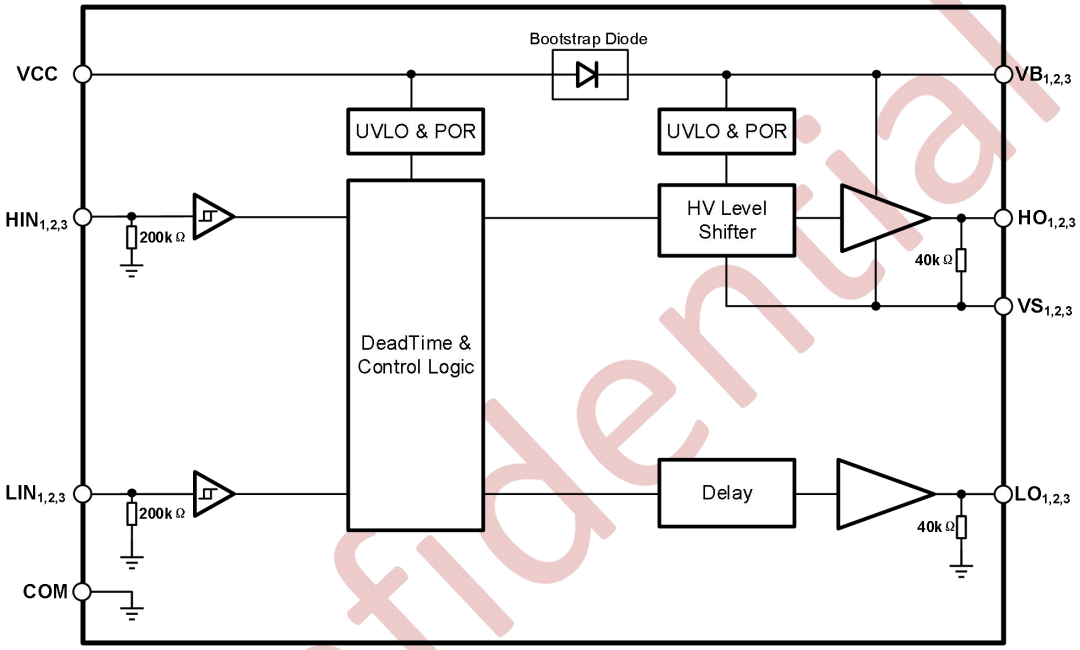


Figure10-1 Function Block Diagram of NSG2065Q

10.2 Typical application circuit

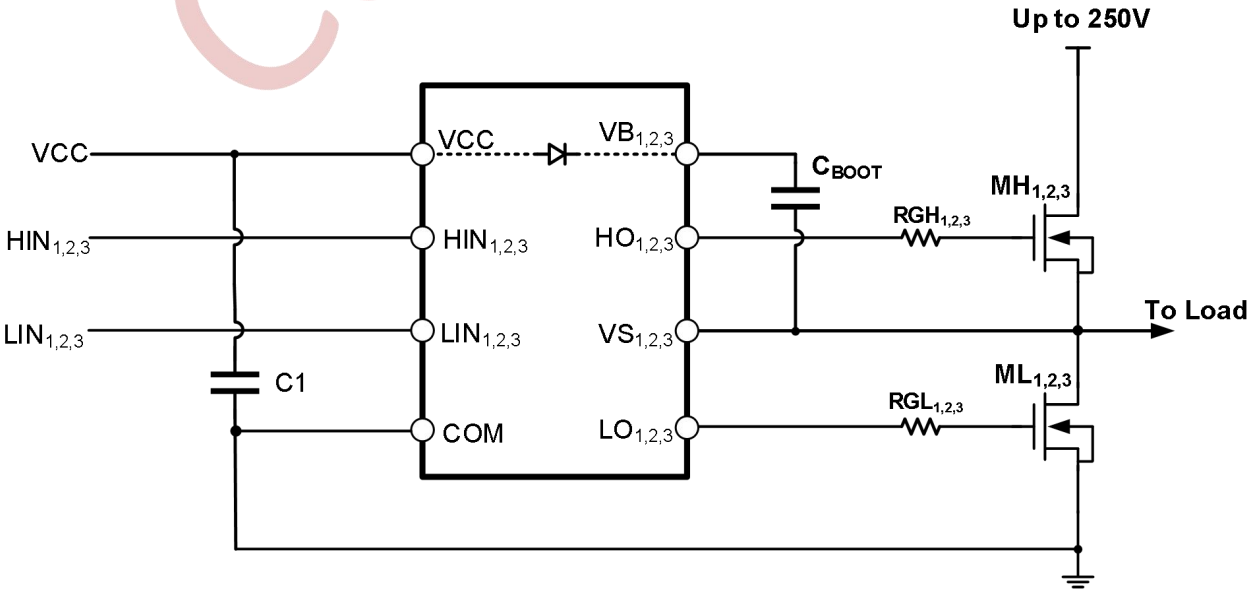


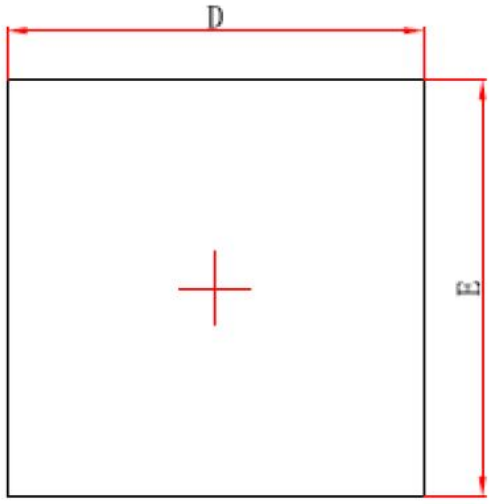
Figure10-2 Typical application circuit of NSG2065Q

11 Package Information

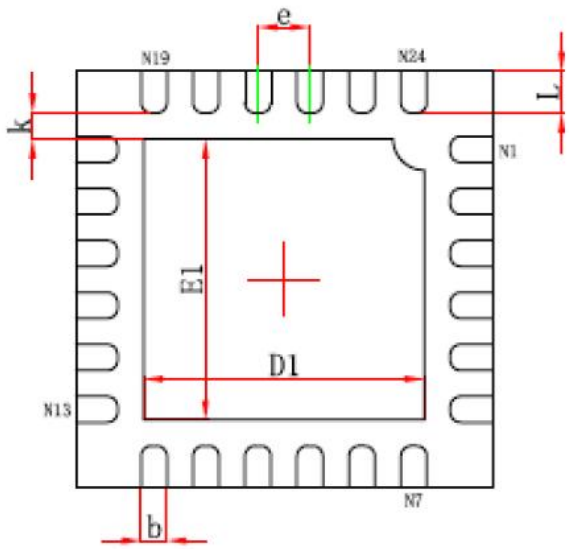
QFN24 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	0.700/0.800	-	0.800/0.900	E1	2.600	-	2.800
A1	0.000	-	0.050	K		0.200MN	
A3		0.203REF		B	0.200	-	0.300
D	3.924	-	4.076	e		0.500TYP	
E	3.924	-	4.076	L	0.324	-	0.476
D1	2.600	-	2.800				

QFN24 Package Outlines



Top View



Bottom View