



## General Description

The DMTH10H009SPSQ-13 use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics.

This device is specially designed to get better ruggedness and suitable.

## General Features

$V_{DS} = 100V$   $I_D = 75A$

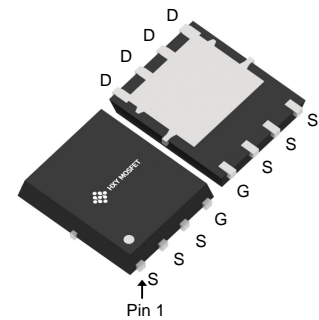
$R_{DS(ON)} < 9.2m\Omega @ V_{GS}=10V$

## Applications

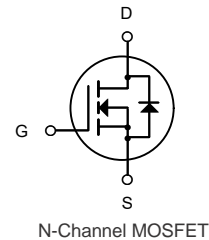
Consumer electronic power supply Motor control

Synchronous-rectification Isolated DC

Synchronous-rectification applications



DFN5X6-8L  
(TDSO8-8-EP(5x6))



## Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
DMTH10H009SPSQ-13	DFN5X6-8L (TDSO8-8-EP(5x6))	HXY MOSFET	5000

## Absolute Maximum Ratings at $T_j=25^\circ C$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V <sub>DS</sub>	100	V
Gate source voltage	V <sub>GS</sub>	±20	V
Continuous drain current <sup>1)</sup>	I <sub>D</sub>	75	A
Pulsed drain current <sup>2)</sup>	I <sub>D, pulse</sub>	300	A
Power dissipation <sup>3)</sup>	P <sub>D</sub>	97	W
Single pulsed avalanche energy <sup>5)</sup>	E <sub>AS</sub>	90	mJ
Operation and storage temperature	T <sub>stg</sub> , T <sub>j</sub>	-55 to 150	°C
Thermal resistance, junction-case	R <sub>θJC</sub>	1.3	°C/W



**Electrical Characteristics** ( $T_J=25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristics</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=100V, V_{GS}=0V,$	-	-	1.0	$\mu A$
$I_{GSS}$	Gate to Body Leakage Current	$V_{DS}=0V, V_{GS}= \pm 20V$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.6	2.5	V
$R_{DS(on)}$	Static Drain-Source on-Resistance <small>note3</small>	$V_{GS}=10V, I_D=20A$	-	7.3	9.2	m $\Omega$
		$V_{GS}=4.5V, I_D=8A$	-	9	13.5	m $\Omega$
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS}=50V, V_{GS}=0V,$ $f=1.0MHz$	-	2046	-	pF
$C_{oss}$	Output Capacitance		-	865	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	25	-	pF
$Q_g$	Total Gate Charge	$V_{DS}=50V, I_D=30A,$ $V_{GS}=10V$	-	39.4	-	nC
$Q_{gs}$	Gate-Source Charge		-	5.2	-	nC
$Q_{gd}$	Gate-Drain("Miller") Charge		-	9.8	-	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=50V, I_D=25A,$ $R_G=6\Omega, V_{GS}=10V$	-	20	-	ns
$t_r$	Turn-on Rise Time		-	5.2	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	49	-	ns
$t_f$	Turn-off Fall Time		-	12	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain to Source Diode Forward Current		-	-	75	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		-	-	300	A
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS}=0V, I_S=30A$	-	-	1	V
$t_{rr}$	Body Diode Reverse Recovery Time	$T_J=25^\circ\text{C},$ $I_F=12A, di/dt=100A/\mu s$	-	49	-	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge		-	85	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

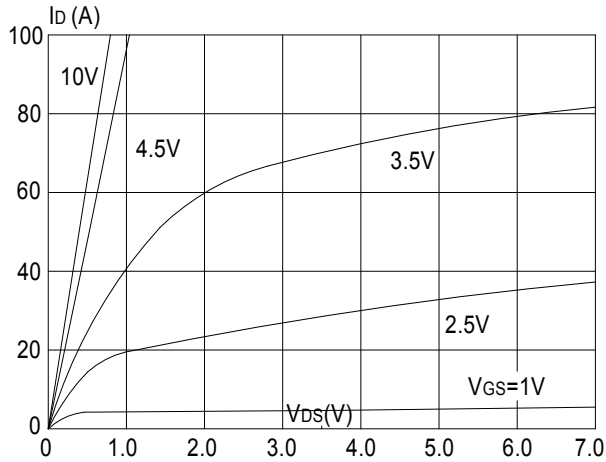
2. EAS condition:  $T_J=25^\circ\text{C}, V_{DD}=50V, V_G=10V, R_G=25\Omega, L=0.5mH, I_{AS}=19A$

3. Pulse Test: Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 0.5\%$

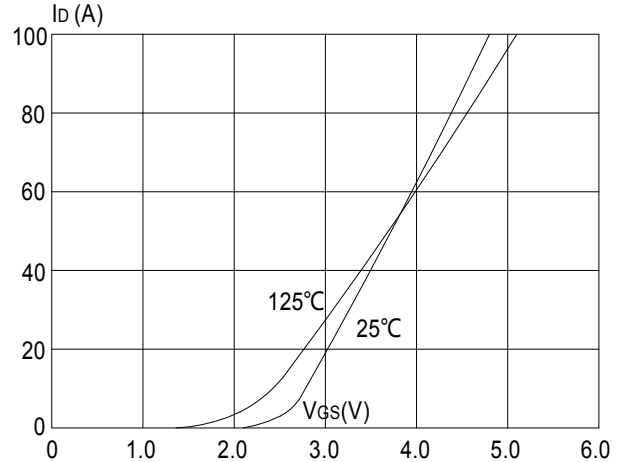


## Typical Performance Characteristics

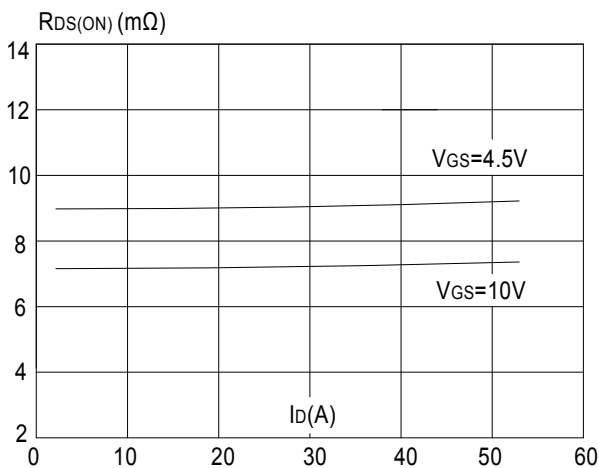
**Figure 1:** Output Characteristics



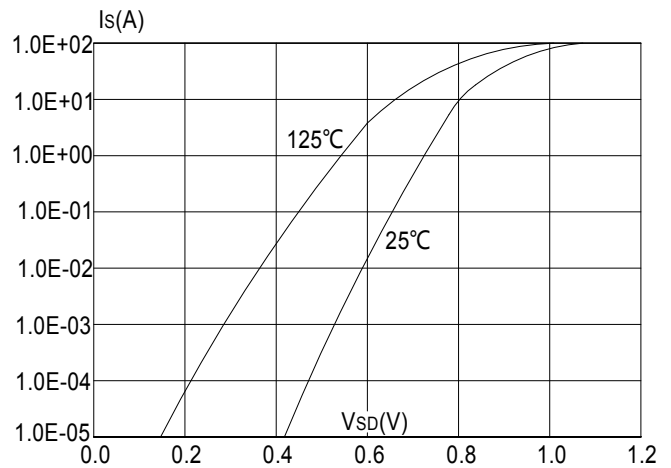
**Figure 2:** Typical Transfer Characteristics



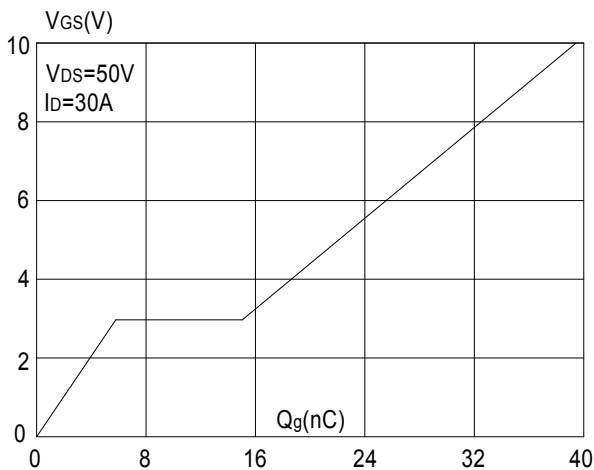
**Figure 3:** On-resistance vs. Drain Current



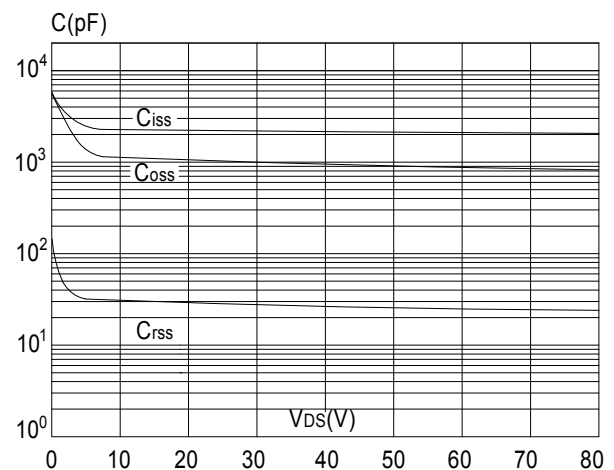
**Figure 4:** Body Diode Characteristics



**Figure 5:** Gate Charge Characteristics

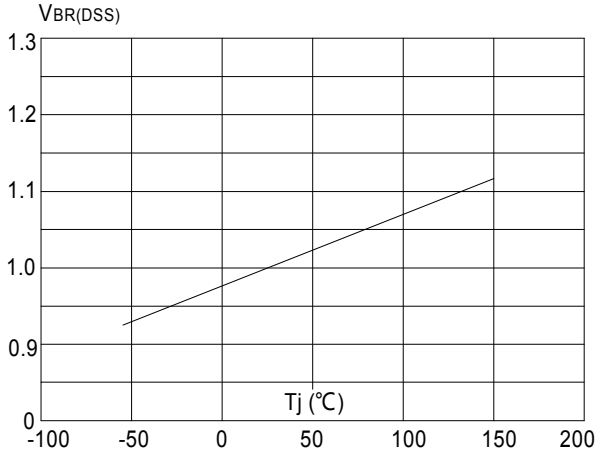


**Figure 6:** Capacitance Characteristics

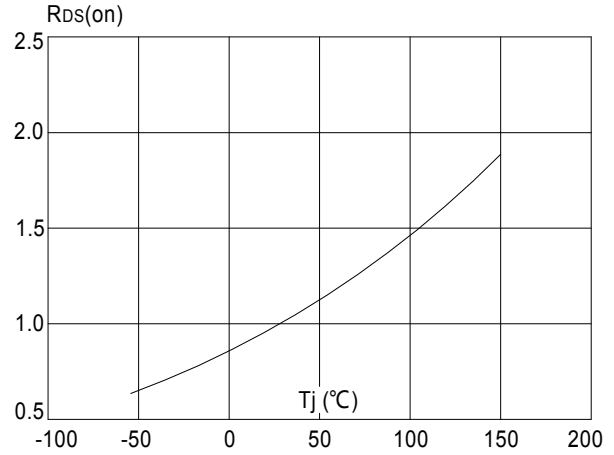




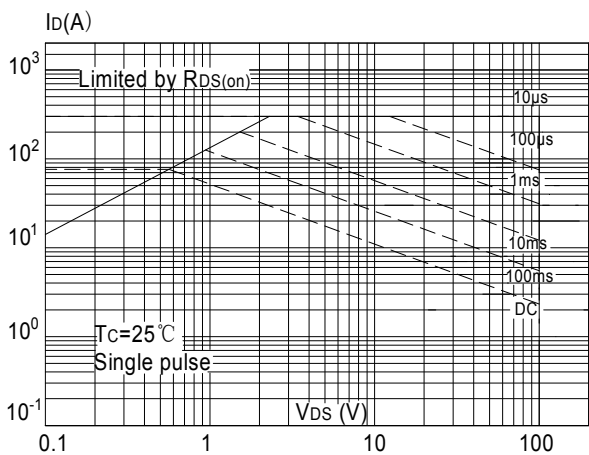
**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature



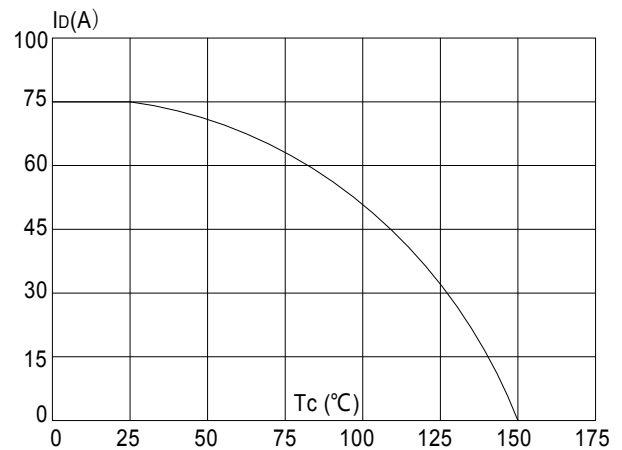
**Figure 8:** Normalized on Resistance vs. Junction Temperature



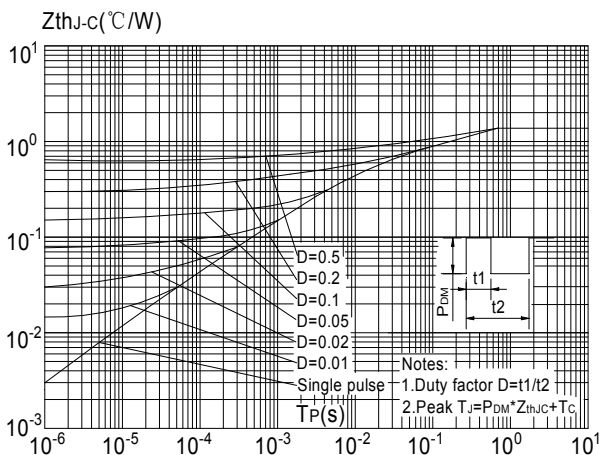
**Figure 9:** Maximum Safe Operating Area



**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature



**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case





## Test Circuit

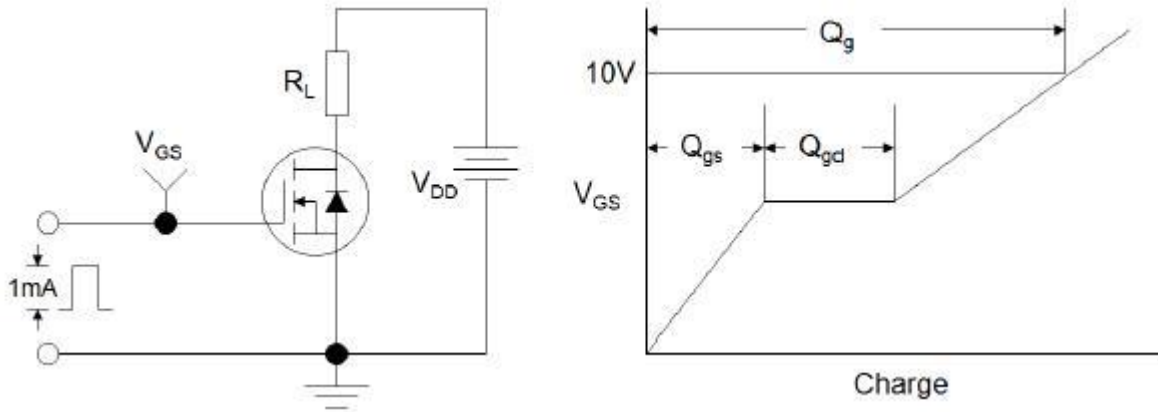


Figure1:Gate Charge Test Circuit & Waveform

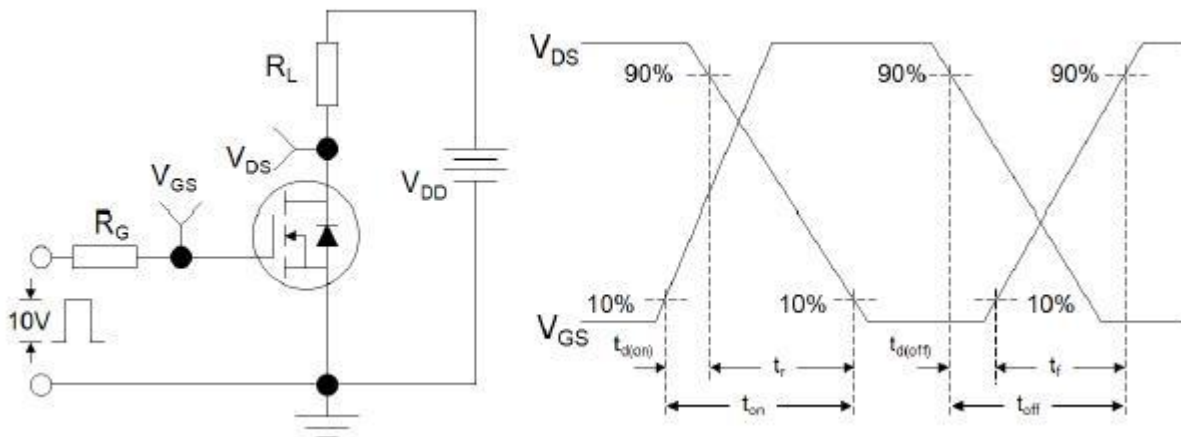


Figure 2: Resistive Switching Test Circuit & Waveforms

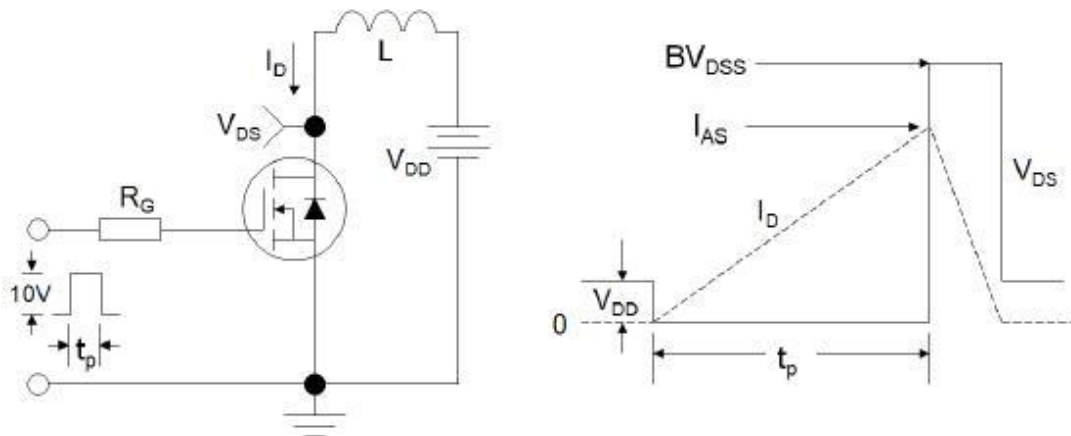
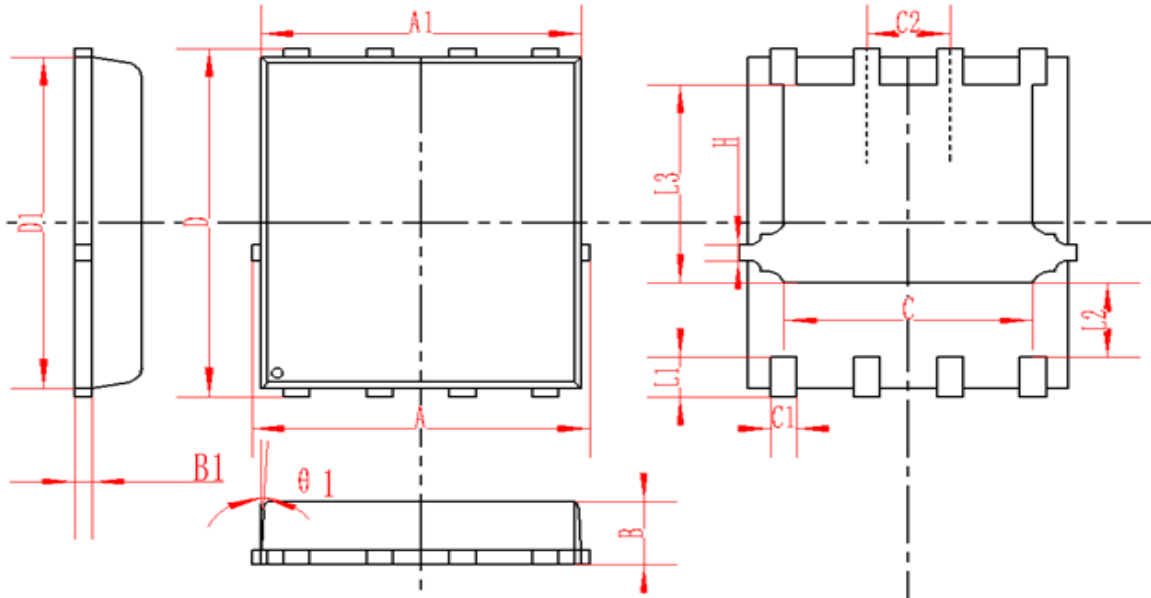


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



**DFN5X6-8L(TDSON-8-EP(5x6)) Package Information**



SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.95	5	5.05	0.195	0.197	0.199
A1	4.82	4.9	4.98	0.190	0.193	0.196
D	5.98	6	6.02	0.235	0.236	0.237
D1	5.67	5.75	5.83	0.223	0.226	0.230
B	0.9	0.95	1	0.035	0.037	0.039
B1	0.254REF			0.010REF		
C	3.95	4	4.05	0.156	0.157	0.159
C1	0.35	0.4	0.45	0.014	0.016	0.018
C2	1.27TYP			0.5TYP		
$\theta 1$	8°	10°	12°	8°	10°	12°
L1	0.63	0.64	0.65	0.025	0.025	0.026
L2	1.2	1.3	1.4	0.047	0.051	0.055
L3	3.415	3.42	3.425	0.134	0.135	0.135
H	0.24	0.25	0.26	0.009	0.010	0.010



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