

4-Port IEEE 802.3af/at PSE Controller for Power-over-Ethernet

Features

- IEEE 802.3af/at compliant
- Single DC power supply voltage input (44~57V)
- Supplies 4 independent power ports
- Supports DC Load-Removal Detections
- Supports 3-EVENT classification for IEEE802.3bt PD
- Up to 100W per Port for PSE Applications
- 0.25Ω Current-Sensing Resistor
- Automatic Mode and I2C Command Control Mode
- I2C Bus to access up to 16 x TME7624 devices
- Independent system parameters setting for every port
- Built-in temperature sensors and thermal protection
- Robust Short-Circuit Protection
- Built-in 3.3V regulators for external devices
- Built-in LEDs control for multi-port use, and support Serial or Direct LED
- Support overload LED
- Built-in EEPROM interface for dumb application
- Pin Selectable Detection Backoff Timer for ALT_A/B
- Pin Programmable Maximum Total current limit for Smart power management
- Space-Saving, 32-Pin QFN (5mm x 5mm) Power Package

Application

- Power-Sourcing Equipment (PSE)
- Switches/Routers
- PSE Midspan Power Injectors
- Surveillance NVR and DVRs

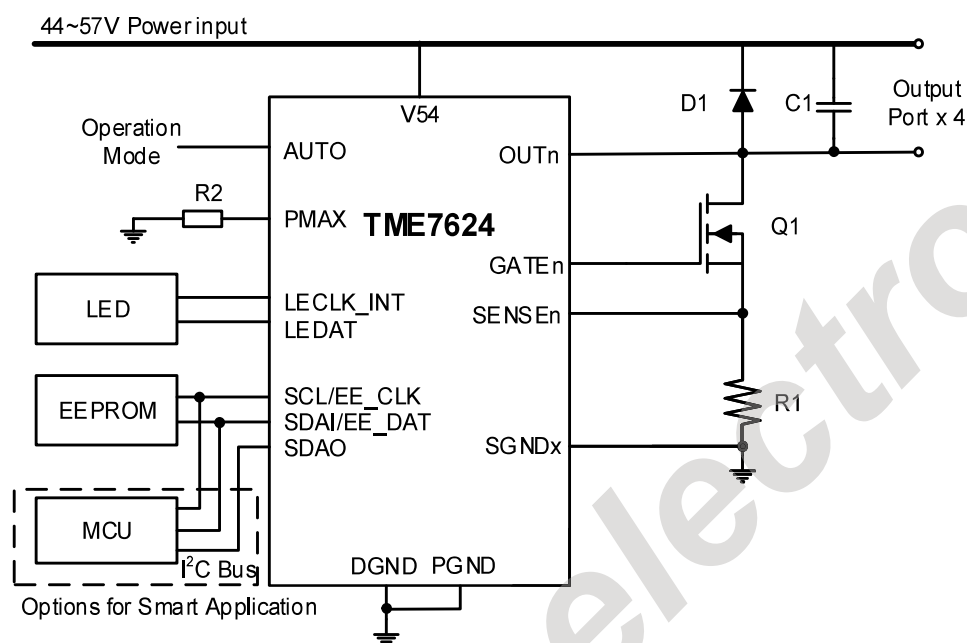
Description

TME7624 is an 4-port PSE (Power Sourcing Equipment) controller IC for PoE (Power over Ethernet) systems. It integrates power, analog and logic circuits into a single chip, and can be used for Midspans and Endpoint PSE applications. TME7624 meets all IEEE 802.3AF-2003 requirements, such as multi-point resistor detection, PD classification, DC Disconnect, and Back-off for Midspans. It also meets all IEEE 802.3AT-2009 requirements, such as 2-EVENT classification and supply maximum 36W per port. The device also supports Class4+ for detection and classification of high-power PDs. The device supports single-supply operation, provides up to 100W to each port (Class4+ or 3-EVENT enabled). TME7624 comprises internal temperature monitoring and thermal protection to protect against junction overheating.

TME7624 has a maximum power setting pin. Connect a resistor from this pin to DGND to set the total power capability on all 4 output ports. TME7624 will limit the total power on 4 ports below this power limit.

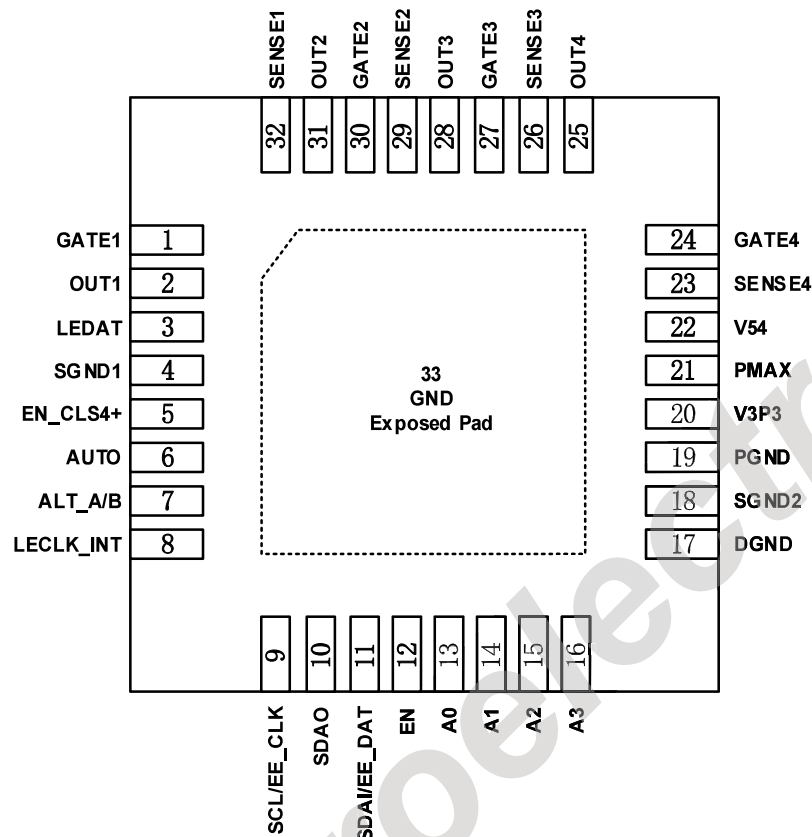
The 3.3V regulator is built-in to support external devices. Multiple TME7624s can integrate to build an 4 x N ports PSE system, and I2C bus uses to collect PD power status from each TME7624 to support global power managements. Management switch host has options to communicate TME7624 via I2C bus for PSE management activities. Optocouplers can be implemented to provide electrical isolations between the host and TME7624 for signal communication.

Typical Application



TME7624 Typical Application Diagram

Package



QFN5x5-32

Top Marking: T7624/XXXXX (T7624: Device Code, XXXXX: Inside Code)

Order Information

Part Number	Package	Top Marking	Quantity/ Reel
TME7624	QFN5x5-32	T7624 XXXXX	5000

TME7624 devices are Pb-free and RoHS compliant.

Pin Functions

Pin	Name	Function
1	GATE1	MOSFET gate driver for port1. Leave floating if not used.
2	OUT1	Output voltage sense pin for port1. Connect to return of output interface for detection, classification, voltage sense and current limit fold-back control. Leave floating if not used.
3	LEDAT	Serial LED data output. AUTO=1, this pin is serial LED data output, and support register configuration selection for direct LED output for port1. AUTO=0, this pin is no function, and support register configuration selection for direct LED output for port1 or serial LED_DAT output. Register configuration selects pin function. 0x98[3:2]=00 or 11, this pin is not used. 0x98[3:2]=01, this pin is serial LED_DAT output. 0x98[3:2]=10, this pin is direct LED output pin for port1.
4	SGND1	Current sense negative input for port 1 & port 2. Connect to low-side terminal of sense resistor. Kelvin connection in PCB layout for accuracy current sense. Connect to DGND if not used.
5	EN_CLS4+	Class4+ Enable Input. Referenced to DGND. EN_CL4+ is internally pulled down to DGND. Leave unconnected to disable the classification for Class4+ devices (IEEE 802.3at-compliant mode). Connect EN_CL4+ to V3P3 to enable the classification of Class4+ devices. EN_CL4+ is latched in after the device is powered up or after a reset condition.
6	AUTO	Auto/Shutdown Mode setting pin. Referenced to DGND. AUTO is internally pulled up to V3P3. Leave unconnected to put the device into auto mode by default. Connect AUTO to DGND instead to set the default mode to shut down. In either configuration, the software can change the operating mode of the device. AUTO is latched in after the device is powered up or after a reset condition.
7	ALT_A/B	ALT_A/B Type setting pin. This pin is latched upon power-on reset to define the ALT_A/B Type and is internally pulled up to V3P3. 0: ALT_A 1: ALT_B
8	LECLK_INT	Serial LED clock output. AUTO=1, this pin is serial LED clock output, and support register configuration selection for Interrupt request pin for all interrupt source event or direct LED output for port3. AUTO=0, this pin is Interrupt request pin for all interrupt source event, and support register configuration selection for serial LED clock output or direct LED output for port3. Register configuration selects pin function. 0x98[1:0]=00 or 11, this pin is Interrupt request pin for all interrupt source event 0x98[1:0]=01, this pin is serial LED_CLK output. 0x98[1:0]=10, this pin is direct LED output pin for port3.
9	SCL/EE_CLK	EEPROM clock & I2C clock pin. AUTO=0, this pin is I2C clock input. AUTO=1, this pin is clock out to EEPROM and I2C clock input.
10	SDAO	I2C serial data output pin. SDAO is an open-drain output. Connect SDAO to V3P3 using an external pull-up resistor (typically 4.7kΩ). Connect SDAO to SDA/EE_DAT for non-isolated applications. Connect SDAO to DGND if the I2C interface is not used.
11	SDA/EE_DAT	EEPROM data & I2C serial data input pin. AUTO=0, this pin is I2C serial data input. AUTO=1, this pin is data input from EEPROM and I2C serial data input.
12	EN	Enable input. This pin turns on/off all internal circuit and 4 ports except V3P3 regulator. Connect to V3P3 externally to turn on IC automatically.
13	A0	I2C device address bus AD0. The address signal is latched in after the device is powered up or after a reset condition. Internally pulled up to V3P3.
14	A1	I2C device address bus AD1. The address signal is latched in after the device is powered up or after a reset condition. Internally pulled up to V3P3.

Pin	Name	Function
15	A2	I2C device address bus AD2. The address signal is latched in after the device is powered up or after a reset condition. Internally pulled up to V3P3.
16	A3	I2C device address bus AD3. The address signal is latched in after the device is powered up or after a reset condition. Internally pulled up to V3P3.
17	DGND	Ground of internal digital and analog circuit.
18	SGND2	Current sense negative input for port 3 & port 4. Connect to low-side terminal of sense resistor. Kelvin connection in PCB layout for accuracy current sense. Connect to DGND if not used.
19	PGND	Ground of input power supply.
20	V3P3	3.3V internal regulator output for analog and digital circuit supply. A 1uF ceramic capacitor must be placed between V3P3 and DGND
21	PMAX	Maximum loading power setting pin. Connect a resistor from this pin to DGND to set the total power capability on all 4 output ports.The TME7624 will limit the total power on 4 ports below this power limit. The PMAX setting signal is latched when the device starts up or is reset. For the resistance value, see PMAX in Electrical Characteristics. $P_{MAX}=(R_{MAX}/1000+1)*40.17*V54(mW)$
22	V54	Main power supply input for chip. The 0.1uF&22uF capacitor should be added between V54 and PGND.
23	SENSE4	Current-sense pin from high-side terminal of sense resistor for port 4. 0.25Ω sense resistor is suggested for all applications with TME7624. Kelvin connection in PCB layout for accuracy current sense. Connect to DGND if not used.
24	GATE4	MOSFET gate driver for port 4. Leave floating if not used.
25	OUT4	Output voltage sense pin for port 4. Connect to return of output interface for detection, classification, voltage sense and current limit fold-back control. Leave floating if not used.
26	SENSE3	Current-sense pin from high-side terminal of sense resistor for port 3. 0.25Ω sense resistor is suggested for all applications with TME7624. Kelvin connection in PCB layout for accuracy current sense. Connect to DGND if not used.
27	GATE3	MOSFET gate driver for port3. Leave floating if not used.
28	OUT3	Output voltage sense pin for port 3. Connect to return of output interface for detection, classification, voltage sense and current limit fold-back control. Leave floating if not used.
29	SENSE2	Current-sense pin from high-side terminal of sense resistor for port 2. 0.25Ω sense resistor is suggested for all applications with TME7624. Kelvin connection in PCB layout for accuracy current sense. Connect to DGND if not used.
30	GATE2	MOSFET gate driver for port2. Leave floating if not used.
31	OUT2	Output voltage sense pin for port 2. Connect to return of output interface for detection, classification, voltage sense and current limit fold-back control. Leave floating if not used.
32	SENSE1	Current-sense pin from high-side terminal of sense resistor for port 1. 0.25Ω sense resistor is suggested for all applications with TME7624. Kelvin connection in PCB layout for accuracy current sense. Connect to DGND if not used.
33	EPAD	Exposed pad, it should be connected to PGND.

Absolute Maximum Ratings ⁽¹⁾

Items	Description	Min	Typ	Max	Unit
Supply Voltage	V54-SGND	-0.3		90	V
OUT1~4	OUTn- SGND @n=1~4	-0.3		90	V
GATE1~4	GATEn- SGND @n=1~4	-0.3		22	V
SENSE1~4	SENSEn- SGND @n=1~4	-0.3		22	V
All other Pins	All other Pin – (SGND, or DGND)	-0.3		6.5	V
DGND,SGND1, SGND2		-0.3		0.3	V
LECLK_INT, LEDAT, SDAO	Sink Current			20	mA
Continuous power dissipation (T _A = 25°C) (2)(3)			3.9		W
Junction Temperature				150	°C
Storage Temperature Range		-65		150	°C
Lead Temperature	30s, reflow			260	°C
T _A	Operating Ambient Temperature	-40		85	°C
Supply voltage (V _{IN})		44		57	V
Operating junction temp (T _J)		-40		125	°C

Thermal Resistance

Items	Description	Max	Unit
θ_{JA}	Junction-to-ambient thermal resistance EV3924-U-00A (3)	32	°C/W
θ_{JC}	Junction-to-case(top) thermal resistance EV3924-U-00A (3)	2	°C/W

ESD Rating ⁽⁴⁾

Items	Description	Value	Unit
V _{ESD_HBM}	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2017 Classification, Class: 2	±2000	V
V _{ESD_CDM}	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2018 Classification, Class: C3	±1000	V
I _{LATCH-UP}	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±200	mA

Notes:

(1) Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

(2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-toambient thermal resistance, θ_{JA} , and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD

(MAX) = (TJ (MAX) - TA) / θ JA. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

(3) Measured on EV3924-U-00A, 2-layer, 88mmx106mm PCB.

(4) Devices are ESD sensitive. Handling precaution is recommended.

Electrical Characteristics

V54 = 54V, PGND, DGND, SGND1 and SGND2 are connected together, R_{SENSE}=0.25Ω, T_J = -40°C to 125°C(5), typical value is tested at T_A = 25°C unless otherwise noted.

Symbol	Description	Conditions	Min	Typ	Max	Units
POWER SUPPLIES						
V54	Power Supply voltage	@IEEE802.3af	32		60	V
		@IEEE802.3at	50		60	V
I54	V54 operating current	All ports on @w/o peripheral load current & port load current		2	4	mA
V3P3	V3P3 voltage	IV3P3=0~10mA	3	3.30	3.6	V
VUVLO	V54 Undervoltage Lockout	V54-SGND, V54-SGND increasing	28	29.5	31	V
VUVLO_H	V54 Undervoltage Lockout Hysteresis	Ports shut down if: V54 - SGND < UVLO - UVLOH		3		V
V _{HI}	EN Logic High Voltage		2.5			V
V _{LI}	EN Logic Low Voltage				0.4	V
	EN Input Current	Pull EN to 0V, 3.3V		0		μA
V3P3	V3P3 Regulation	Load = 0mA		3.3		V
V3P3-UVLO	V3P3 Under Voltage Lockout	V3P3 rising	1.7	2.0	2.5	V
V3P3-UV-HYS	V3P3 Under Voltage Lockout Hysteresis			200		mV
	V3P3 Current Limit	V3P3 =DGND			10	mA
TPOR	Hardware Reset Pulse Width	Minimum low pulse duration on EN to lead to a hardware reset event	120			μs
DETECTION						
V _{DET1}	Detection Probe Voltage (First Phase)	V54 - OUTn during the first detection phase	3.6	4	4.4	V
V _{DET2}	Detection Probe Voltage (Second Phase)	V54 - OUTn during the second detection phase	7.2	8	8.8	V
V _{SLEW}	Detection Voltage Slew Rate	C _{DET} =0.1μF			0.02	V/μs
I _{DLIM}	Current-Limit Protection	Short V54 to OUTn, current measured through PortNn during detection	1.5	1.8	2	mA
V _{DCP}	Short-Circuit Threshold	If V54 - OUTn < VDCP after the first detection phase, a short circuit to SGND is detected	1	1.5	1.8	V
I _{D_OPEN}	Open-Circuit Threshold	First point measurement current threshold for open condition	10	15	25	μA
R _{GOODL}	Minimum Valid Detection Resistance		15	17	19	kΩ
R _{GOODH}	Maximum Valid Detection Resistance		26.5	30	33	kΩ
C _{GOOD-MAX}	Maximum Valid Capacitance		1		9	μF
t _{DET}	Detection Time	Maximum time allowed before detection is completed		320	350	ms
t _{RESET}	Detection Reset Time	Port reset by internal discharge between V54 and OUTn before detection starts		800		ms
t _{MIDLY}	Midspan Mode Detection Delay	Re-detection interval, ALT_A/B=1	2			s

Electrical Characteristics(continued)

V54 = 54V, PGND, DGND, SGND1 and SGND2 are connected together, R_{SENSE}=0.25Ω, T_J = -40°C to 125°C⁽⁵⁾, typical value is tested at T_A = 25°C unless otherwise noted.

Symbol	Description	Conditions	Min	Typ	Max	Units
t _{REMDLY}	Power Removal Detection Delay	Re-detection after one power removal event due to error condition (ICUT, ILIM, INRUSH), fault timer = 60ms ALT_A/B=0, auto and semi-auto mode.	1.6	2	2.4	s

CLASSIFICATION

V _{CL}	Classification Probe Voltage	V54 - OUTn during classification, Load < 60mA	16	18	20	V
I _{CL_LIM}	Current-Limit Protection	Short V54 to OUTn	60	70	80	mA
t _{CL_E}	Classification Event Timing		14	18	22	ms
V _{MARK}	Mark Event Voltage	Test V54 to OUTx pins	7.6		9.8	V
I _{MARK_LIM}	Mark Event Current Limit	Short V54 to OUTn	34	40	46	mA
t _{MARK_E}	Mark Event Timing		6.5	9	11	ms
I _{CL}	Classification Current Thresholds	Class 0 to 1	5	6.5	8	mA
		Class 1 to 2	13	14.5	16	
		Class 2 to 3	21	23	25	
		Class 3 to 4	31	33	35	
		Class 4 upper limit (or class4+)(7)	45	48	51	

GATE DRIVER

I _{SOURCE}	GATE Source Capability	Port Power on, V _{GATE} =GND	-30	-40	-50	μA
I _{SINK}	GATE Sink Capability	Port Power off, V _{GATE} =10V	30	40	50	μA
		V _{SENSE} =500mV, V _{GATE} =2V	30		100	mA
V _{GS-MAX}	GATE Clamp Voltage	Float GATE pin	8.5	10	11.5	V

OUT PIN

R _{OUT}	OUT Pin Resistance	Between V54 and OUTn, pull OUTn high in idle state (detection / classification off, port power off)		0.5		MΩ
I _{OUT}	OUT Pin Bias Current	OUTn=0V, port power-on		-95		μA
		OUTn=54V, port shutdown	-1		1	μA

Protection

V _{FLBK_ST}	Foldback Initial Voltage	VPortN - SGND above which the current-limit trip voltage starts folding back	IEEE802.3af		32	V
			IEEE802.3at		18	V
V _{FLBK_END}	Foldback Final Voltage	VPortN - SGND above which the current limit reaches V _{LIM_MIN}		46		V

Electrical Characteristics(continued)

V54 = 54V, PGND, DGND, SGND1 and SGND2 are connected together, $R_{SENSE}=0.25\Omega$,
TJ = -40°C to 125°C(5), typical value is tested at TA = 25°C unless otherwise noted.

Symbol	Description	Conditions	Min	Typ	Max	Units
V _{LIM_MIN}	Foldback minimum current limit	Short V54 to OUTn		35		mV
V _{PG}	Output power good (PG) rising threshold	OUTn pin voltage decrease	1.5	2	2.5	V
	RS_ Input Bias Current	VRS_ = SGND	-1		+1	μA
I _{Inrush}	Output current in POWER_UP State		400	425	450	mA
I _{LIM}	Short Circuit Current Limit Threshold	Class0~3	750	850	950	mA
		Class4	750	850	950	mA
		Class4+	1.9	2.2	2.5	A
I _{CUT}	Overcurrent Threshold after Startup	Class0	350	375	400	mA
		Class1	91	112	133	mA
		Class2	160	206	252	mA
		Class3	350	375	400	mA
		Class4	600	640	680	mA
		Class4+	1200	1280	1360	mA
t _{LIM}	Current Limit Timer	Class0~3, TLIM bit=00	50	60	70	ms
		Class4\4+, TLIM bit=00	10	12	15	ms
t _{CUT}	Over Current Timer	TCUT bit=00	50	60	70	ms
t _{INRUSH}	Start Inrush Current Limit Timer	INRUSH_ILIM_CFG=0x00	50	60	70	ms
V _{SCP}		ILIMn bit=0		212		mV
		ILIMn bit=1		425		mV
T _{SHD}	Thermal-Shutdown Threshold	Port is shut down and device resets if the junction temperature exceeds this limit, temperature increasing (6)		150		°C
T _{SHDN}	Thermal-Shutdown Hysteresis	Temperature decreasing (6)		20		°C
Total Load Power Limit						
P _{MAX}	Load Power Limit on All 4 Ports P _{MAX} calculation reference(8)	R _{MAX} = 26.7kΩ (25.5kΩ+1.2kΩ)		60		W
		R _{MAX} = 35.9kΩ (35.7kΩ+0.2kΩ)		80		W
		R _{MAX} = 45.1kΩ (43kΩ+2.1kΩ)		100		W
		R _{MAX} = 54.3kΩ (51kΩ+3.3kΩ)		120		W
P _{MAX-LIMIT}	Maximum Load Capability on all 4 Ports	Float P _{MAX} pin Class4+		200		W
T _{MAX-DLY}	Maximum Load Power Protection Delay	TPMAX bit=10 100% x P _{MAX} < Load < 150% x P _{MAX}		60		ms
		Load > 150% x P _{MAX}		2		ms

Electrical Characteristics(continued)

V54 = 54V, PGND, DGND, SGND1 and SGND2 are connected together, R_{SENSE}=0.25Ω, T_J = -40°C to 125°C(5), typical value is tested at T_A = 25°C unless otherwise noted.

Symbol	Description	Conditions		Min	Typ	Max	Units
DC Load Disconnection							
I _{MPSTH}	DC Load Disconnect Threshold	Minimum I _{port} allowed before disconnect (DC disconnect active), V _{PortN_} = 0V		5	7.5	10	mA
t _{DISC}	Load Disconnect Time	Time from IRS < I _{MPSTH} to gate shutdown		300	350	400	ms
ADC PERFORMANCE (Power-On Mode)							
	Resolution				9		Bits
	Offset Error	Voltage reading	TA = -40°C to +85°C			3	LSB
		Current reading	TA = -40°C to +85°C			3	
	Gain Error	Gain error voltage	TA = -40°C to +85°C	-1		1	%
		Gain error current	TA = -40°C to +85°C				
	V54 Voltage Accuracy	V54-SGND=48V	TA = -40°C to +85°C	-2.5		2.5	%
I _{NL}	Integral Nonlinearity					1	LSB
D _{NL}	Differential Nonlinearity					1	LSB
	Current Reading Range	Classes 0~4			1		A
		Class4+			2		
	Current LSB Step Size	Classes 0~4			1.956		mA
		Class4+			3.912		
	Voltage Reading Range	All classes			63.6		V
	Voltage LSB Step Size	All classes			124.5		mV
Logic Interface (SCL/EE_CLK, SDA/EE_DAT, SDAO, LECLK_INT, LEDAT, ALT_A/B, A0, A1, A2, A3, AUTO, EN_CLS4+)							
V _{LI}	Input Logic Low Voltage					0.4	V
V _{HI}	Input Logic High Voltage			2			V
	Logic Input Current	For SCL/EE_CLK, SDA/EE_DAT		-1		1	μA
V _{LO}	Open Drain Output Logic Low Voltage	Sink current = 3mA SDAO, LECLK_INT, LEDAT				0.4	V
	Open Drain Output Logic High Leakage	Open Drain to 3.3V				1	μA
R _{UP}	Internal Pull up/down Resistance	A0, A1, A2, A3, AUTO, ALT_A/B to V3P3. EN_CLS4+ to DGND			50		kΩ
TIMING CHARACTERISTICS							
f _{SCL}	Serial Clock Frequency			1		1000	kHz
t _{BUF}	Bus Free Time Between a STOP and START Condition			500			ns
t _{HD, STA}	Hold Time for a START Condition			200			ns

Electrical Characteristics(continued)

V54 = 54V, PGND, DGND, SGND1 and SGND2 are connected together, $R_{SENSE}=0.25\Omega$,
TJ = -40°C to 125°C⁽⁵⁾, typical value is tested at TA = 25°C unless otherwise noted.

Symbol	Description	Conditions	Min	Typ	Max	Units
t _{LOW}	Low Period of the SCL Clock		250			ns
t _{HIGH}	High Period of the SCL Clock		250			ns
t _{SU, STA}	Setup Time	START and STOP conditions	250			ns
t _{HD, DAT}	Data in Hold Time	Receive	0			ns
		Transmit	150		375	ns
t _{SU, DA}	Data in Setup Time		250			ns
t _F	Fall Time of SDAO Transmitting	(9)			250	ns
t _{SU, STO}	Setup Time for STOP Condition		0			ns
t _{SP}	Pulse Width of Spike Suppressed	(9)		100		ns

Notes:

(5) Guaranteed by over-temperature correlation.

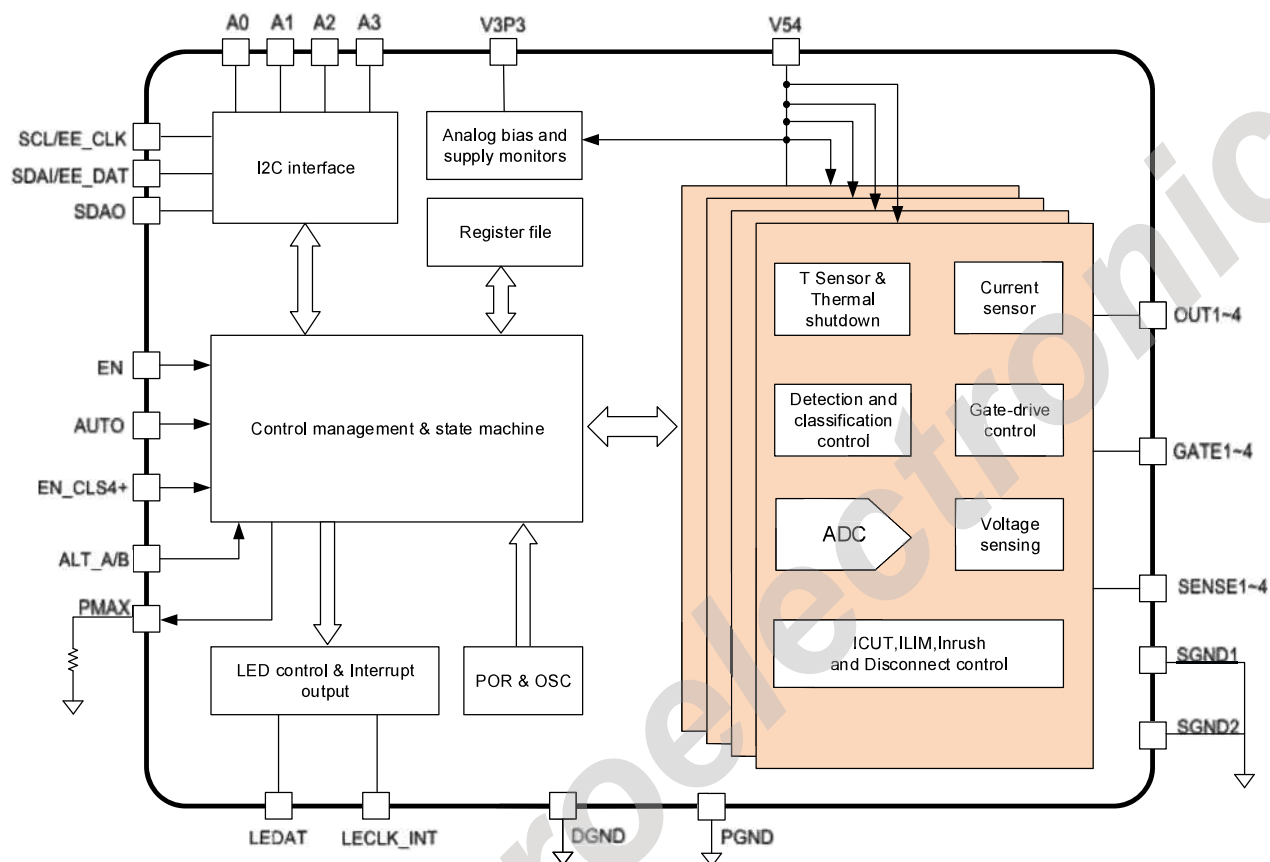
(6) Guaranteed by engineering sample characterization.

(7) If EN_CLS4+ is enabled, the TME7624 treats the classification current range from the upper of class 4 to the classification current limit as class4+.

(8) P_{MAX} calculation : $P_{MAX}=(R_{MAX}/1000+1)*40.17*V54(mW)$.

(9) Guaranteed by design. Not subject to production testing.

Block Diagram



TME7624 Block Diagram

Functions Description

Detailed Description

The TME7624 is an 4-ports PSE power controller designed for use in IEEE 802.3at/af-compliant PSE. This device provides PD discovery, classification, current limit, and load disconnect detections. The device supports both fully automatic operation and software programmability. The device also supports 2-EVENT classification, Class4+ for detection and classification of high-power PDs, and 3-EVENT classification for detection and classification of IEEE802.3bt PDs. The device supports single-supply operation, provides up to 100W to each port (EN_CLS4+ or 3-EVENT enabled), and still provides high-capacitance detection for legacy PDs. The device features an I2C compatible is fully software configurable and programmable. The device provides instantaneous readout of port current , voltage and temperature through the I2C interface. The device provides input under-voltage lockout (UVLO), over-temperature protection, and output voltage slew-rate limit during startup.

Reset

The device is reset by any of the following conditions:

- 1) Power-up/down. Reset condition is asserted once V54 falls below the UVLO threshold.
- 2) Hardware reset. To initiate a hardware reset, pull EN low to DGND for at least 100μs. Hardware reset clears once, EN returns high to V3P3, and all registers are set to their default states.
- 3) Software reset. To initiate a software reset, write a logical 1 to the RESET_IC register (R2Bh[3]) any time after power-up. Reset clears automatically.
- 4) Thermal shutdown. The device enters thermal shutdown at +150°C. The device exits thermal shutdown and is reset once the temperature drops below 130°C.

During normal operation, changes to the address inputs, ALT_A/B, EN_CLS4+, PMAX and AUTO are ignored, and they can be changed at any time prior to a reset state. At the end of a reset event, the device latches in the state of these inputs.

Port Reset

Set RESET_P_ (R2Ah[3:0]) high anytime during normal powered operation to turn off port, disable detection and classification, and clear the Port Event and Status registers. If a port is not powered, setting RESET_P_ high for that port has no effect. Individual port reset does not initiate a global device reset.

ALT_B Mode

In ALT_B mode, the device adopts cadence timing during the detection phase. When cadence timing is enabled and a failed detection occurs, the ports wait at least 2s before attempting to detect again. ALT_B mode is activated by setting ALT_A/B high and then powering or resetting the device. Alternatively, ALT_B mode can be software programmed individually for each port by setting ALT_B_ (R24h[3:0]) to a logical 1. By default, the ALT_A/B input is internally pulled up to V3P3 to disable this function.

Operation Modes

The device provides four operating modes to suit different system requirements. By default, auto mode allows the device to operate automatically at its default settings without any software. Semiautomatic mode automatically detects and classifies devices connected to the ports but does not power a port until instructed to by software. Manual mode allows total software control of the device and is useful for system diagnostics. Shutdown mode terminates all activities and securely turns off power to the ports. Switching between auto, semiautomatic, and manual mode does not interfere with the operation of an output port. When a port is set into shutdown mode, other ports are not affected. The four ports work independently of each other.

Auto (Automatic) Mode

By default, when the auto input is unconnected, the device enters auto mode after power-up or when the reset condition is cleared. To manually place a port into auto mode from any other mode, set the corresponding port mode bits (R1Fh[7:0]) to [11]. In auto mode, the device performs detection, classification, and powers up the port automatically if a valid PD is connected to the port. If a valid PD is not connected at the port, the device repeats the detection routine continuously until a valid PD is connected. When entering auto mode after a reset condition (state of AUTO input), the DET_ENn (R22h[3:0]) and CLASS_ENn (R23h[3:0]) bits are set to high and stay high, unless changed by software. When entering auto mode from any other mode due to a software command (programmed with R1Fh[7:0]), the DET_ENn and CLASS_ENn bits retain their previous state.

Semi(Semiautomatic) Mode

Enter semiautomatic mode by setting the port operating mode (R1Fh) to [10]. When entering semi mode, the DET_ENn and CLASS_ENn bits retain their previous states. When the DET_ENn and/or CLASS_ENn bits are set to 1, the TME7624 performs detection and/or classification repeatedly, but does not power up the port(s) automatically. Setting R28h[3:0] (PWR_ONn) high turns on power to the port(s) if detection and classification has successfully completed. If a port is powered down while in semiautomatic mode, the corresponding DET_ENn and CLASS_ENn bits are reset to 0.

Manual Mode

Enter manual mode by setting the port operating mode (R1Fh) to [01]. Manual mode allows the software to dictate any sequence of operation. In manual mode, the Detection register (R22h) and Classification register (R23h) are set to [00], and DET_ENn, CLASS_ENn become push-button bits. A port will only perform a single detection/classification cycle when DET_ENn, CLASS_ENn are set high, and they are reset low after execution.

PWR_ONn (R28h[3:0]) has the highest priority, and setting PWR_ONn high at any time causes the device to immediately enter the powered mode. Setting DET_ENn and CLASS_ENn high at the same time causes detection to be performed first. Once in the powered state, the device ignores DET_ENn and CLASS_ENn commands.

Shutdown Mode

To put a port into shutdown mode, set the corresponding port mode bits (R1Fh) to [00]. Putting a port into shutdown mode immediately turns off port power, clears the event and status bits, and halts all port operations. In shutdown mode the serial interface is still fully active; however, all DET_ENn, CLASS_ENn, and PWR_ONn commands are ignored.

PD Detection

During normal operation, the device probes the output for a valid PD. A valid PD has a 24.9kΩ discovery signature characteristic as specified in the IEEE 802.3at/af standard. Table 1 shows the IEEE 802.3at specification for a PSE detecting a valid PD signature. After each detection cycle, the device sets DETn (R06h[3:0] and R07h[3:0]) to 1 and reports the detection results in the detection status bits. The DETn bits are reset to 0 when read through the CoR (clear on read) register (R07h), or after a reset event.

During detection, the device keeps the external MOSFET off and forces two probe voltages through OUTn. The current through OUTn is measured, as well as the voltage difference from SGND to OUTn. A two-point slope measurement is used, as specified by the IEEE 802.3at/af standard, to verify the device connected to the port. The device implements appropriate settling times to reject 50Hz/60Hz power-line noise coupling.

Table 1. PSE PI Detection Modes Electrical Requirements (IEEE 802.3at)

PARAMETER	SYMBOL	MIN	MAX	UNIT	ADDITIONAL INFORMATION
Open-Circuit Voltage	VOC	—	30	V	In detection mode only
Short-Circuit Current	ISC	—	5	mA	In detection mode only
Valid Test Voltage	VVALID	2.8	10	V	—
Voltage Difference Between Test Points	ΔVTEST	1	—	V	—
Time Between Any Two Test Points	tBP	2	—	ms	This timing implies a 500Hz maximum probing frequency
Slew Rate	VSLEW	—	0.1	V/μs	—
Accept Signature Resistance	RGOOD	19	26.5	kΩ	—
Reject Signature Resistance	RBAD	< 15	> 33	kΩ	—
Open-Circuit Resistance	ROPEN	500		kΩ	—
Accept Signature Capacitance	CGOOD		150	nF	—
Reject Signature Capacitance	CBAD	10		μF	—
Signature Offset Voltage Tolerance	VOS	0	2.0	V	—
Signature Offset Current Tolerance	IOS	0	12	μA	—

High-Capacitance Detection

High-capacitance detection for legacy PDs is software programmable. To use the software to enable high-capacitance detection, set LEG_ENn (Port GPMD registers) to 1 during normal operation. If high-capacitance detection is enabled, PD signature capacitances up to 40μF (typ) are accepted.

Power Device Classification

During PD classification, the device forces a probe voltage between 16V and 20V at OUTn and measures the current into OUTn. The measured current determines the class of the PD.

After each classification cycle, the device sets CLSn (R08h[3:0] and R09h[3:0]) to 1 and reports the classification results in the classification status bits. The CLSn bits are reset to 0 when read through the CoR (clear on read) register (R09h) or after a reset event.

If EN_CL4+ is left unconnected, the device will classify the PD based on IEEE 802.3at standard. If the measured current exceeds 51mA, the device will not power the PD, but will report an over-current classification result and will return to IDLE state before attempting a new detection cycle.

Table 2. PSE Classification of a PD (Table 33-9 of the IEEE 802.3at Standard)

MEASURED ICLASS (mA)	CLASSIFICATION
0 to 5	Class 0
> 5 and < 8	May be Class 0 or 1
8 to 13	Class 1
> 13 and < 16	Either Class 1 or 2
16 to 21	Class 2
> 21 and < 25	Either Class 2 or 3
25 to 31	Class 3
> 31 and < 35	Either Class 3 or 4
35 to 45	Class 4
> 45 and < 51	Either Class 4 or Invalid

Class4+ PD Classification

The device supports high power beyond the IEEE802.3at standard by providing an additional classification (Class4+) if needed. To enable Class4+, connect EN_CL4+ to V3P3 and initiate a global reset or use the software to individually enable Class4+ classification for each port (R2Dh[3:0]). Once Class4+ is enabled, during classification, if the device detects currents in excess of the Class 4 upper-limit threshold, the PD will be classified as a Class4+ powered device. The PD is guaranteed to be classified as a Class4+ device for any classification current from 51mA up to the classification current-limit threshold. The Class4+ overcurrent threshold and current limit will be set automatically with ICUTn[5:0] and ILIMn. Leave EN_CL4+ unconnected to disable Class4+ detection and to be fully compliant to IEEE 802.3at standard classification.

2-EVENT PD Classification

If the result of the first classification event is Class 0 to 3, then only a single classification event occurs as shown in Figure 1. However, if the result is Class 4 (or Class4+), the device will perform a second classification event as shown in Figure 2. Between the classification cycles, the device performs a first and the second mark event as required by the IEEE 802.3at standard, forcing a 8V probing voltage at OUTn.

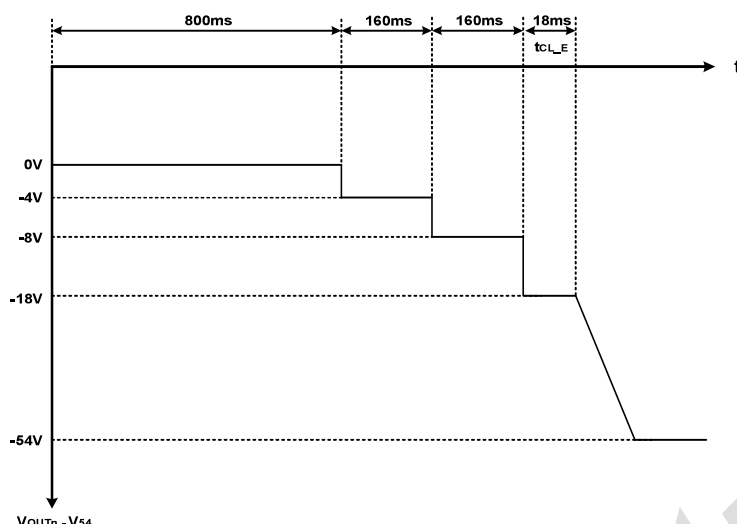


Figure 1. Detection, Classification, and Port Power-Up Sequence

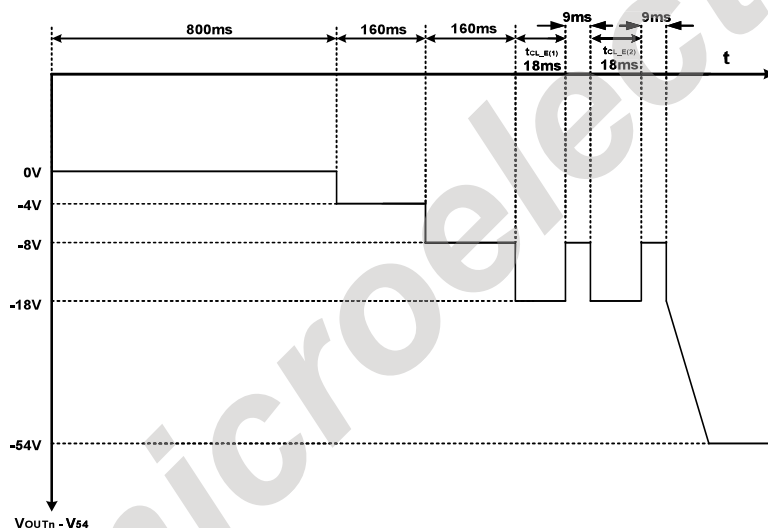


Figure 2. Detection, 2-EVENT Classification, and Port Power-Up Sequence

3-Event Classification

When the BT_CLASS_ENn bit is set to 1, the device can connect to the IEEE 802.3bt PD. If the classification of PD is 4~8, TME7624 will perform a third classification event after the second classification event, as shown in Figure 3. The TME7624 will provide this PD with a maximum current output equivalent to class4+ power.

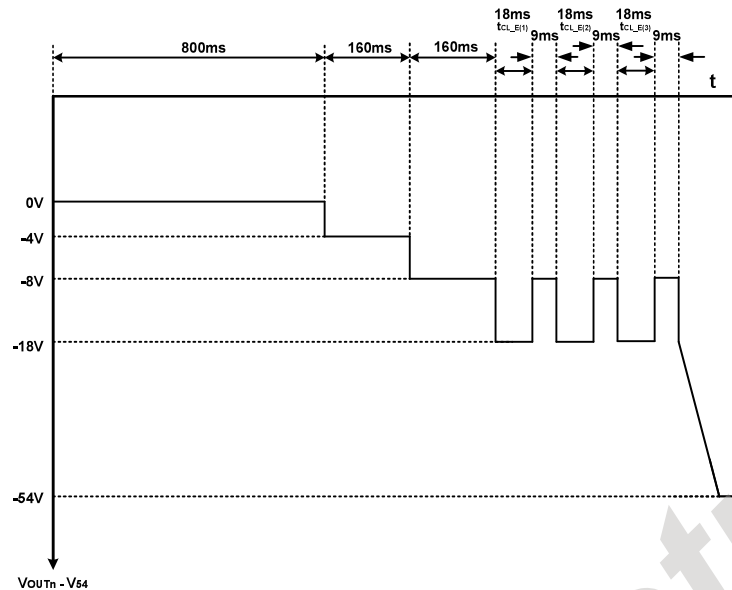


Figure 3. Detection, 3-EVENT Classification, and Port Power-Up Sequence

Powered State

When the device enters a powered state, the PGOODn (R1Dh[3:0]) is set to 1, and the device enters the normal power condition. PGOODn immediately resets to 0 whenever the power to the port is turned off. The power-good change bits, PG_CHGn (R02h[3:0]) are set both when the port powers up and when it powers down.

Over current Protection

During startup, if the current-limit condition persists, when the startup timer, TINRUSH, times out, the port shuts off, and the TINRUSHn bit is set (R0Eh[3:0] and R0Fh[3:0]).

In the normal powered state, the device checks for overcurrent conditions as determined by ICUT. The TCUT counter sets the maximum allowed continuous current period. When the counter reaches the TCUT limit, the device powers the port down and asserts the corresponding TCUTn bit (R0Ah[3:0] and R0Bh[3:0]). ICUT is programmable through the ICUTn registers. If a port is powered down due to a current-limit condition, during normal operation, the device asserts the corresponding ICVn bit (R10h[3:0] and R11h[3:0]) after power-off due to an current-limit fault. This feature sets an automatic duty-cycle protection to the external MOSFET to avoid overheating.

Foldback Current

During startup and normal operation, an internal circuit senses the voltage at OUTn and when necessary reduces the current-limit clamp current (ILIM) to help reduce the power dissipation through the external FET. When ILIMn = 00h (Class 0~3), foldback begins when VOUTn - SGND > 32V; and when ILIMn = 80h (Class4) or ILIMn = C0h (Class4+), foldback begins when VOUTn - SGND > 18V. The ILIM eventually reduces down to the minimum current-limit threshold V_{LIM_MIN} when VOUTn - SGND > 46V (Figure 4).

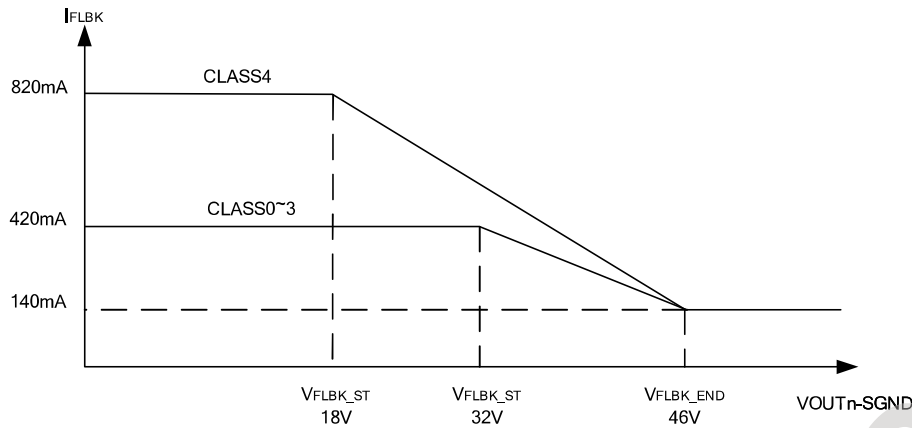


Figure 4. Foldback Current Characteristics

Interrupt

The device contains an open-drain logic output (LECLK_INT) that goes low when an interrupt condition exists. The Interrupt register (R00h) contains the interrupt flag bits and the Interrupt Mask register (R01h) determines which events can trigger an interrupt. When an event occurs, the appropriate Interrupt Event register bits (in R02h to R13h) and the corresponding interrupt (in R00h) are set to 1 and LECLK_INT is asserted low (unless masked). As a response to an interrupt, the controller can read the status of the event register(s) to determine the cause of the interrupt and take appropriate action. Each interrupt event register is paired with a Clear-on-Read (CoR) register. When an interrupt event register is read through the corresponding CoR register, the corresponding event register is reset to 0 (clearing interrupt event). LECLK_INT remains low and the interrupt is not reset when the Interrupt Event register is read through the read-only address. For example, to clear a supply event fault read R13h (CoR) not R12h (readonly). Use the INT_CLR bit (R2Bh[7]) to clear an interrupt, or the RESET_IC bit (R2Bh[4]) to initiate software resets.

V3P3 Power Supply

The device has an internally regulator generates 3.3V power for internal use and 3.3V power also can supply typical 10mA current on V3P3 pin for external devices. V3P3 has an under-voltage lockout (V3P3_UVLO) of 2V, and an under-voltage condition on V3P3 keeps the device in reset and the ports shut off. When V3P3 has recovered and the Reset condition clears, the V3P3_UVLO bit in the Supply Event registers is set to 1 (R12h[12] and R13h[13]). The digital address inputs, AUTO, and ALT_A/B are internally pulled up to V3P3, and all digital inputs are referenced to DGND. V3P3 can also be used to source up to 10mA for external circuitry. For internal regulator stability, connect a 33nF capacitor at the V3P3 output (Figure 5). If an external load is to be shared among multiple TME7624 devices, isolate the external supply bus with a series resistor (50Ω for 3 devices, 75Ω for 4 devices), and place a single 1μF capacitor on the bus.

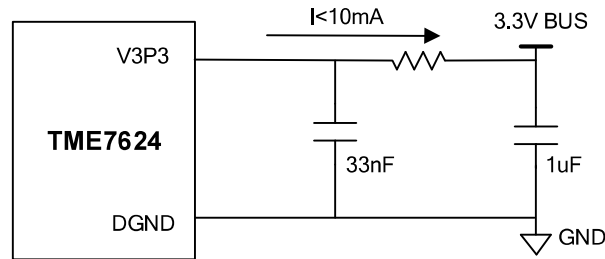


Figure 5 V3P3 External Power Sourcing

Undervoltage Protection

The device contains undervoltage protection features, and the flag bits can be found in the Supply Event register (R12h and R13h). An internal undervoltage lockout circuit keeps the MOSFET off and the device in reset until $V_{54} - SGND$ exceeds 29.5V for more than 3ms. An internal overvoltage circuit shuts down the ports. The digital supply also contains an undervoltage lockout that triggers when $V3P3 - DGND \leq 2V$.

DC Disconnect Monitoring

The DC disconnect monitoring settings are found in the Disconnect Enable register (R21h). To enable DC disconnect, set either the DCD_ENn bit for the corresponding port to 1. To disable the DC disconnect monitoring, DCD_ENn bit for that port must be set to 0. When enabled, if VRSENSEn (the voltage across RSENSEn) falls below the DC load disconnect threshold, VDCTH, for more than tDISC, the device turns off power and asserts the DISn bit for the corresponding port (R0Ch[3:0] and R0Dh[3:0]).

Hardware Power-Down

The EN digital input is referenced to DGND and is used for hardware level control of device power management. During normal operation, EN should be externally pulled directly up to V3P3, the 3.3V internal regulator output. To initiate a hardware reset and port power-down, pull EN to DGND for at least 100μs. While EN is held low, the device remains in reset and the ports remain securely powered down. Normal device operation resumes once EN is pulled up to the V3P3.

Total Load Power Limit

TME7624 has the classification capability to allocate power to each port based on IEEE802.3at, except this, TME7624 can monitor the total loading power and automatically shut down the lower priority port if total load power is higher than expected power rating. Set the 'PMAx_EN' bit high can enable this function, and TME7624 will compare total load power with the reference power set by PMAx pin. If the total loading is higher the programmed power level and TPMAx over load timer is out, TME7624 will shut down the lowest priority port among the powered ports. If the total loading power is higher than 150% of programmed limit, the lowest priority port will be shut down at once with about 2ms delay. By default, port 1 has the highest priority and port 4 has the lowest priority.

EEPROM controller

When the AUTO pin setup high, and the hardware or software is reset globally, the register file can be loaded with some initial value from external EEPROM (24xx series EEPROM, Maximum support to 24C16). TME7624 reads the EEPROM starting from address 0, parses the contents of the EEPROM command blocks, checks for integrity of the contents, and then writes the designated registers. This process continues until there is either no more data or the integrity check fails. When the TME7624 is finished reading the EEPROM, it automatically switches to the slave. EEPROM is necessary only if user wants to modify the default value of registers in auto mode.

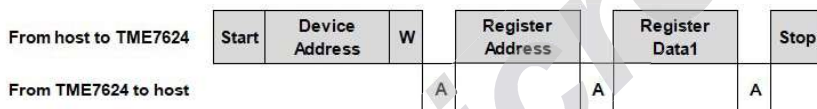
Thermal Shutdown

If the device's die temperature reaches 150°C (typ), an overtemperature fault is generated and the device shuts down. The die temperature must cool down below 130°C (typ) to remove the overtemperature fault condition. After a thermal shutdown condition clears, the device is reset and the TSD event bit is set to a logical 1 (R12h[7]/R13h[7]).

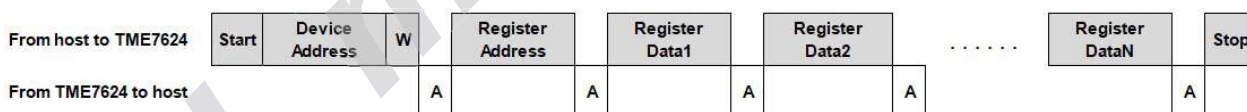
I2C Slave Interface

Through the I2C slave interface of TME7624, host CPU can access the register file in TME7624. It consists of SCL, SDAO and SDAI pins, where SCL is Clock, SDAO is Serial Data Output and SDAI is Serial Data Input. This I2C interface supports the 7-bit addressing mode of the I2C standard. The clock speed can be up to 1 Mbit/sec. There can be up to 16 TME7624 chips on one I2C bus, the LSB 4 bits of the I2C address can be assigned with the address pin A3~A0. The MSB 3 bits of the I2C address are fixed at 010. The following diagram (see Figure 6) is the register read/write cycles of the I2C bus.

I2C Register Write 1 Byte Cycle:



I2C Register Write n Bytes Cycle:



I2C Register Read 1 Byte Cycle:



I2C Register Read n Bytes Cycle:



Start Bit = 1→0, Stop Bit = 0→1

W = write Bit = 0, R = Read Bit = 1

A = ACK Bit = 0, NA = NO ACK Bit = 1

Figure 6 I2C bus read/write cycles diagram

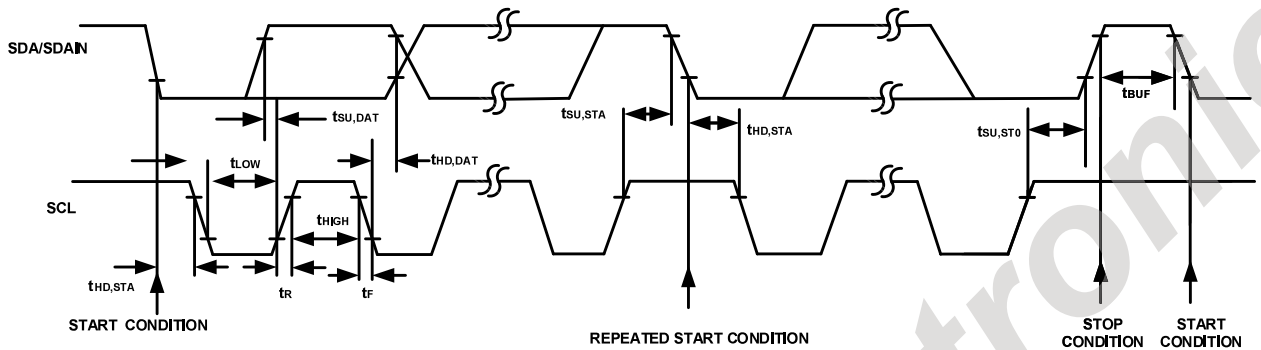


Figure 7 Serial Interface Timing Details

Table 3. Programmable Device Address Settings

DEVICE ADDRESS						
B7	B6	B5	B4	B3	B2	B1
0	1	0	A3	A2	A1	A0

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master finishes communicating with the slave, the master issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The STOP condition frees the bus for another transmission (see Figure 8).

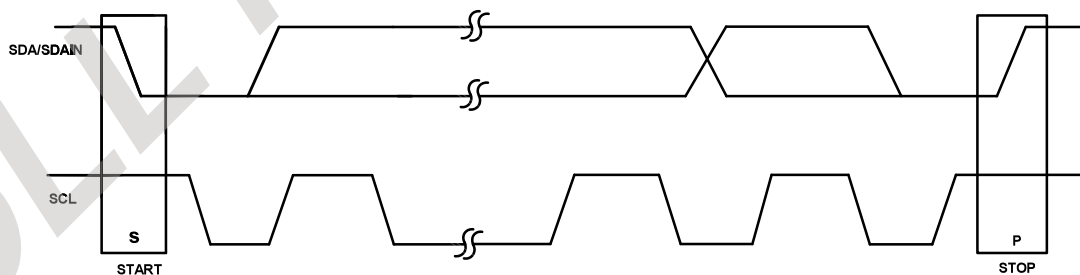


Figure 8 START and STOP Conditions

Bit Transfer

Each clock pulse transfers one data bit (Figure 9). The data on SDA must remain stable while SCL is high.

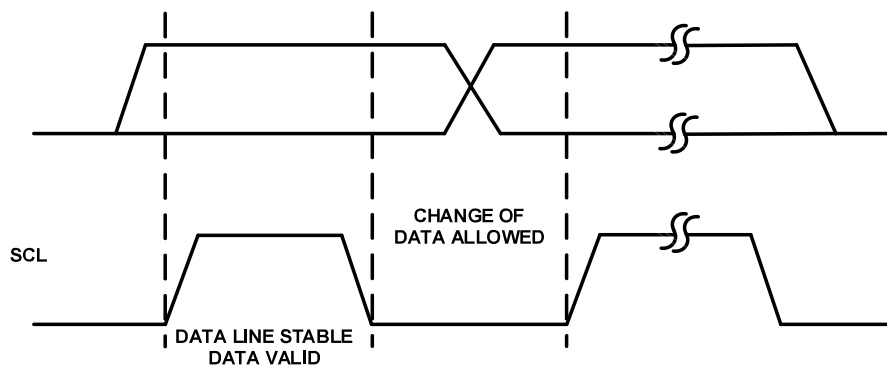


Figure 9 Bit Transfer

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 10) that the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, so the SDA line is stable low during the high period of the clock pulse. When the master transmits to the TME7624, the device generates the acknowledge bit. When the device transmits to the master, the master generates the acknowledge bit.

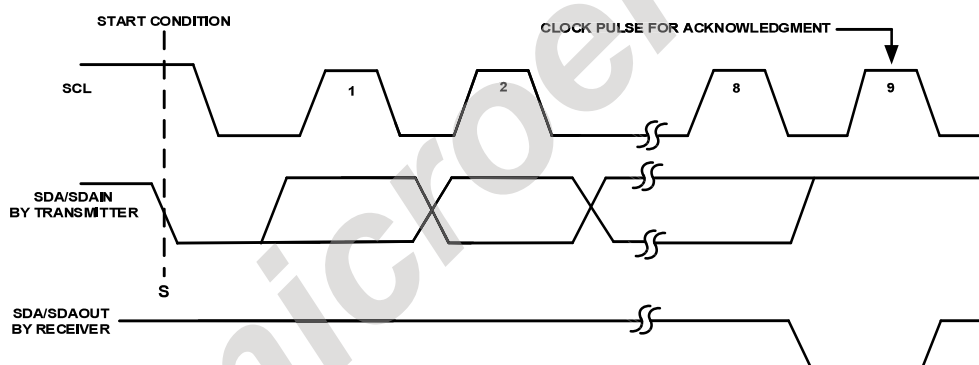


Figure 10 Acknowledge

LED Interface

When the AUTO pin setup high, the LEDAT pin is serial LED data output, and the LECLK_INT pin is serial LED clock output, and support register configuration. The LED interface can hook up with an IP403 (Serial-to-Parallel LED driver) to display the port status. A port status LED is lit up when TME7624 allocates power to the port. LED interface is enabled by pulling up LEDAT pin with a resister. One TME7624 can handle 4 LEDs and up to five TME7624s can share one IP403, where one TME7624 serves as the master to drive LECLK and the others are slaves. A2 pin defines TME7624 to be a master or a slave. The index counter in all TME7624s counts from 0 to 55 repeatedly with LECLK after reset and the value of index counter in all TME7624 are identical. An TME7624 will send out 4-bit LED information on LEDAT when its index counter reaches start index defined in start index register (0x8C). The detail is illustrated in the LED start index register (0x8C) and Figure 11. If there is only one or two TME7624s, user can replace IP403 with a 74LS164 to display port status for cost saving. One TME7624 must be configured as a master.

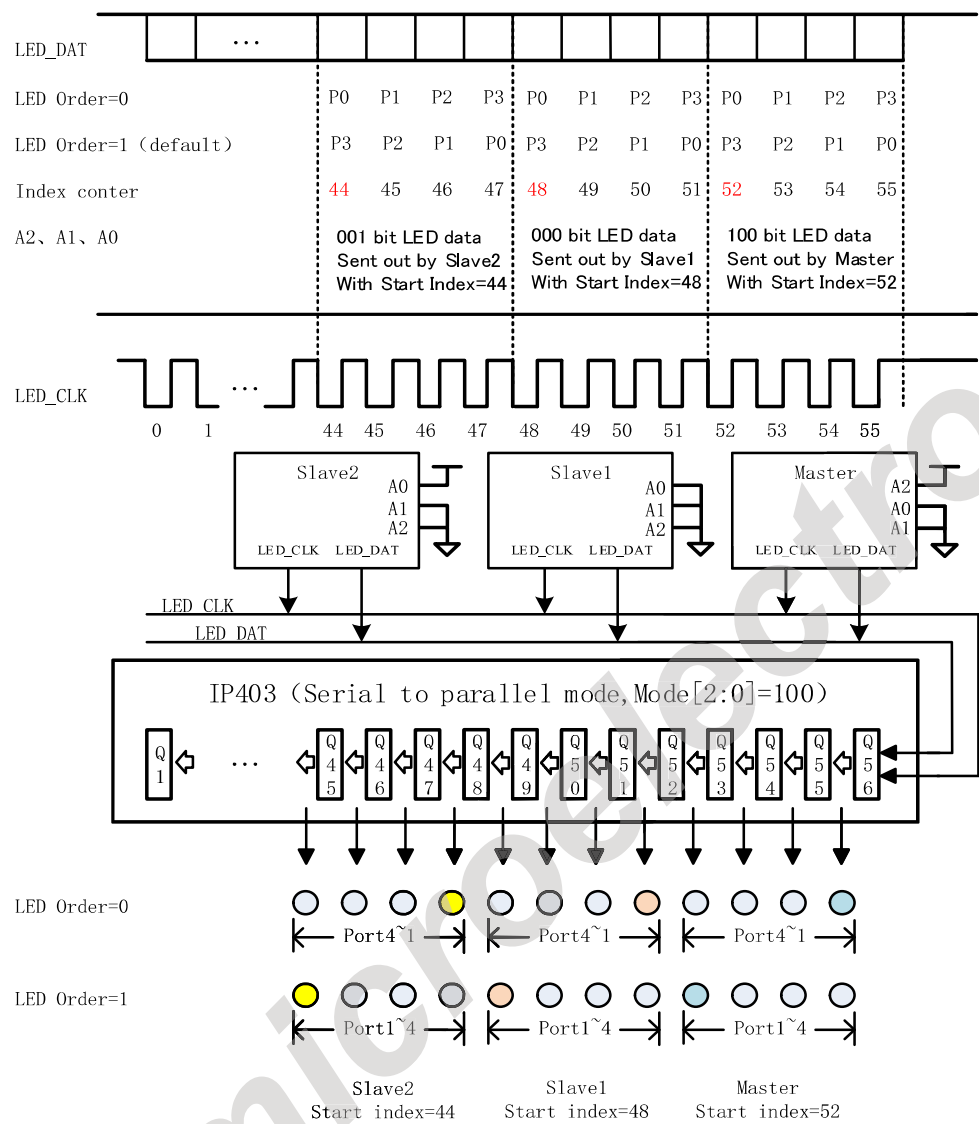


Figure 11 LED behavior and system diagram of multiple TME7624 application

Power On Sequence and Reset Timing

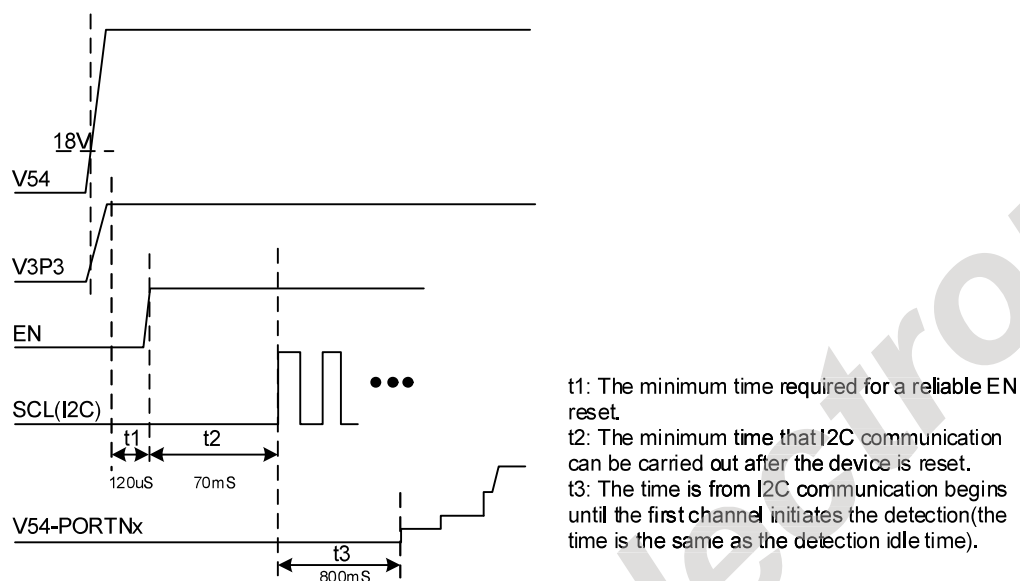
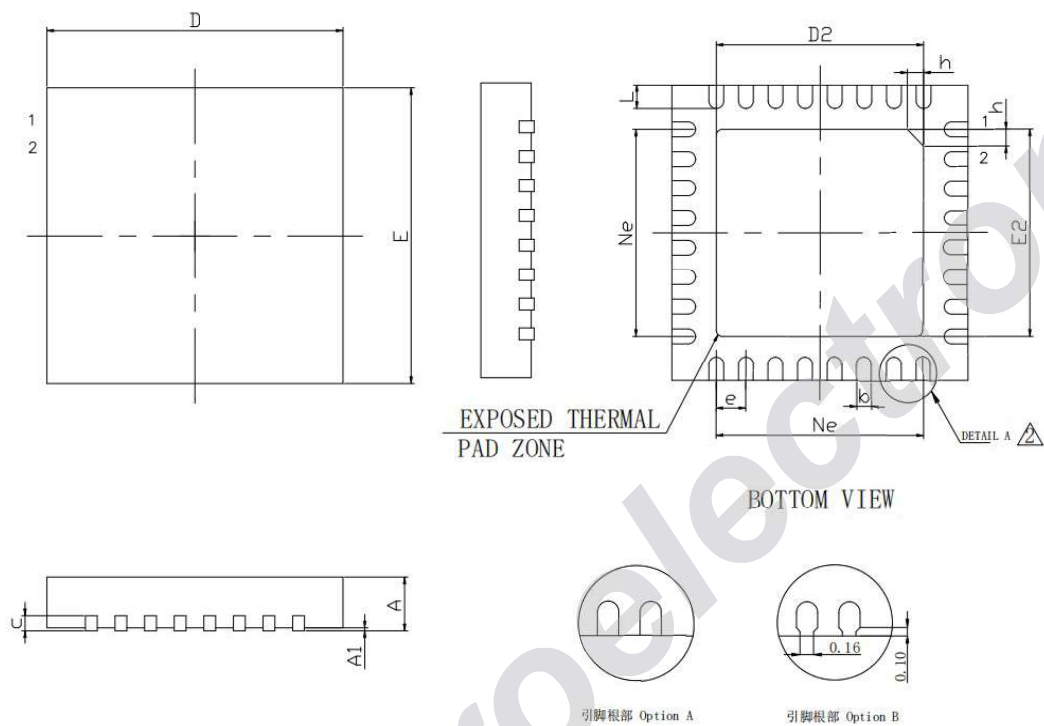


Figure 12 Power on Sequence and Reset Timing Diagram

Package Information

QFN5x5-32

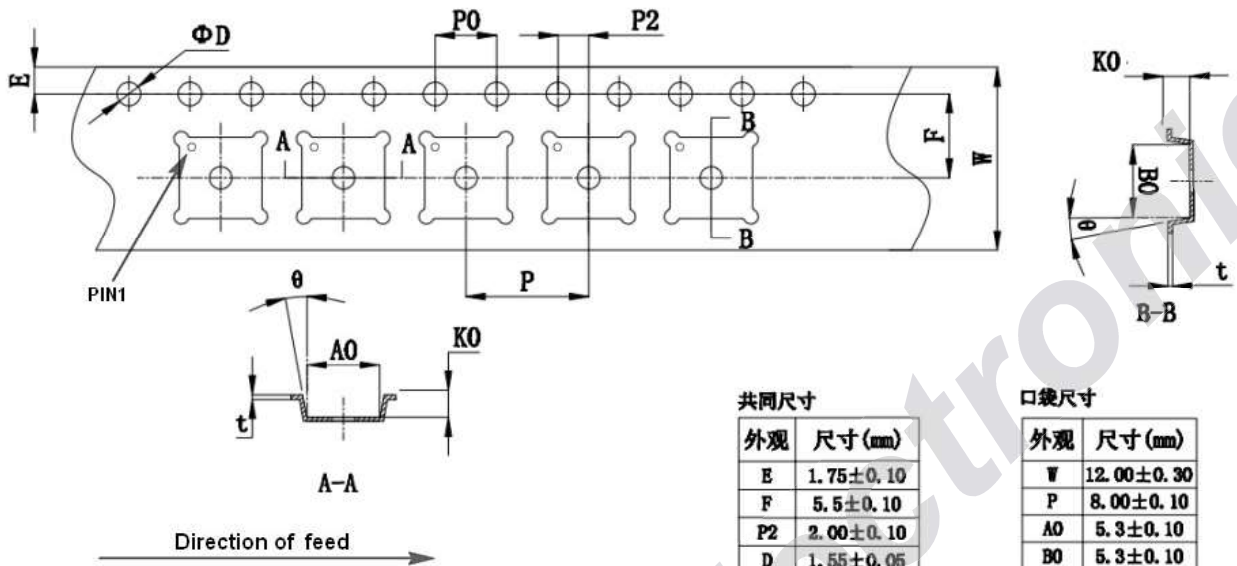


Symbol	Dimensions In Millimeters			Symbol	Dimensions In Millimeters		
	Min	Nom	Max		Min	Nom	Max
A	0.70	0.75	0.80	e	0.50BSC		
A1	—	0.02	0.05	Ne	3.50BSC		
b	0.18	0.25	0.30	E	4.90	5.00	5.10
c	0.18	0.20	0.25	E2	3.40	3.50	3.60
D	4.90	5.00	5.10	L	0.35	0.40	0.45
D2	3.40	3.50	3.60	h	0.30	0.35	0.40

Note 1: All dimensions are in millimeters.

Tape And Reel Information

TAPE DIMENSIONS:QFN 5*5-32

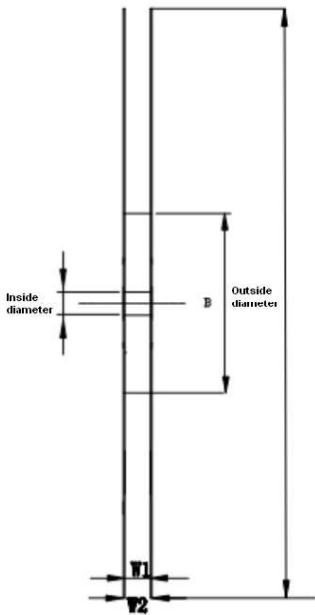
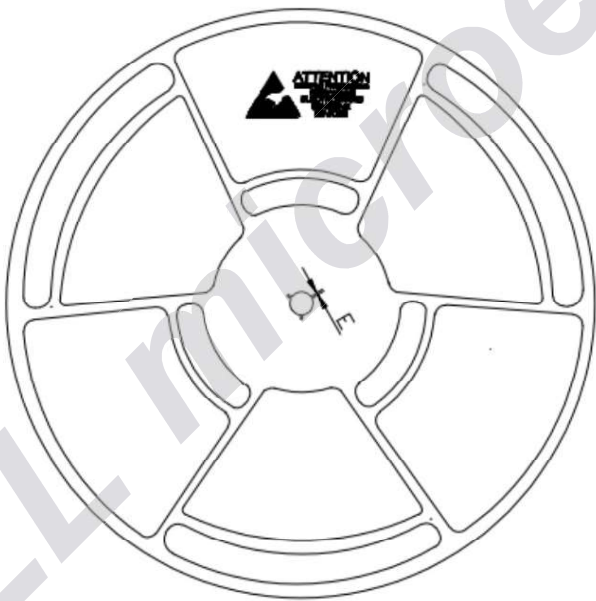


共同尺寸

外观	尺寸(mm)
E	1.75 ± 0.10
F	5.5 ± 0.10
P2	2.00 ± 0.10
D	1.55 ± 0.05
D1	1.55 ± 0.05
P0	4.00 ± 0.10
10P0	40.00 ± 0.20

口袋尺寸

外观	尺寸(mm)
W	12.00 ± 0.30
P	8.00 ± 0.10
A0	5.3 ± 0.10
B0	5.3 ± 0.10
K0	1 ± 0.10
t	0.25 ± 0.05
θ	5° TYP



Dimension(mm)	Outside diameter	B	W1	Inside diameter	W2
	$\Phi 328 \pm 1$	$\Phi 100 \pm 1$	12.5 ± 0.5	$\Phi 13.2 \pm 0.2$	14.8 ± 2

Note:

- 1) All Dimensions are in Millimeter
- 2) Quantity of Units per Reel is 5000
- 3) MSL level is level 3

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