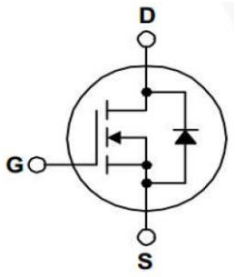
迈诺斯科技

IRFP140NPBF

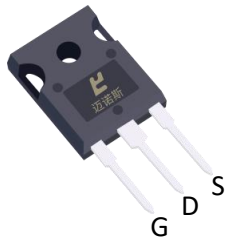
Silicon N-Channel Power MOSFE

Description

IRFP140NPBF,the silicon N-channel Enhanced MOSFETS, is obtained by advanced MOSFET technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor is suitable device for Synchronous Rectification, inverter systems ,high speed switching and general purpose applications.



Schematic diagram



TO-247

General Features

① V_{DS}=100V, R_{dson}<36mΩ @V_{GS}=10V, I_D=50A (Typ:27mΩ)
② Fast switching
③ 100% avalanche tested
④ Improved dv/dt capability

Application

① Power switching application
② Hard switched and High frequency circuits
③ Uninterruptible power supply

Package Marking And Ordering Information：

Ordering Codes	Package	Product Code	Packing
IRFP140NPBF	TO-247	IRFP140N	Tube

ABSOLUTE RATINGS (at TC = 25°C, unless otherwise specified)

Symbol	Parameter	Value	Units
		TO-247	
V_{DSS}	Drain-Source Voltage (VGS = 0V)	100	V
I_D	Continuous Drain Current	50	A
	Continuous Drain Current@TC = 100ºC	30	A
I_{DM}	Pulsed Drain Current(note1)	125	A
V_{GSS}	Gate-Source Voltage	±25	V
E_{AS}	Single Pulse Avalanche Energy (note2)	600	mJ
P_D	Power Dissipation (TC = 25ºC)	13	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55 to175	ºC

Thermal Resistance

Symbol	Parameter	Value	Units
		TO-247	
R_{thJC}	Thermal Resistance, Junction-to-Case	1.2	℃/W
R_{thJA}	Thermal Resistance, Junction-to-Ambient	50	

Electrical Characteristics (at T_C = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
OFF Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	100	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 100V, V_{GS} = 0V, T_J = 25ºC	--	--	2.0	μA
I_{GSS}	Gate-Source Leakage	V_{GS} = +25V,V_{DS}=0V	--	--	100	nA
		V_{GS}=-25V, V_{DS}=0V	--	--	-100	
ON Characteristics						
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{DS} = VGS, I_D = 250μA	2.0	3.0	4.0	V
$R_{DS(on)}$	Drain-Source On-Resistance (Note3)	V_{GS} = 10V, I_D = 25A	--	27	36	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{GS} =0V, V_{DS} = 25V, f = 1.0MHz	--	2120	--	pF
C_{oss}	Output Capacitance		--	420	--	
C_{rss}	Reverse Transfer Capacitance		--	110	--	
Q_g	Total Gate Charge	V_{DD} =80V, I_D = 25A, V_{GS} = 0 to 10V	--	48	--	nC
Q_{gs}	Gate-Source Charge		--	13.5	--	
Q_{gd}	Gate-Drain Charge		--	17.5	--	
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 50V, I_D =25A, V_{GS}= 10V R_G = 5.1Ω	--	15	--	ns
t_r	Turn-on Rise Time		--	46	--	
$t_{d(off)}$	Turn-off Delay Time		--	38	--	
t_f	Turn-off Fall Time		--	36	--	

Source-Drain Diode Characteristics						
I_S	Continuous Body Diode Current	T_C= 25 ºC	--	50	--	A
I_{SM}	Pulsed Diode Forward Current		--	125	--	
V_{SD}	Body Diode Voltage	T_J = 25ºC, I_{SD} = 20A, V_{GS} = 10V	--	0.86	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 10V,I_S = 25A, d_{iF}/d_t =100A /μs	--	63	--	ns
Q_{rr}	Reverse Recovery Charge		--	148	--	μC

Notes

Note1：Repetitive Rating: Pulse width limited by maximum junction temperature

Note2：IAS = 30A, VDD = 50V, RG = 25 Ω, Starting TJ = 25ºC

Note3：Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

Characteristics Curves

Figure 1. Typical Output Characteristics

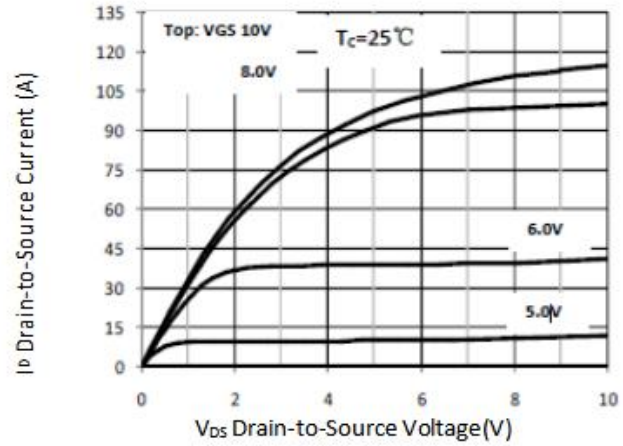


Figure 2. Typical Transfer Characteristics

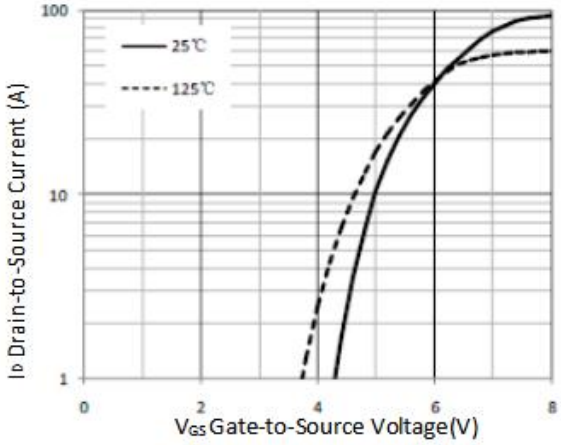


Figure 3. Normalized On-Resistance Vs Temperature

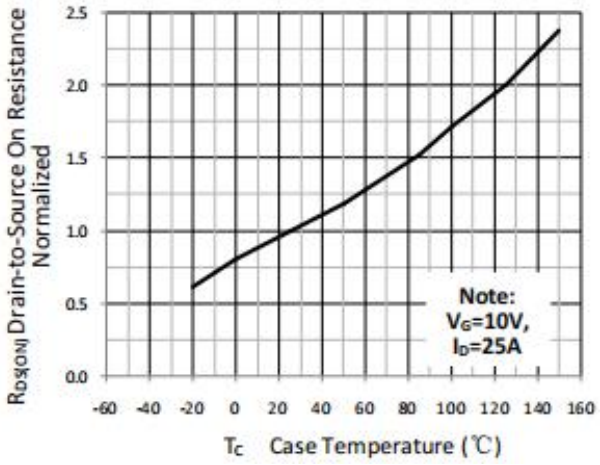


Figure 4. On-Resistance Vs Drain Current

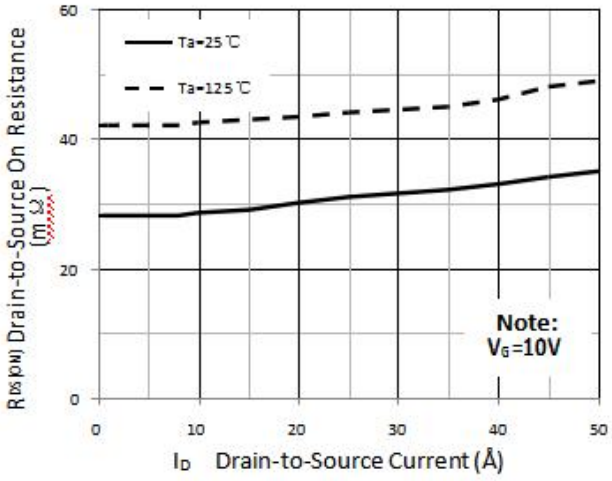


Figure 5. Typical Capacitance Vs Drain-Source Voltage

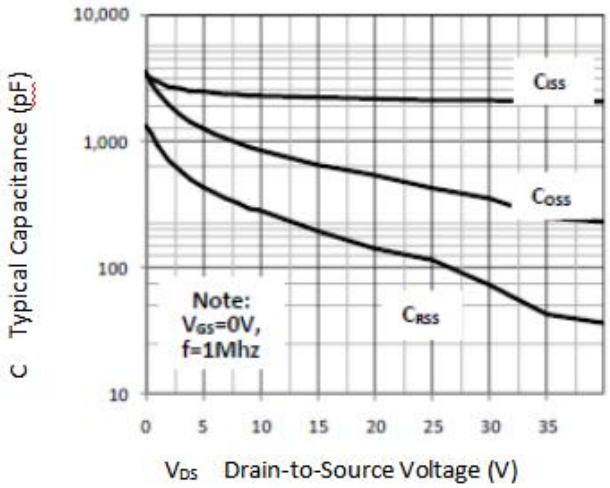


Figure 6. Typical Gate Charge Vs Gate-Source Voltage

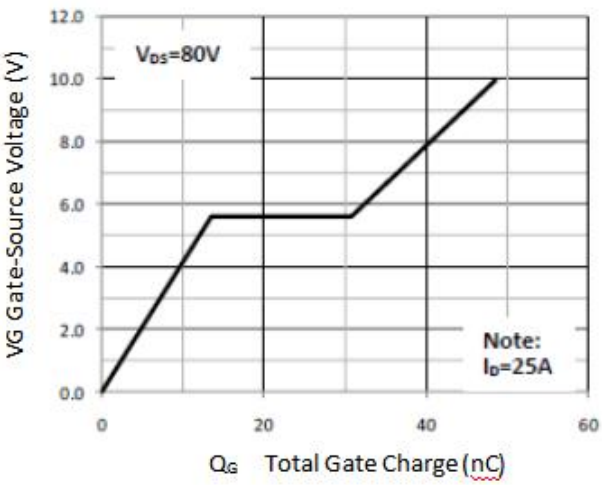
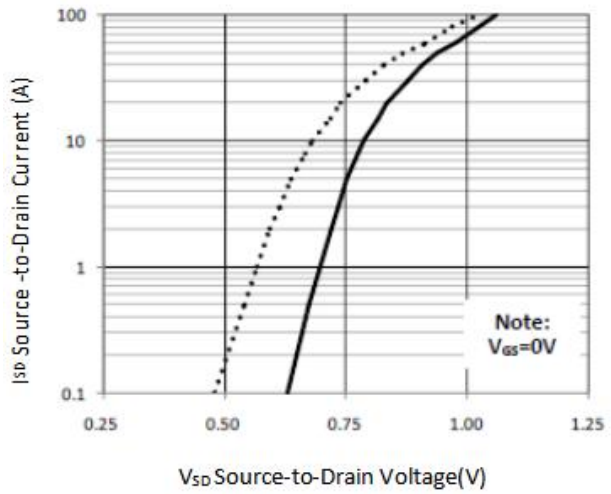
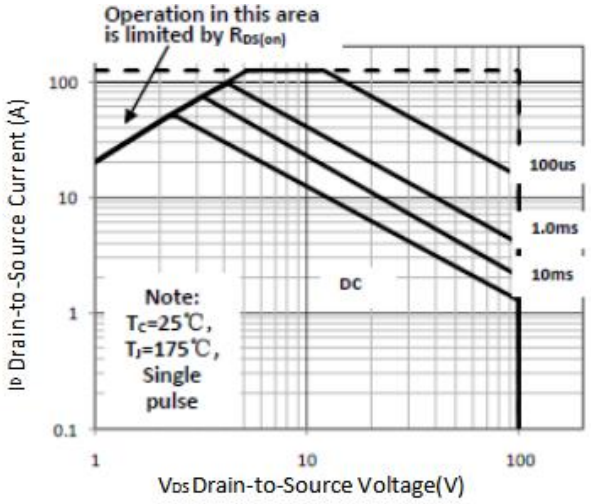
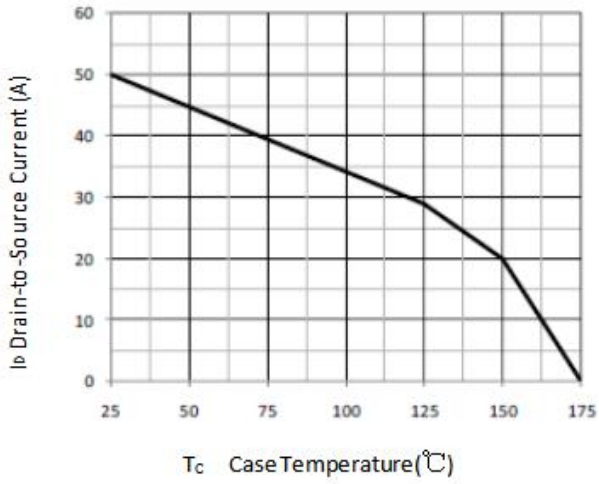
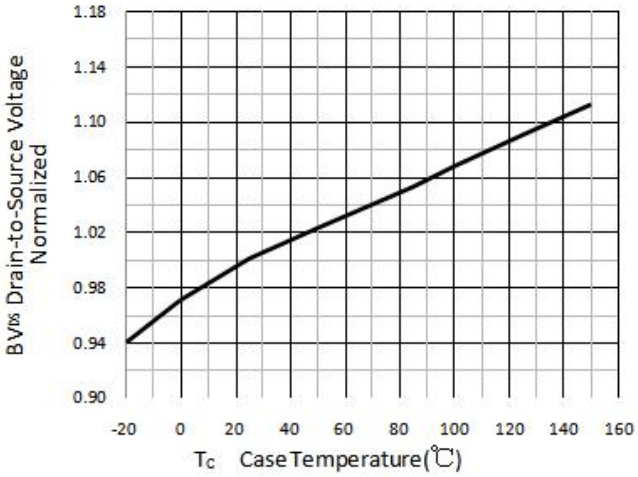
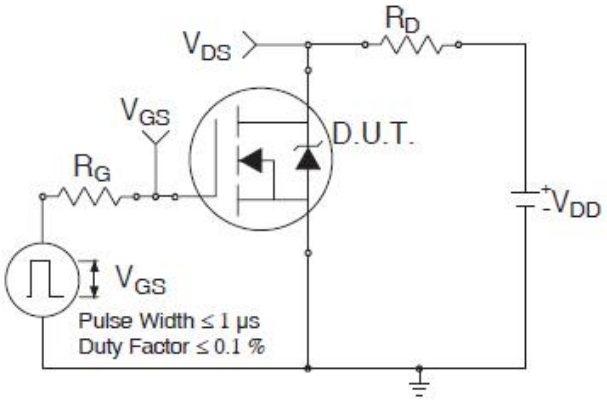
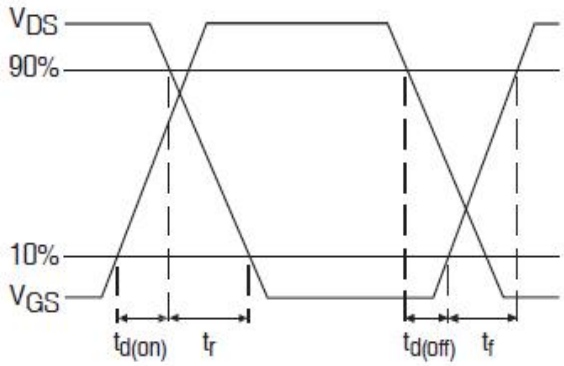
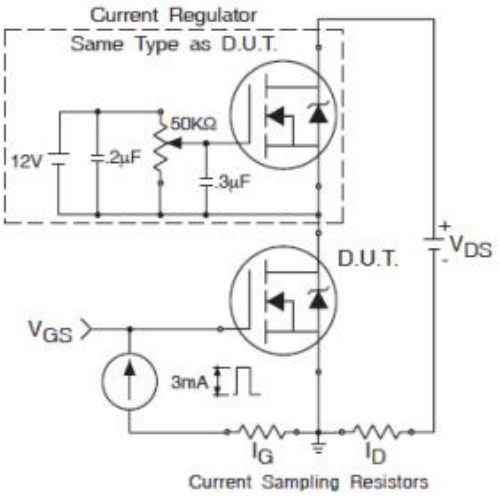
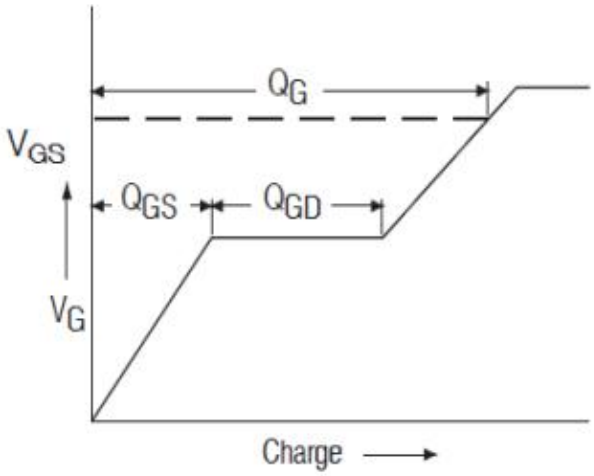
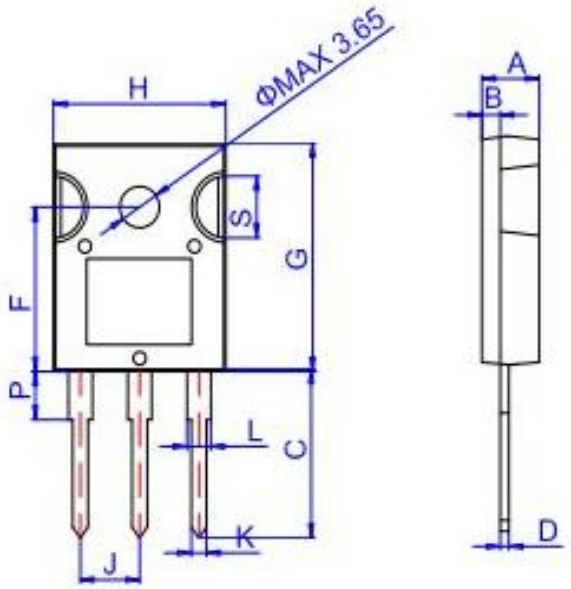


Figure 7. Typical Source-Drain Diode Forward Voltage	Figure 8. Maximum Safe Operating Area
	
Figure 9. Maximum Drain Current Vs Temperature	**Figure 10.Normalized Drain-Source Voltage Vs Temperature**
	

Test Circuit and Waveform

Figure 11a. Switching Time Test Circuit	Figure 11b. Switching Time Waveforms
	
Figure 12a. Gate Charge Test Circuit	**Figure 12b. Basic Gate Charge Waveforms**
	

Package Information



Symbol	Values(mm)	
	MIN	MAX
A	4.9	5.4
B	1.6	2.0
C	14.35	15.4
D	0.5	0.8
F	14.4	15.1
G	19.7	20.6
H	15.4	16.2
J	5.3	5.6
K	1.3	1.5
L	2.8	3.3
ϕp	3.7	4.2
S	5.35	5.65

TO-247 Package

NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shenzhen Minos reserves the right to make changes in this specification sheet and is subject to change without prior notice.

CONTACT:

深圳市迈诺斯科技有限公司（总部）

地址：深圳市福田区华富街道田面社区深南中路4026号田面城市大厦16D

邮编：518025

电话：0755-83273777