74LVC1G57

Low-power configurable multiple function gate

Product datasheet, Rev. 1.0 Aug 08, 2024

1. General Description

The 74LVC1G57 is a configurable multiple function gate with Schmitt-trigger inputs. The device can be configured as any of the following logic functions AND, OR, NAND, NOR, XNOR, inverter and buffer; using the 3-bit input. All inputs can be connected directly to V_{CC} or GND. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and Benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- ±24 mA output drive (VCC = 3.0 V)
- CMOS low power dissipation
- Latch-up performance exceeds 200 mA
- Direct interface with TTL levels
- I_{OFF} circuitry provides partial Power-down mode operation
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 3B exceeds 8000 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options

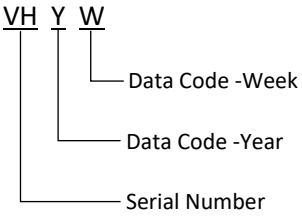
3. Ordering Information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Quantity
74LVC1G57GV	VHYW	SOT23-6L	SOT23 package, 6 pins 2.92 mm × 1.6 mm; 1.25 mm (Max) height	3000
74LVC1G57GW	VHYW	SOT363	SOT363 package, 6 pins 2.1 mm × 1.25 mm; 1.1 mm (Max) height	3000

MARKING INFORMATION

NOTE: YW = Data Code.



4. Function Diagram

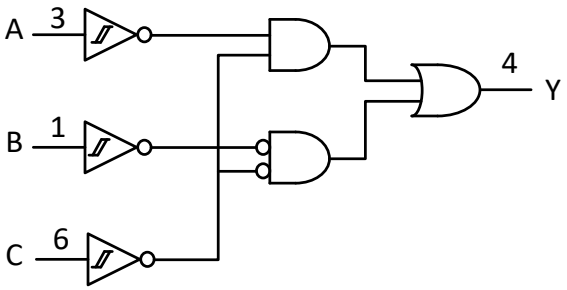


Fig. 1. Logic symbol

5.Pinning Information

5.1. Pinning

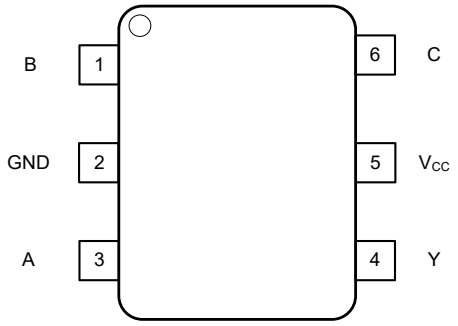


Fig. 2. Top view pin configuration SOT23-6 and SOT363

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
B	1	Data input
GND	2	Ground (0V)
A	3	Data input
Y	4	Data output
V_{CC}	5	Supply voltage
C	6	Data input

6.Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Input			Output
C	**B**	**A**	**Y**
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

6.1. Logic configurations

Table 4. Function selection table

Logic function	Figure
2-input AND	see Fig. 3
2-input AND with both inputs inverted	see Fig. 6
2-input NAND with inverted input	see Fig. 4 and Fig. 5
2-input OR with inverted input	see Fig. 4 and Fig. 5
2-input NOR	see Fig. 6
2-input NOR with both inputs inverted	see Fig. 3
2-input XNOR	see Fig. 7
Inverter	see Fig. 8
Buffer	see Fig. 9

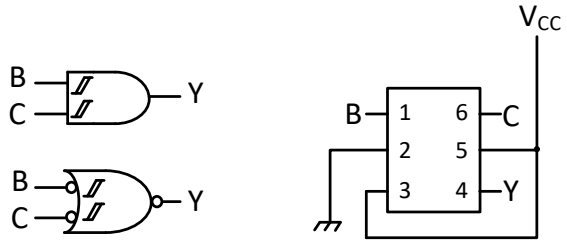


Fig. 3. 2-input AND gate or 2-input NOR gate with both inputs inverted

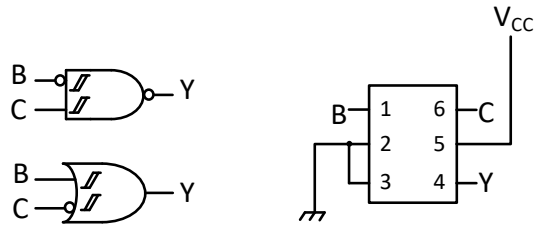


Fig. 4. 2-input NAND gate with input B inverted or 2-input OR gate with inverted C input

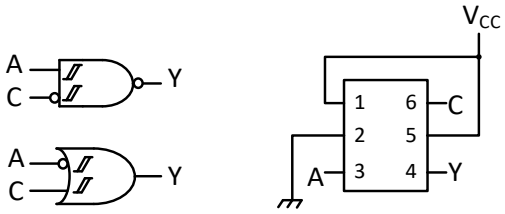


Fig. 5. 2-input NAND gate with input C inverted or 2-input OR gate with inverted A input

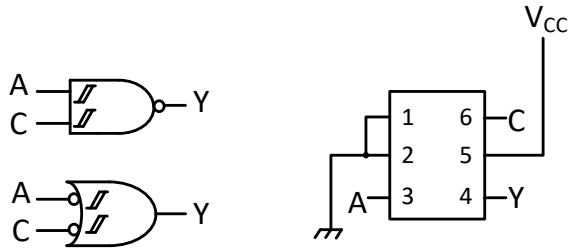


Fig. 6. 2-input NOR gate or 2-input AND gate with both inputs inverted

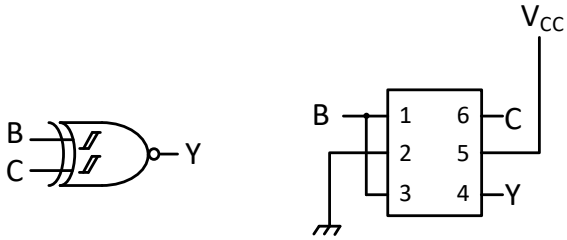


Fig. 7. 2-input XNOR gate

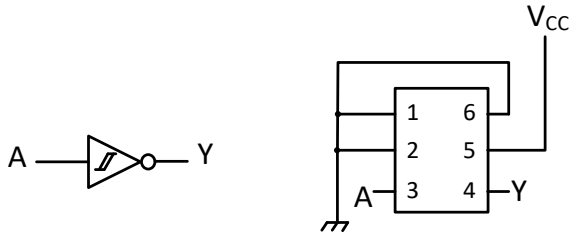


Fig. 8. Inverter

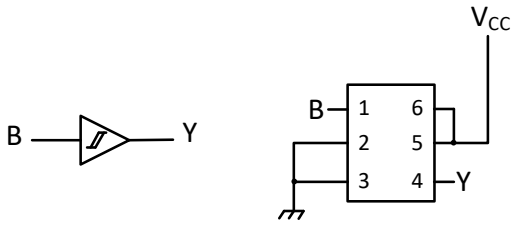


Fig. 9. Buffer

7.Absolute Maximum Ratings

Stresses exceeding the absolut`e maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 5. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50		mA
V_I	input voltage	[1]	-0.5	6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		±50	mA
V_O	output voltage	Active mode [1]	-0.5	6.5	V
		Power-down mode; V_{CC} = 0 V [1]	-0.5	6.5	V
I_O	output current	V_O = 0 V to V_{CC}		±50	mA
I_{CC}	supply current			100	mA
I_{GND}	ground current		-100		mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to + 125 °C		250	mW
T_{stg}	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8.Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 6. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65		5.5	V
V_I	input voltage		0		5.5	V
V_O	output voltage	Active mode	0		V_{CC}	V
		Power-down mode; V_{CC} = 0V	0		5.5	V
T_{amb}	ambient temperature		-40		125	°C

9.Static Characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}						
		I_O = -100µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} - 0.1			V_{CC} - 0.1		V
		I_O = -4 mA; V_{CC} = 1.65 V	1.2	1.6		0.95		V
		I_O = -8 mA; V_{CC} = 2.3 V	1.9	2.2		1.7		V
		I_O = -12 mA; V_{CC} = 2.7 V	2.2	2.5		1.9		V
		I_O = -24 mA; V_{CC} = 3.0 V	2.3	2.7		2.0		V
		I_O = -32 mA; V_{CC} = 4.5 V	3.8	4.2		3.4		V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}						
		I_O = 100µA; V_{CC} = 1.65 V to 5.5 V			0.10		0.10	V
		I_O = 4 mA; V_{CC} = 1.65 V		0.02	0.45		0.70	V
		I_O = 8 mA; V_{CC} = 2.3 V		0.06	0.30		0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V		0.12	0.40		0.60	V
		I_O = 24 mA; V_{CC} = 3.0 V		0.28	0.55		0.80	V
		I_O = 32 mA; V_{CC} = 4.5 V		0.34	0.55		0.80	V
I_I	input leakage current	V_I = 5.5 V or GND ; V_{CC} = 0 V to 5.5 V		±0.1	±1		±1	µA
I_{OFF}	power-off leakage current	V_{CC} = 0V ; V_I or V_O = 5.5 V		±0.1	±2		±2	µA
I_{CC}	supply current	V_I = 5.5V or GND ; I_O = 0A ; V_{CC} = 5.5V		0.1	4		4	µA
ΔI_{CC}	additional supply current	per pin ; V_{CC} = 2.3V to 5.5V ; $V_I = V_{CC}$ -0.6V ; I_O = 0A		5	500		500	µA
C_I	input capacitance	V_{CC} = 3.3V ; V_I = GND to V_{CC}		5				pF

[1]All typical values are measured at T_{amb} = 25℃.

10. Dynamic Characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 11.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	A, B, C to Y; see Fig. 10 [2]						
		V_{CC} = 1.65 V to 1.95 V	4.0	15.7	26	4.0	26.5	ns
		V_{CC} = 2.3 V to 2.7 V	2.5	9.5	14	2.5	14.5	ns
		V_{CC} = 3.0 V to 3.6 V	2.0	7.1	9	2.0	9.5	ns
		V_{CC} = 4.5 V to 5.5 V	1.5	2.9	5	1.5	5.5	ns
C_{PD}	power dissipation capacitance	V_{CC} = 3.3 V V_I = GND to V_{CC} [3]		25				pF

[1] Typical values are measured at norminal at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

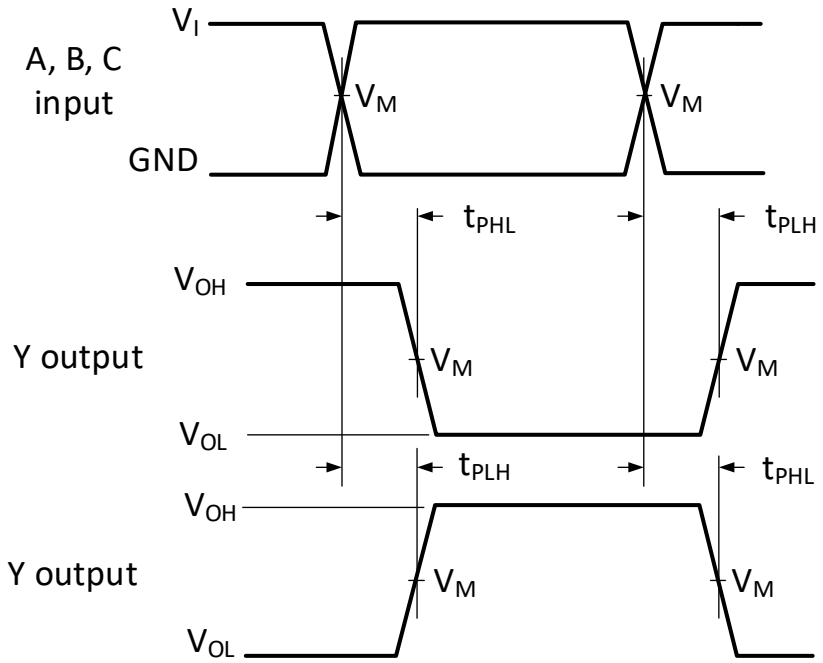
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit

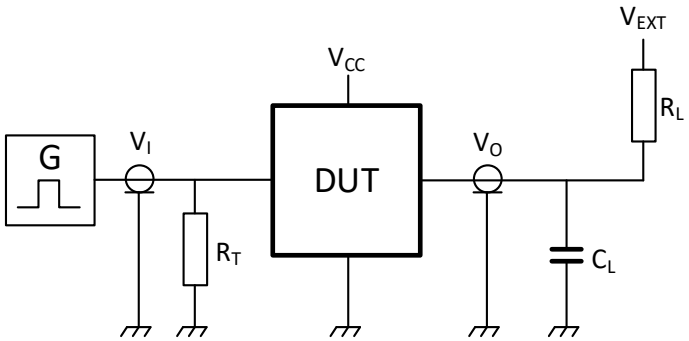


Measurement points are given in Table 9.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 10. Input A, B and C to output Y propagation delays

Table 9. Measurement points

Supply Voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in Table 10.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
V_{EXT} = External voltage for measuring switching times.

Fig. 11. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	15 pF	500 Ω	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	15 pF	500 Ω	open
3.0 V to 3.6 V	3 V	≤ 2.5 ns	15 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	15 pF	500 Ω	open

11. Transfer Characteristics

Table 11. Transfer characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{T+}	positive-going threshold voltage	see Fig. 12, Fig. 13, Fig. 14 and Fig. 15						
		V_{CC} = 1.8 V	0.70	1.09	1.20	0.67	1.20	V
		V_{CC} = 2.3 V	1.11	1.36	1.60	1.08	1.60	V
		V_{CC} = 3.0 V	1.50	1.69	2.00	1.47	2.00	V
		V_{CC} = 4.5 V	2.16	2.39	2.74	2.13	2.74	V
		V_{CC} = 5.5 V	2.61	2.86	3.33	2.58	3.33	V
V_{T-}	negative-going threshold voltage	see Fig. 12, Fig. 13, Fig. 14 and Fig. 15						
		V_{CC} = 1.8 V	0.30	0.6	0.72	0.30	0.75	V
		V_{CC} = 2.3 V	0.58	0.77	1.00	0.58	1.03	V
		V_{CC} = 3.0 V	0.80	1.09	1.30	0.80	1.33	V
		V_{CC} = 4.5 V	1.21	1.62	1.90	1.21	1.93	V
		V_{CC} = 5.5 V	1.45	1.99	2.29	1.45	2.32	V
V_H	hysteresis voltage	see Fig. 12, Fig. 13, Fig. 14 and Fig. 15						
		V_{CC} = 1.8 V	0.30	0.49	0.62	0.23	0.62	V
		V_{CC} = 2.3 V	0.40	0.58	0.80	0.34	0.80	V
		V_{CC} = 3.0 V	0.50	0.6	1.00	0.44	1.00	V
		V_{CC} = 4.5 V	0.71	0.76	1.20	0.65	1.20	V
		V_{CC} = 5.5 V	0.71	0.86	1.40	0.65	1.40	V

[1]All typical values are measured at T_{amb} = 25℃.

11.1. Waveforms transfer characteristics

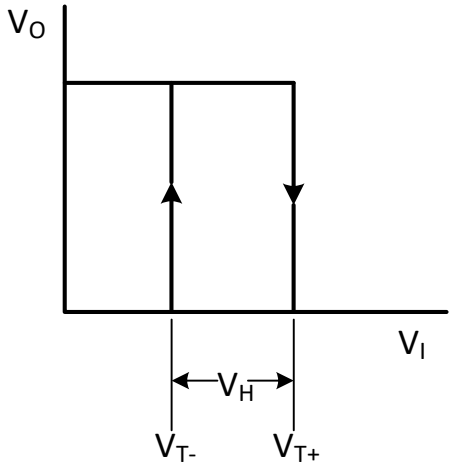
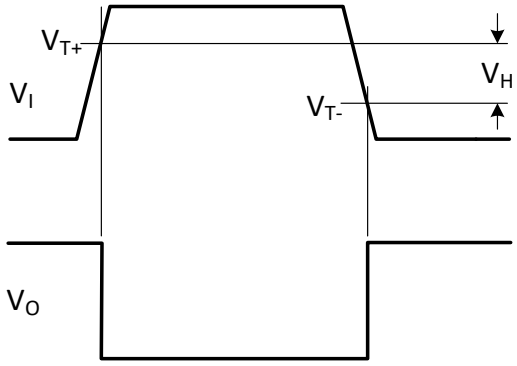


Fig. 12. Transfer characteristic



V_{T+} and V_{T-} limits at 70% and 20%.

Fig. 13. Definition of V_{T+}, V_{T-} and V_H

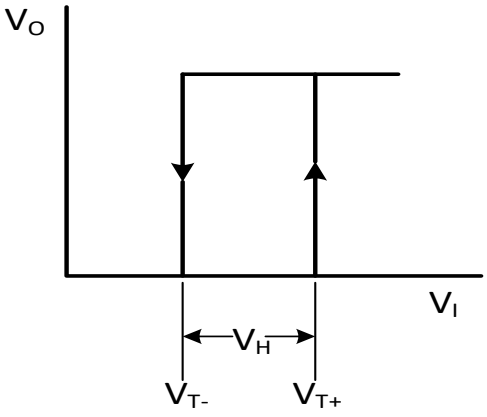


Fig. 14. Transfer characteristic

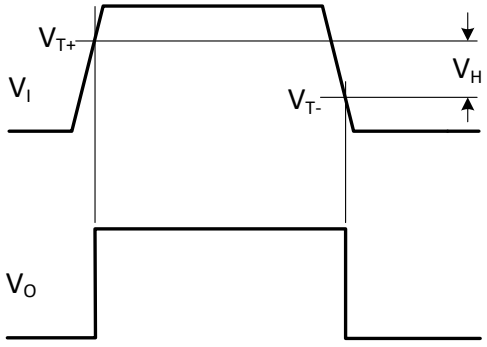
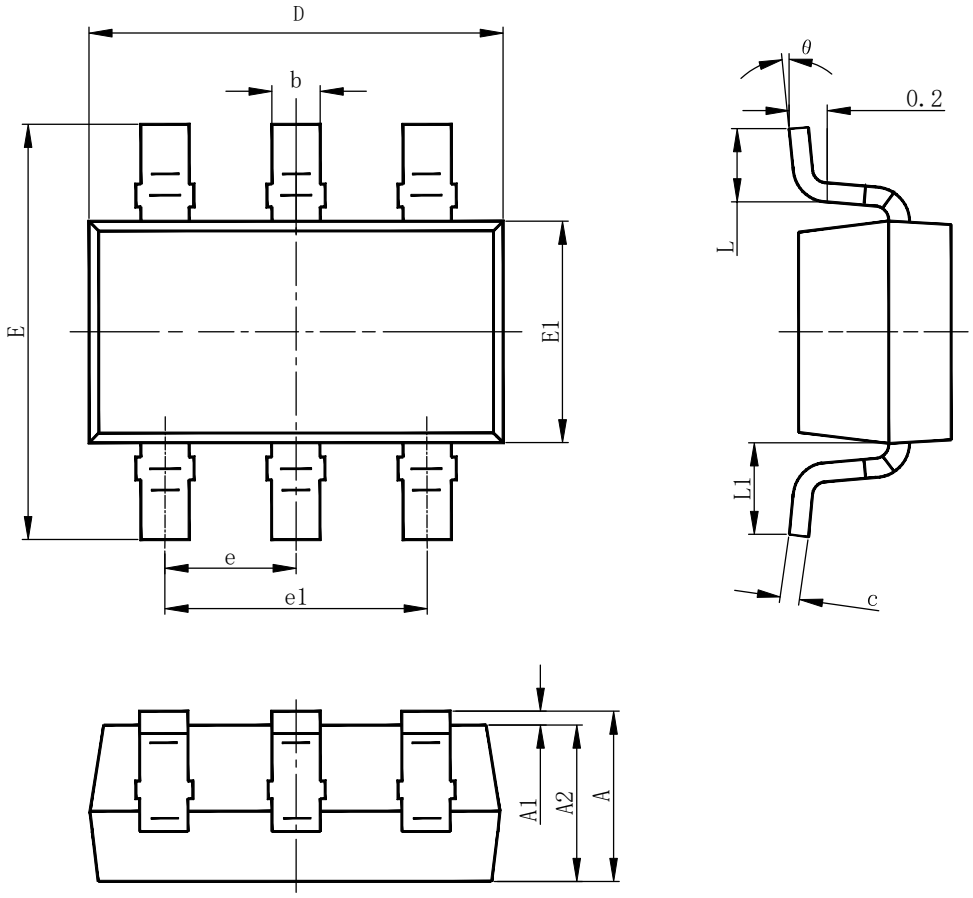


Fig. 15. Definition of V_{T+}, V_{T-} and V_H

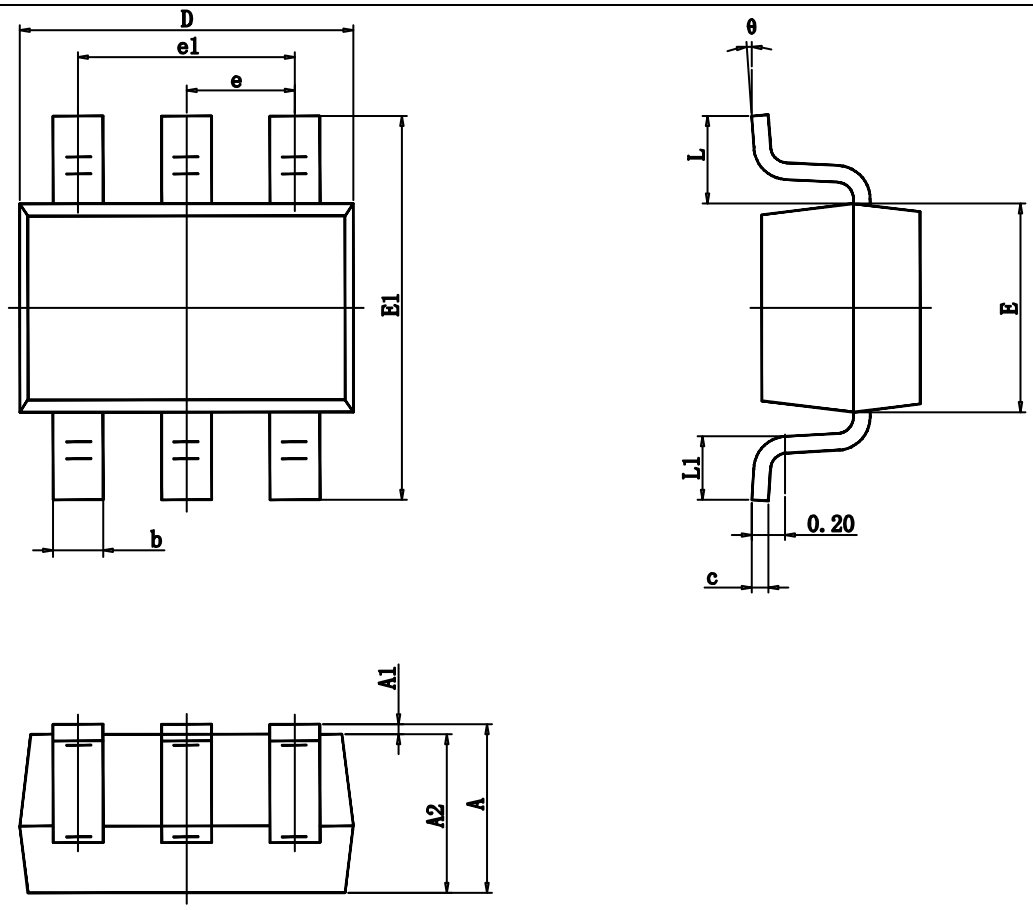
12. Package Outline

SOT23-6L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600REF.		0.024REF.	
θ	0°	8°	0°	8°

SOT363



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.110	0.175	0.004	0.007
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 TYP.		0.026 TYP.	
e1	1.200	1.400	0.047	0.055
L	0.525 REF.		0.021 REF.	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

14. Revision History

Table 13. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
74LVC1G57Rev. 1.0	Aug 08, 2024	Product datasheet		