GENERAL DESCRIPTION

This document describes specifications for the F1650NLGI Zero/Complex IF Modulator implementing Zero-Distortion™ technology for low power consumption with improved ACLR. This device interfaces directly to a high performance Tx dual DAC.

COMPETITIVE ADVANTAGE

In typical multi-mode, multi-carrier basestation transmitters the modulator has limited linearity and high power consumption which penalizes the system ACLR and system Power consumptions budgets in a Digital-Pre-Distortion environment.

The IDTF1650 is designed to eliminate these penalties by embedding Zero-Distortion™ technology into the device such that very high IP3 and IP2 are achieved with minimal current draw.

- Power consumption ⇩**45%**
- IM3 Distortion ⇩**12 dB**

Zero-Distortion™

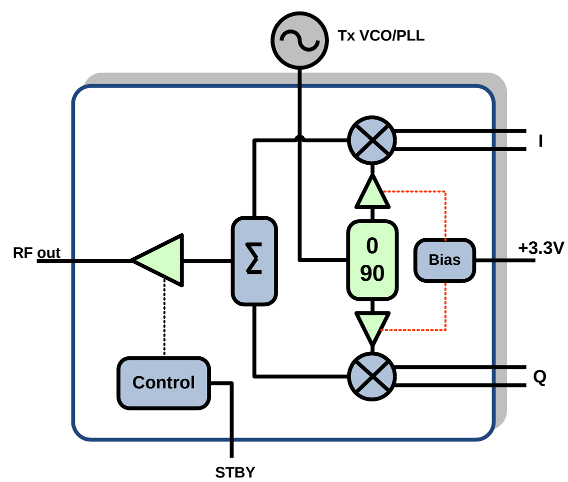
PART# MATRIX

Part#	RF freq Range	$IP2_O$	Power Cons.	$IP3_O$	Noise
F1650	**600 – 2400**	**+60 dBm**	**587 mW**	**+36 dBm**	**-158 dBm/Hz**

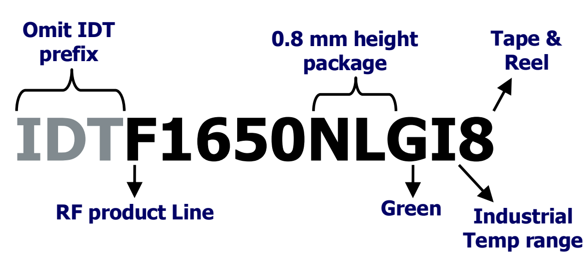
FEATURES

- Power Gain = 3.25dB
- Direct 100Ω differential drive from Tx DAC
- **< 590mW Power Consumption @ 2GHz**
- -158dBm/Hz Output Noise
- $IP2_O$ = +60dBm @ 2GHz
- **$IP3_O$ = +36dBm @ 2GHz**
- Excellent native LO and image suppression
- 600 MHz input 1dB Bandwidth
- 600 MHz to 2400MHz RF BW
- **Constant LO impedance when OFF**
- 3.3V Single Power Supply
- LO port can be driven single ended or differential
- 4mm x 4mm 24-pin TQFN package

DEVICE BLOCK DIAGRAM



ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS

VDD to GND	-0.3V to +3.6V
STBY	-0.3V to (VDD + 0.3V)
BB_I+, BB_I-, BB_Q+, BB_Q-	-0.3V to 1.8V
LO_IN	-0.3V to 0.3V
RF_OUT	(VDD-0.35V) to (VDD-0.05V)
Continuous Power Dissipation	1.5W
θ_{JA} (Junction – Ambient)	+45°C/W
θ_{JC} (Junction – Case) The Case is defined as the exposed paddle	+2.5°C/W
Operating Temperature Range (Case Temperature)	T_{CASE} = -40°C to +105°C
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+260°C

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

IDTF1650 Recommended Operation Conditions

Parameter	Comment	Symbol	min	typ	max	units
Supply Voltage(s)	All V_{DD} pins	V_{DD}	3.15	***3.30***	3.45	*V*
Operating Temperature	Case Temperature	T_{CASE}	-40	***25***	+105	deg C
LO Freq Range	LO power -3dBm to +5dBm	F_{LO}	600		2400	*MHz*
BB Freq Range	▪ F_{LO} = 1950 MHz, BB_IQ = 200 mV ▪ P_{RF} degrades < 1 dB	F_{BB}	DC		600	*MHz*

IDTF1650 SPECIFICATION

See application circuit. Typical values are measured at V_{DD} = +3.3V, F_{LO} = 1950 MHz, P_{LO} = 0 dBm, T_{CASE}= +25°C, STBY = GND, BB_IQ frequency = 49, 50 MHz, BB_I&Q levels = 200 mVp-p each (14 dB backoff from 1V DAC compliance), I & Q = 0.250V common-mode bias unless otherwise noted.

Parameter	Comment	Symbol	min	typ	max	units
Logic Input High	For STBY Pin	V_{IH}	***1.07***			V
Logic Input Low	For STBY Pin	V_{IL}			***0.68***	V
Logic Current	For STBY Pin	I_{IH}, I_{IL}	***-100***		***+1***	µA
Supply Current (ON)	Total V_{DD}	I_{SUPP}		***178***	***210***[1]	mA
Supply Current (STBY)	Total V_{DD}, STBY = V_{IH}	I_{STBY}		***6***	***15***	mA
LO Power	600MHz to 2400MHz	P_{LO}	-3		+5	dBm
BB Input Resistance (Differential)	Freq = 100 MHz	R_{BB}		113		Ω
BB Common Mode Voltage	• DC couple to LCM DAC • T_{CASE} = -40C to +105C • V_{DD} = 3.3 V • LO level = 0dBm	V_{CM}	0.1	0.25	0.8	V
BB input voltage compliance range	For each BB pin		0		1	Vpeak
LO port Impedance	• Single Ended (RL < -10dB) • Can be driven differentially	Z_{LO}		50		Ω
RF port Impedance	Single Ended (RL < -10dB)	Z_{RF}		50		Ω
Power Gain		G	***2.25***	***3.25***	***4.25***	dB
LO Path noise	• Calc. from Noise v. P_{OUT} • + 10 MHz offset, 1.0 GHz F_{LO}	Φ_{N_LO}		-157		dBc/Hz
Output IP3 @ 850 MHz	LO = 800 MHz	$IP3_{O1}$		35		
Output IP3 @ 2.0 GHz	LO = 1950 MHz	$IP3_{O2}$	***30***	***36***		dBm
Output IP3 @ 2.45 GHz	LO = 2400 MHz	$IP3_{O3}$		33		
Output IP2 @ 850 MHz	LO = 800 MHz	$IP2_{O1}$		63		
Output IP2 @ 2.0 GHz	LO = 1950 MHz	$IP2_{O}$	55[2]	60		dBm
Output IP2 @ 2.45 GHz	LO = 2400 MHz	$IP2_{O3}$		60		
LO (Carrier) Suppression	Native, Uncorrected F_{LO} = 1950 MHz	LO_{supp}		***-37***	***-30***	dBm
Sideband (Image) Suppression	Native, Uncorrected F_{LO} = 1950 MHz	SS		***-41***	***-30***	dBc
Output P1dB	Output Compression	$P1dB_{O}$		15		dBm
Output Noise	• 10 MHz offset from LO • BB I&Q levels = 0 V_{P-P}	NSD	-157	-158		dBm/Hz

SPECIFICATION NOTES:

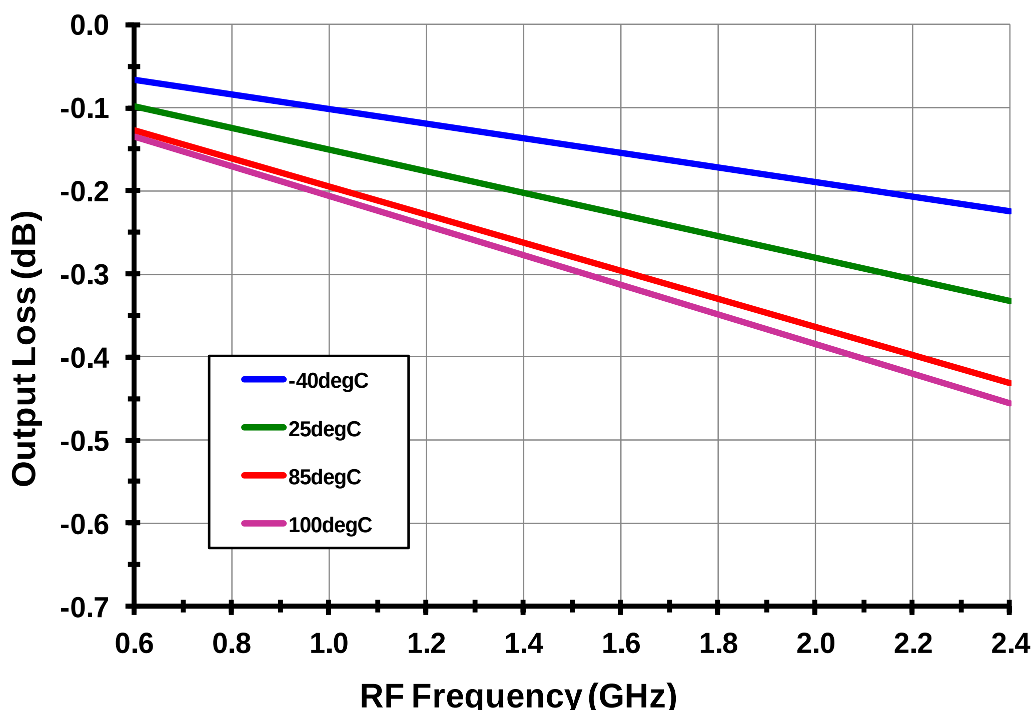
1 – Items in min/max columns in ***bold italics*** are Guaranteed by Test
2 – All other Items in min/max columns are Guaranteed by Design Characterization

TYPICAL OPERATING CONDITIONS

Unless otherwise noted, the following conditions apply:

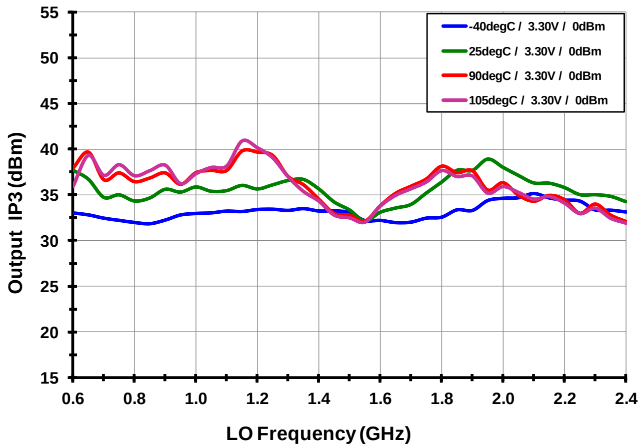
- Baseband I&Q levels = 200 mV_{PP} each (-13 dBm / Channel / Tone)
- Baseband I&Q tones = 49, 50 MHz
- Low Side Injection
- T_{AMB} = 25C, V_{CC} = 3.30 V, LO Power = 0 dBm where T_{AMB} is the ambient temperature
- V_{CM} = 0.250 Volts, where CM is common mode
- Flo = 1.95GHz unless otherwise specified, where lo is Local Oscillator
- EVKit RF output Trace and Connector Losses De-Embedded

EVkit RF output loss (Trace + Connector)

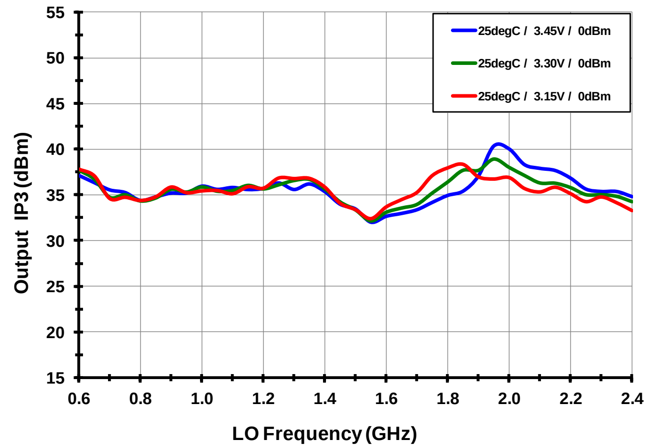


TYPICAL OPERATING CURVES (-1-)

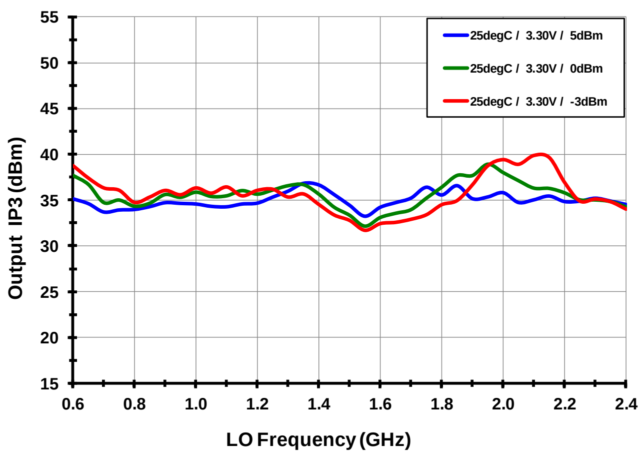
OIP3 vs. T_{AMB}



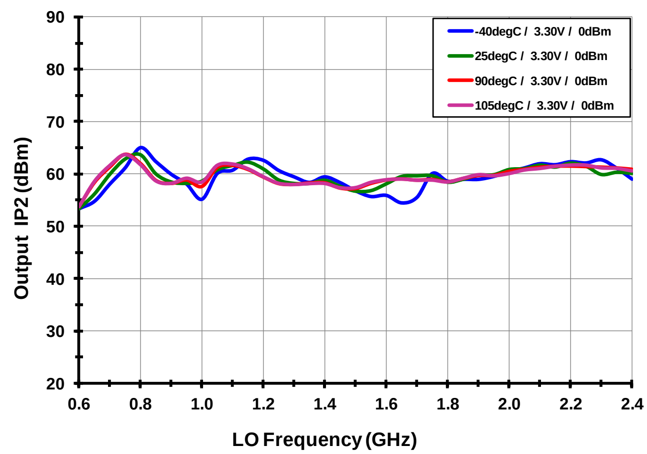
OIP3 vs. V_{CC}



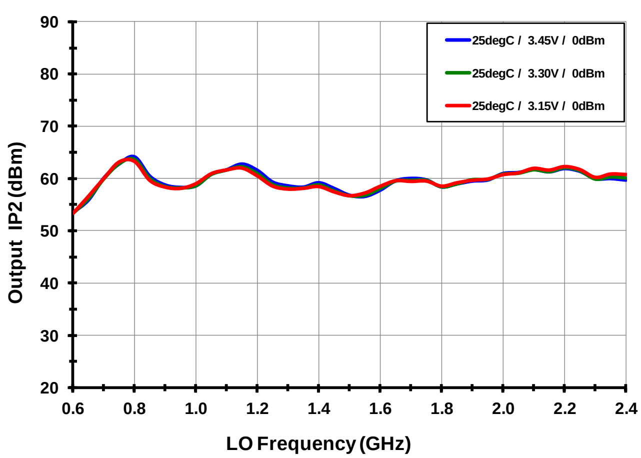
OIP3 vs. LO level



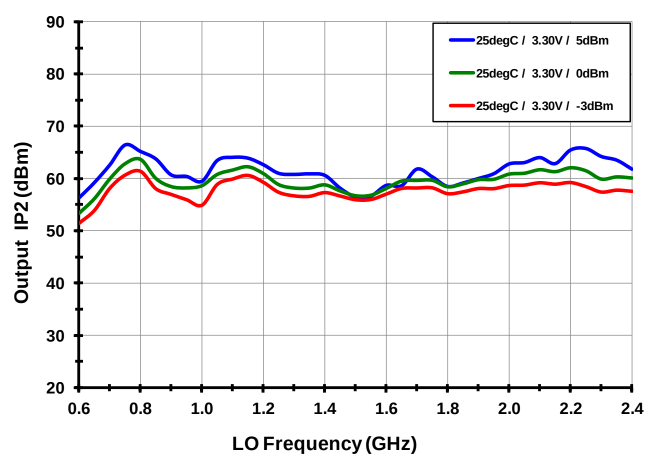
OIP2 vs. T_{AMB}



OIP2 vs. V_{CC}

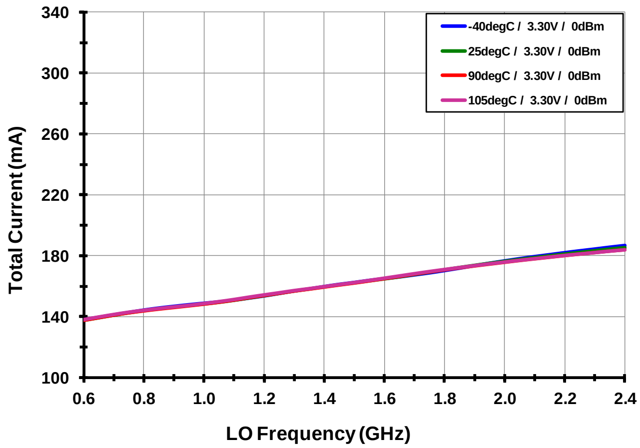


OIP2 vs. LO level

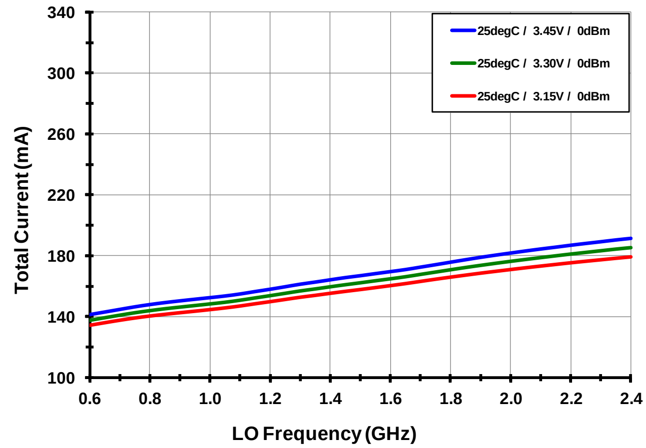


TYPICAL OPERATING CURVES (-2-)

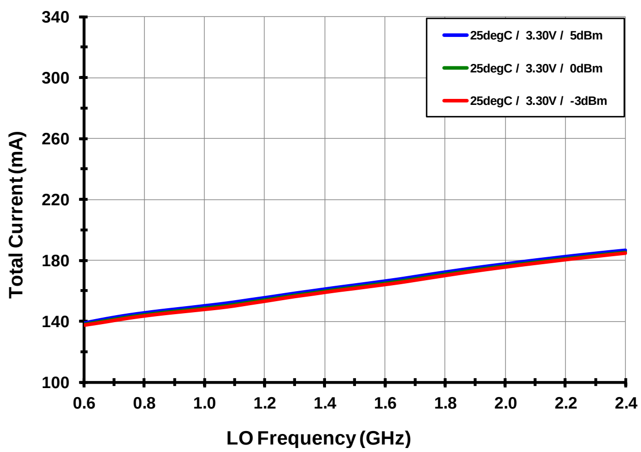
I_{CC} vs. T_{AMB}



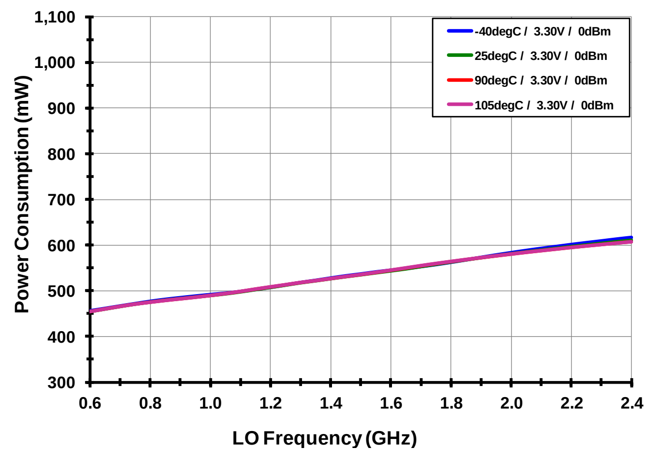
I_{CC} vs. V_{CC}



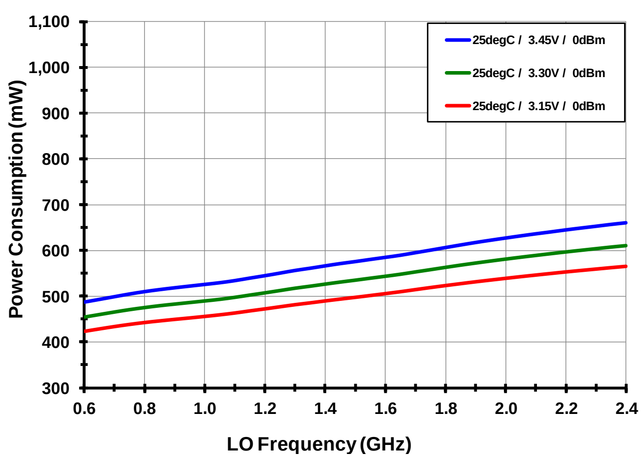
I_{CC} vs. LO level



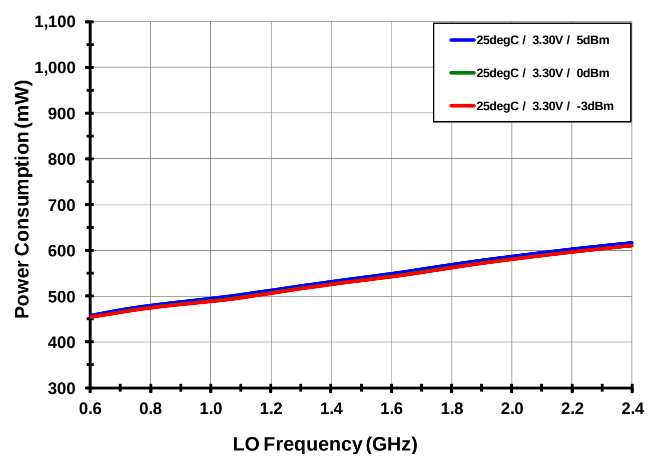
Power Consumption vs. T_{AMB}



Power Consumption vs. V_{CC}

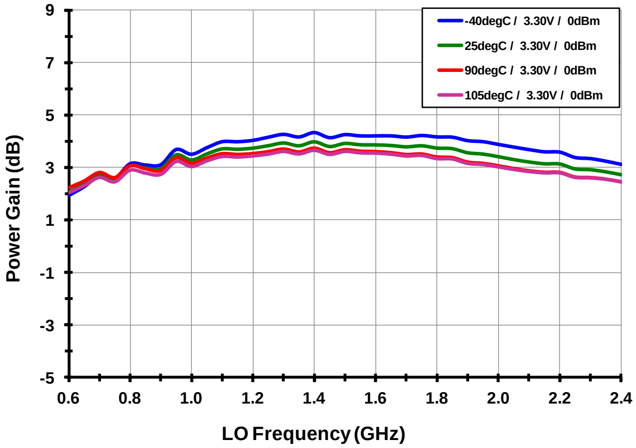


Power Consumption vs. LO level

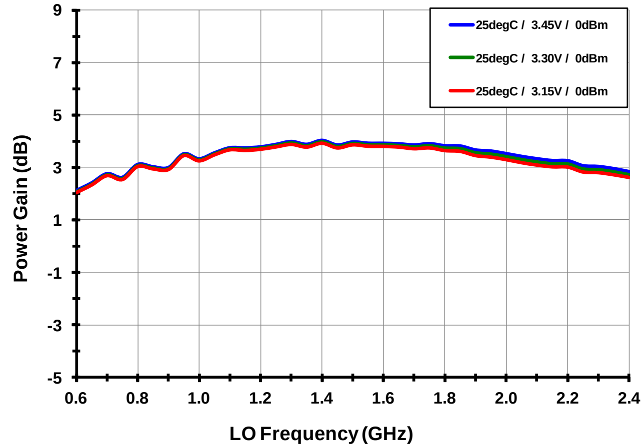


TYPICAL OPERATING CURVES (-3-)

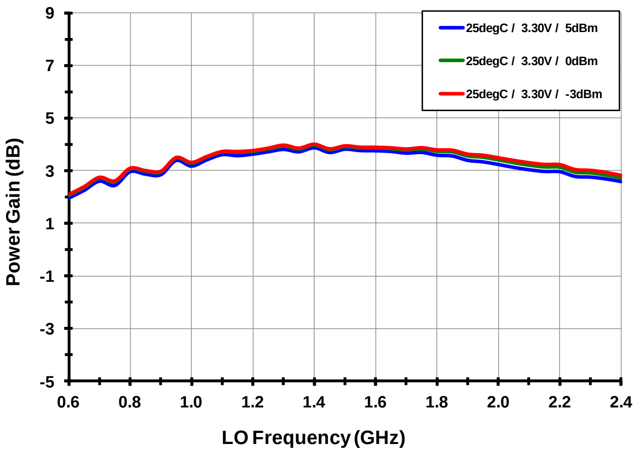
Gain vs. T_{AMB}



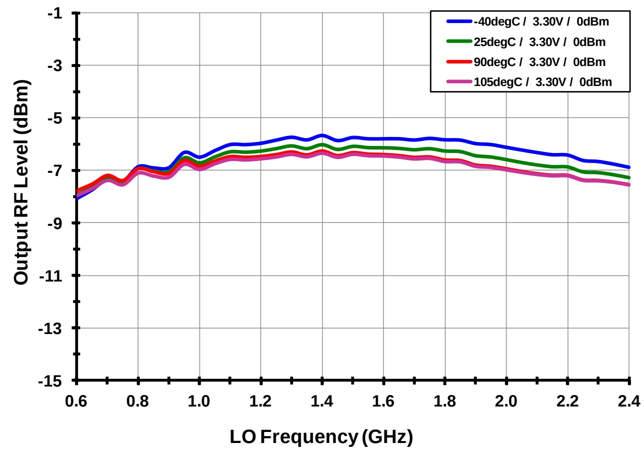
Gain vs. V_{CC}



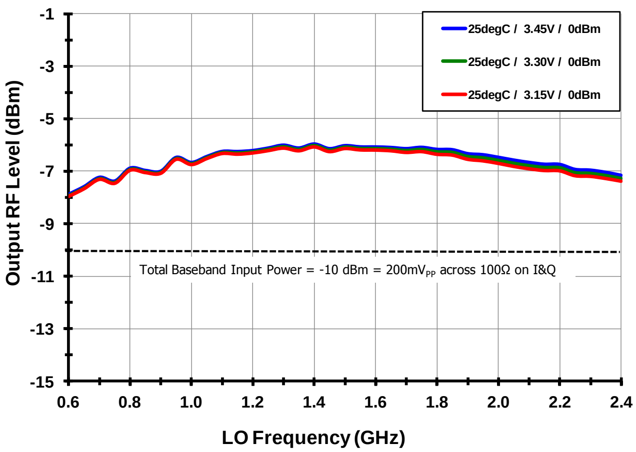
Gain vs. LO level



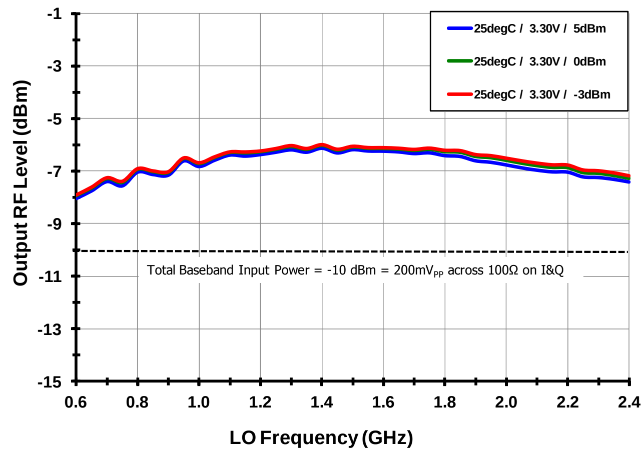
RF Output Power vs. T_{AMB}



RF Output Power vs. V_{CC}

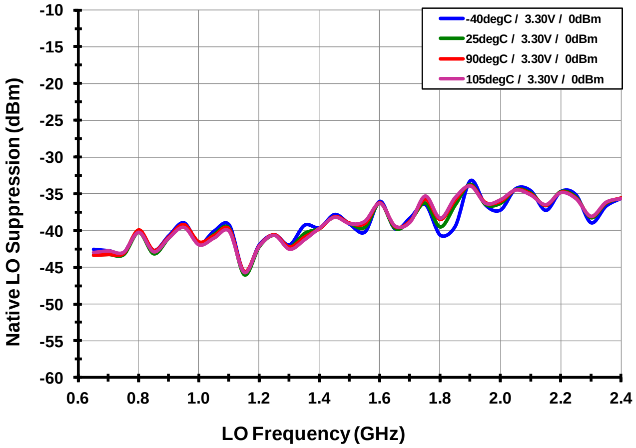


RF Output Power vs. LO level

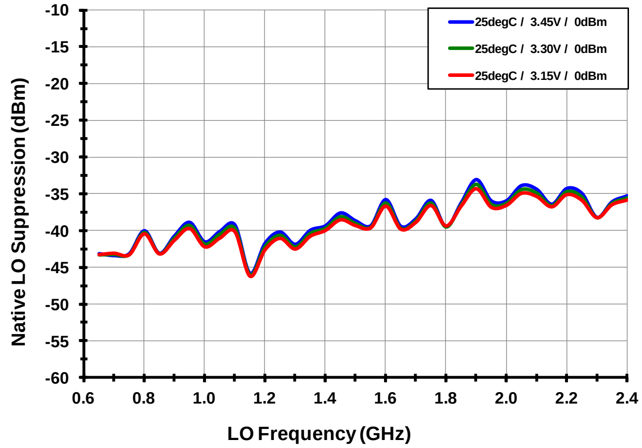


TYPICAL OPERATING CURVES (-4-)

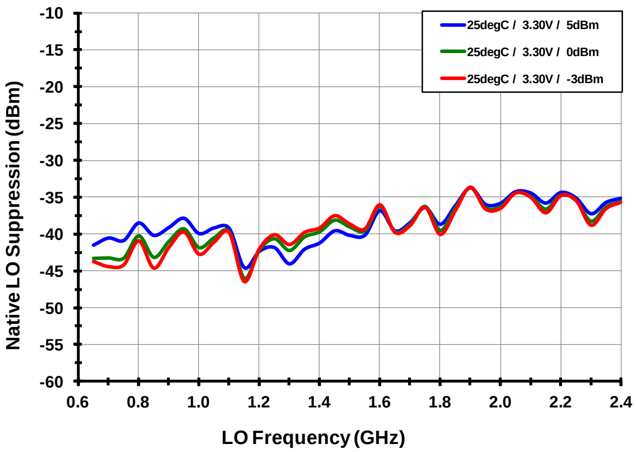
Unadjusted LO Suppression vs. T_{AMB}



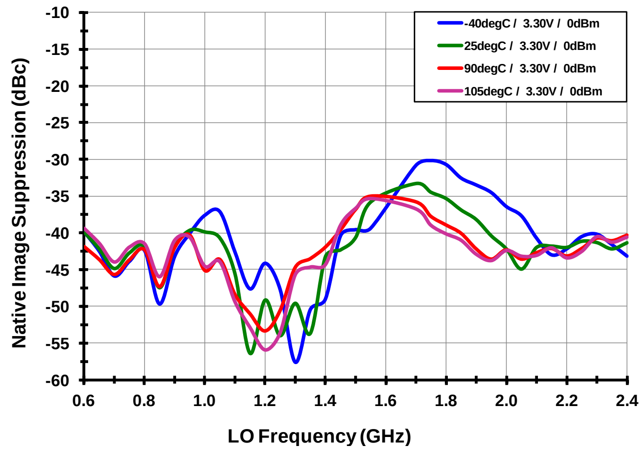
Unadjusted LO Suppression vs. V_{CC}



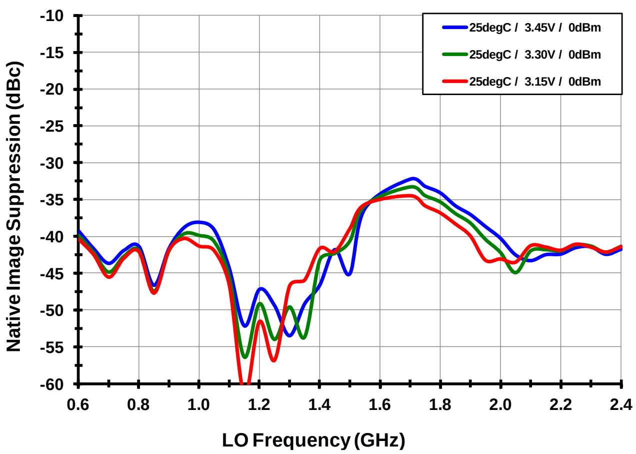
Unadjusted LO Suppression vs. LO level



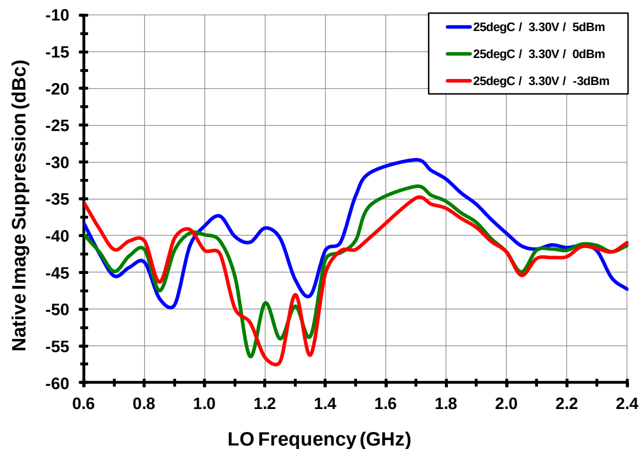
Unadjusted Sideband Suppression vs. T_{AMB}



Unadjusted Sideband Suppression vs. V_{CC}

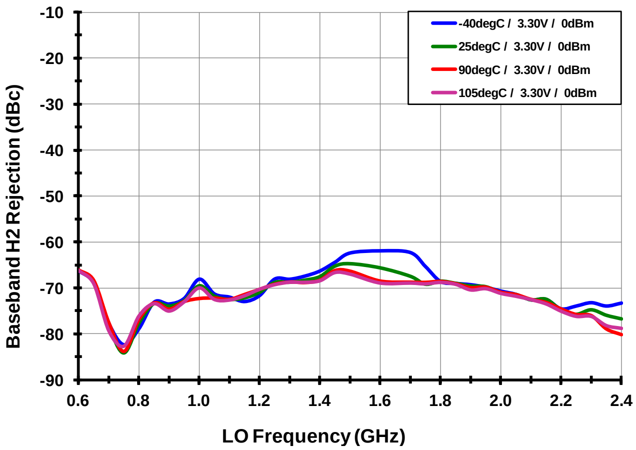


Unadjusted Sideband Suppression vs. LO level

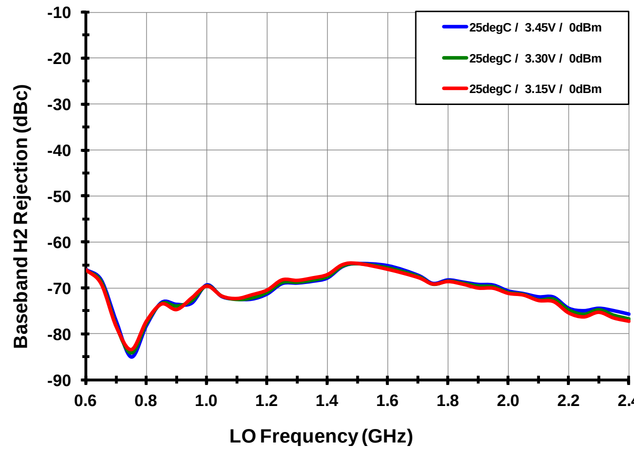


TYPICAL OPERATING CURVES (-5-)

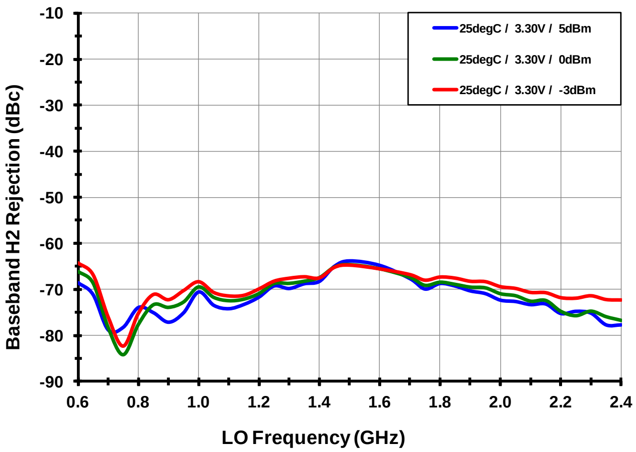
Baseband 2nd Harmonic vs. T_{AMB}



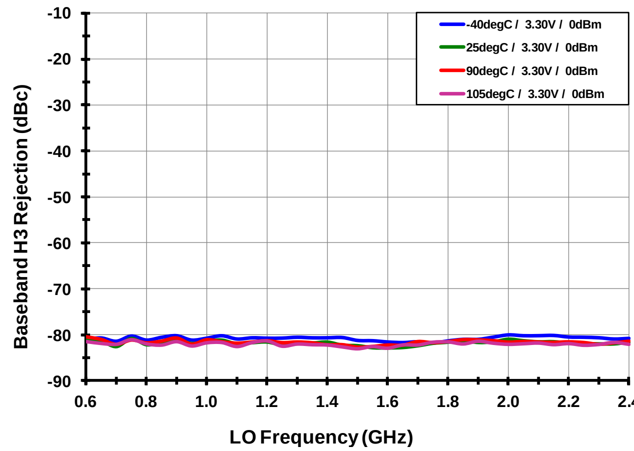
Baseband 2nd Harmonic vs. V_{CC}



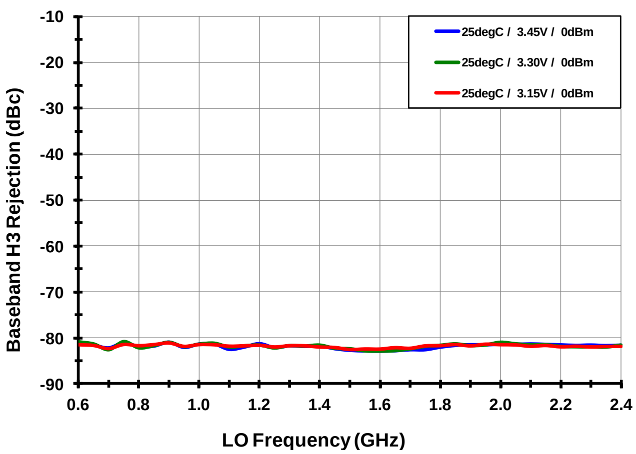
Baseband 2nd Harmonic vs. LO level



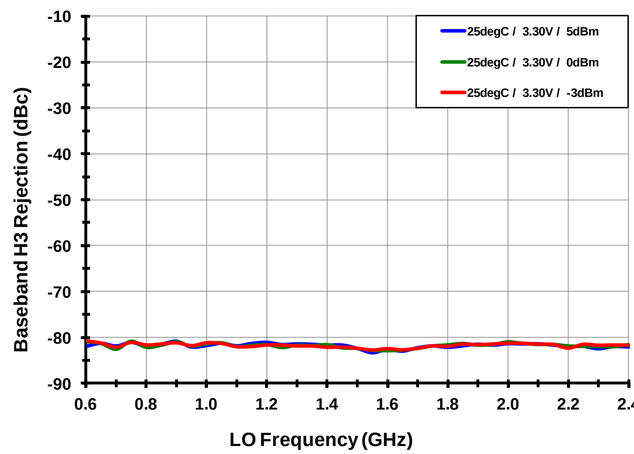
Baseband 3rd Harmonic vs. T_{AMB}



Baseband 3rd Harmonic vs. V_{CC}



Baseband 3rd Harmonic vs. LO level



RENESAS

TYPICAL OPERATING CURVES (-6-)

LO Leakage (Carrier) Nulling

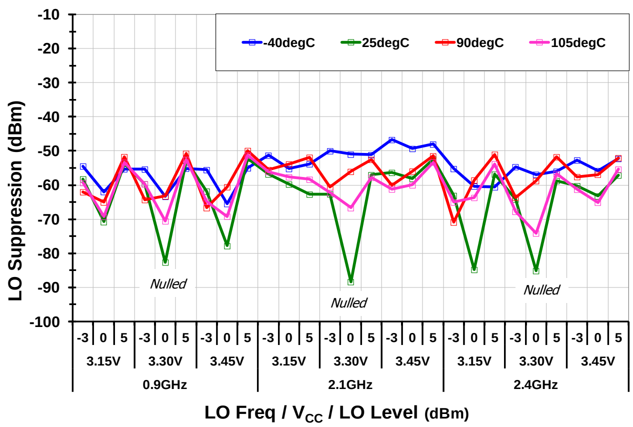
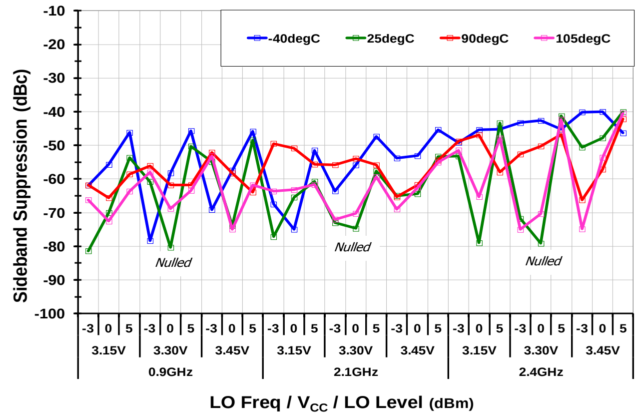
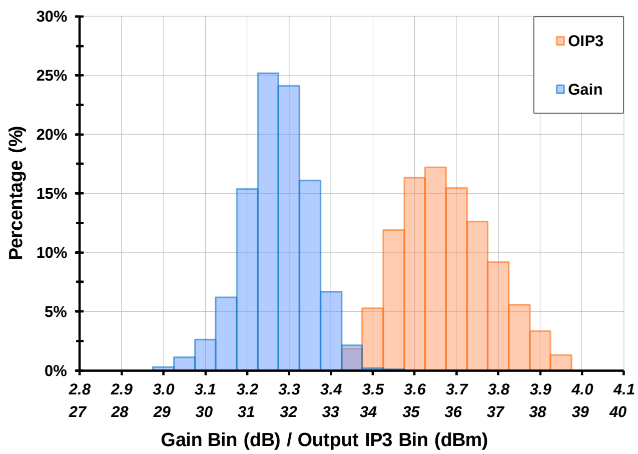


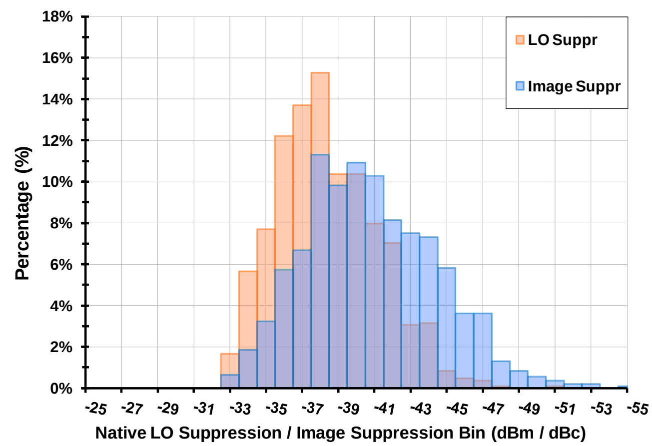
Image (Sideband) Nulling



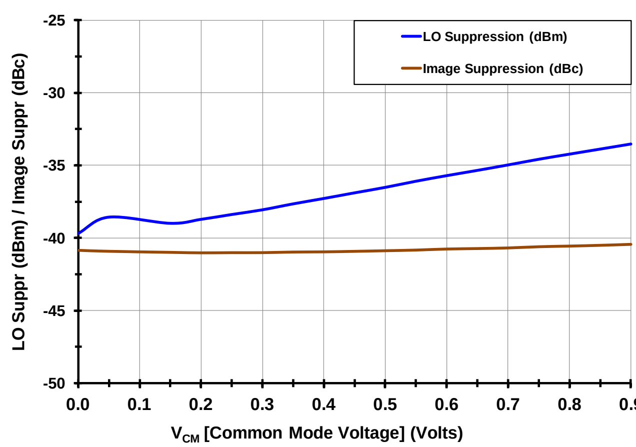
Gain & IP3O Histograms [F_{LO} = 1.95G, N = 1080]



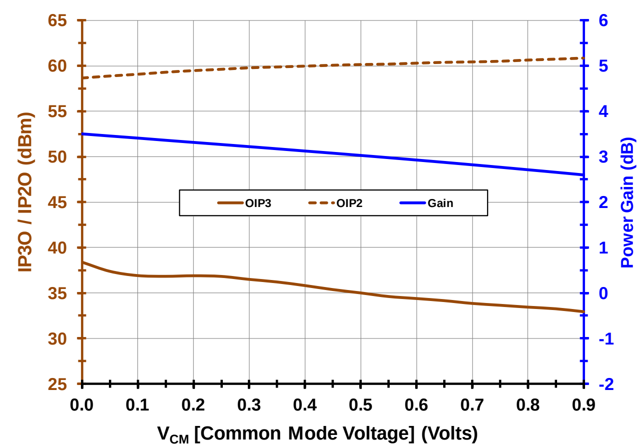
LO & Image Histograms [F_{LO} = 1.95G, N = 1080]



Performance vs. V_{CM} [Native LO & Image Suppression]

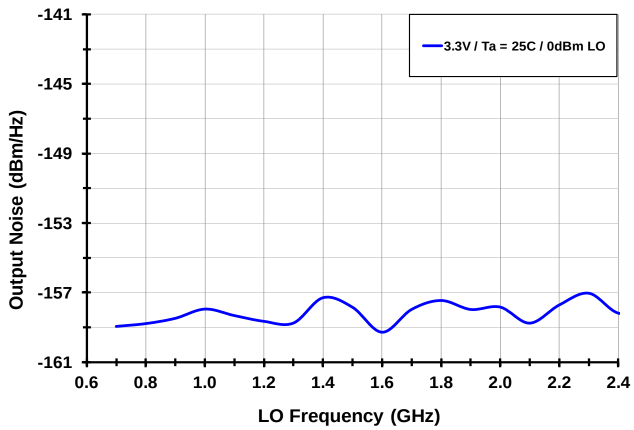


Performance vs. V_{CM} [Gain, IP3, IP2, F_{LO} = 1.95G]

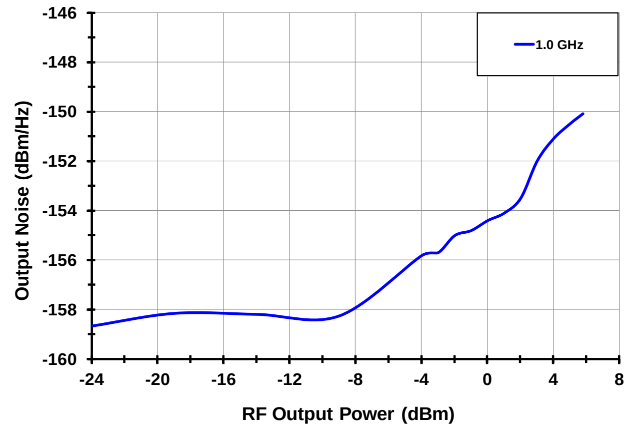


TYPICAL OPERATING CURVES (-7-)

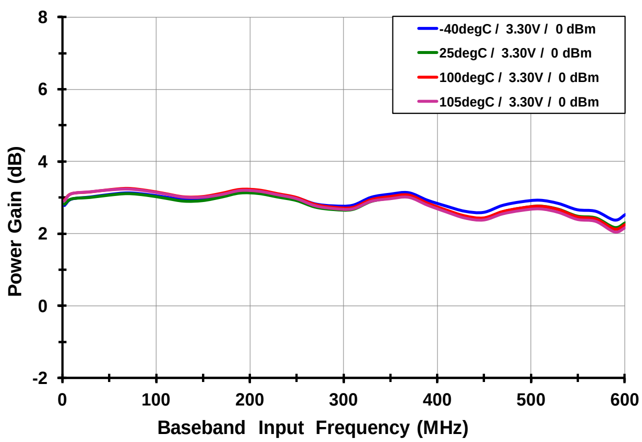
Output Noise vs. Frequency



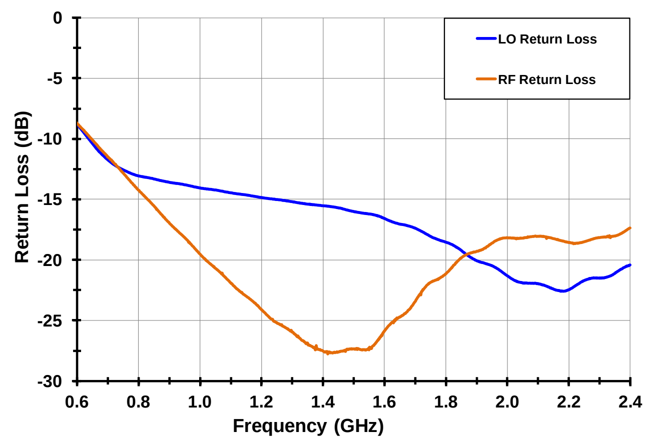
Output Noise vs. P_{OUT} [V_{CC} = 3.3V, T_{AMB} = 25C]



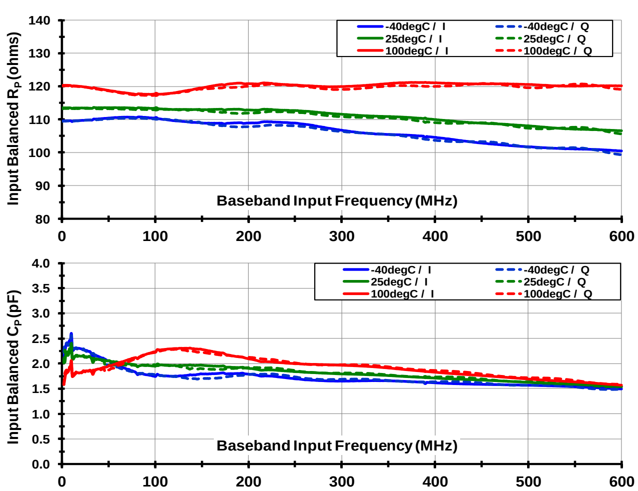
Input Bandwidth (fixed LO = 2.092 GHz)



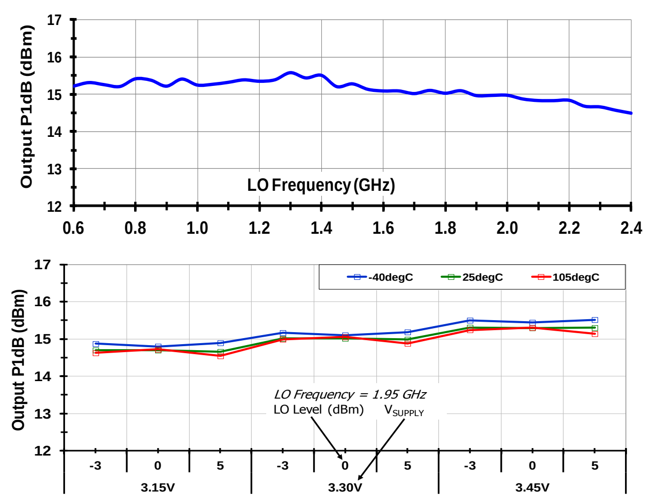
LO & RF Port Return Loss



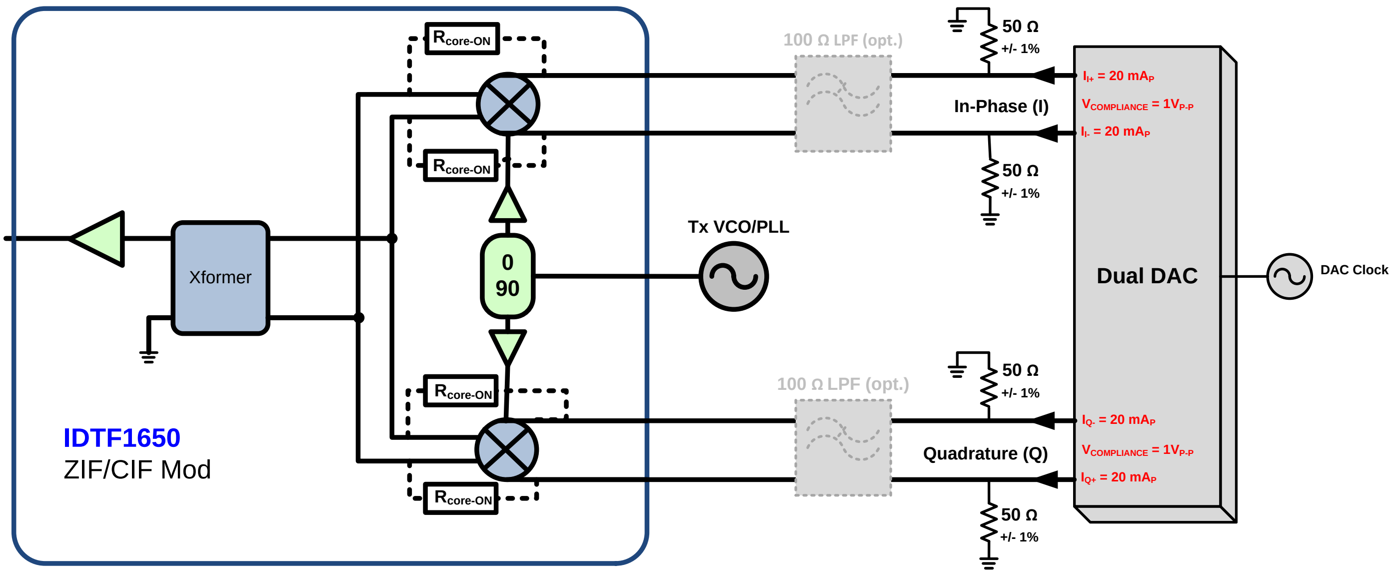
I&Q Input Parallel Resistance/Capacitance



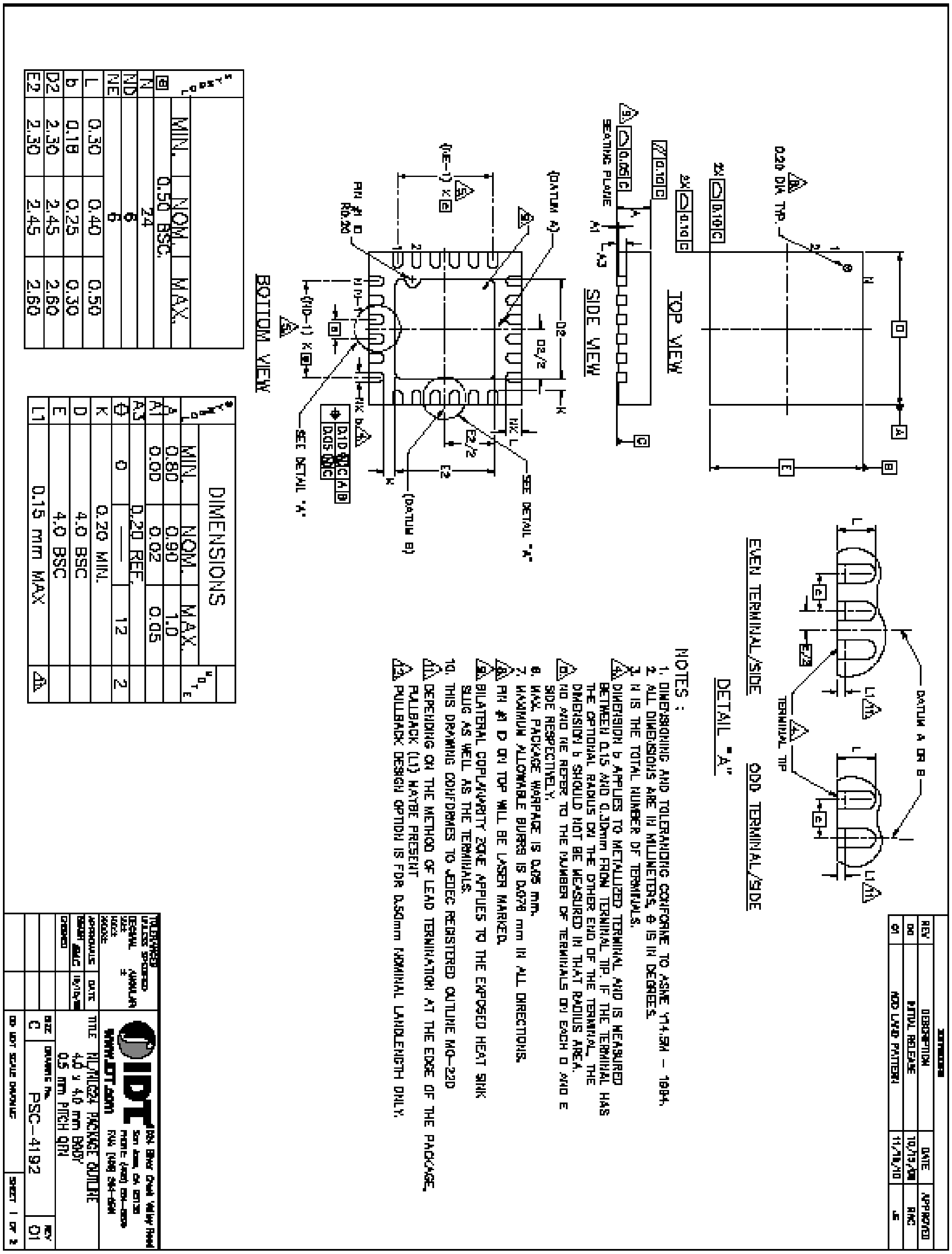
1dB Compression



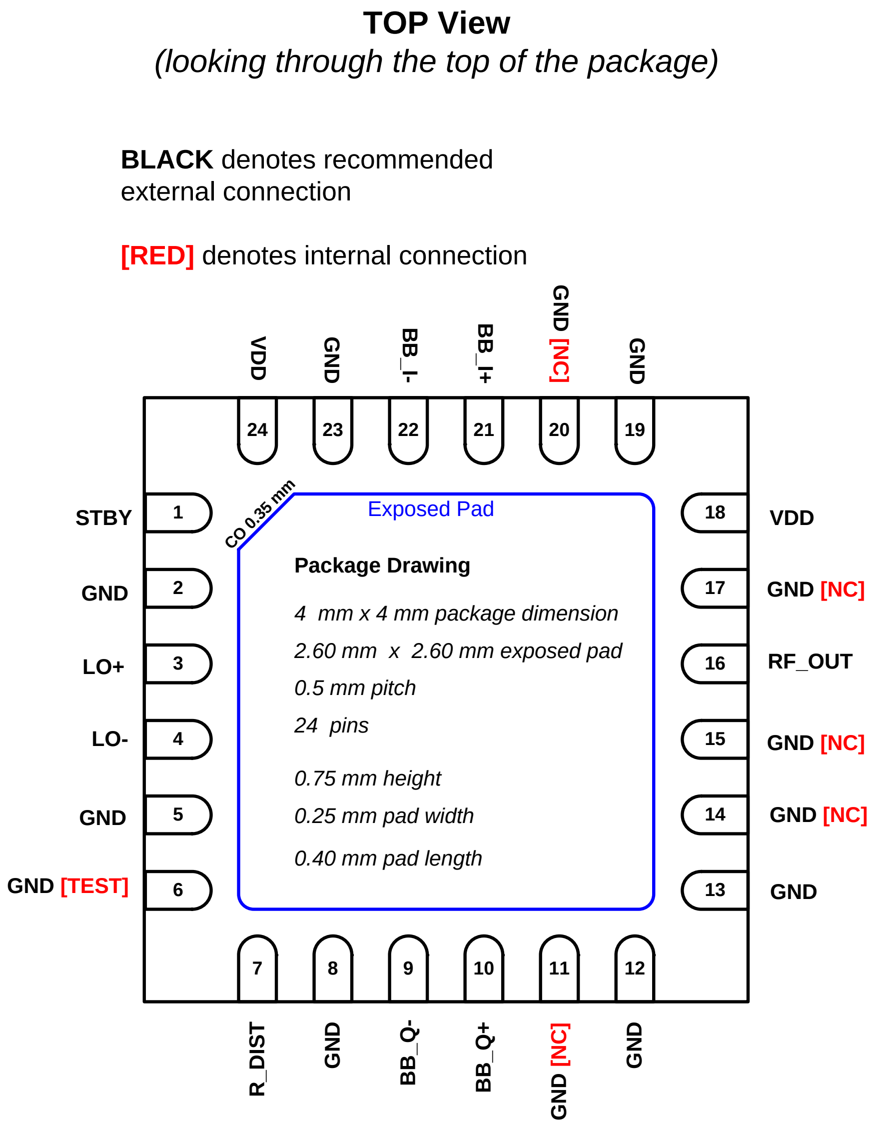
GENERIC DAC INTERFACE



PACKAGE DRAWING (4X4 24 PIN)



PIN DIAGRAM

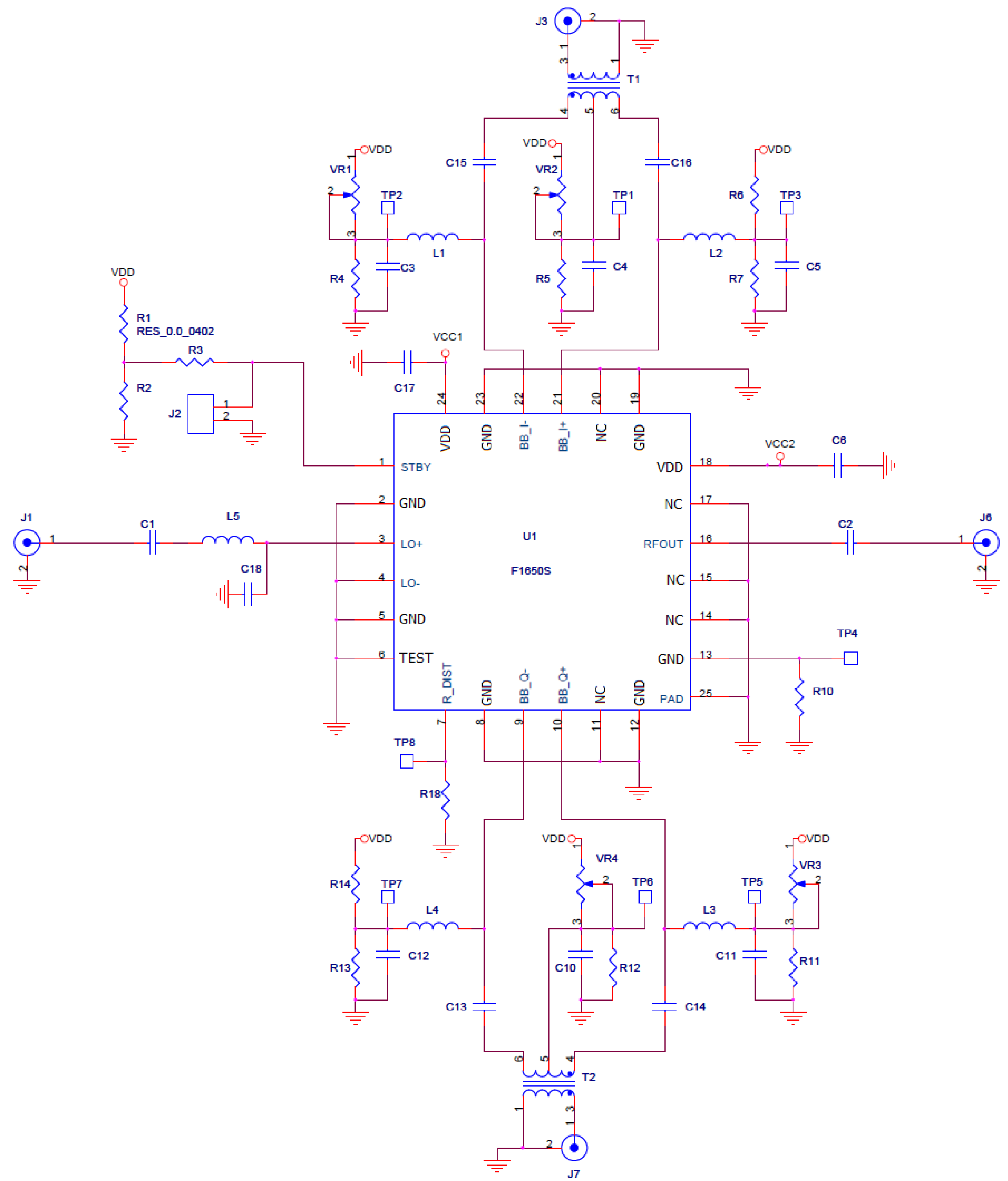


TOP View
(looking through the top of the package)
BLACK denotes recommended external connection
[RED] denotes internal connection
VDD
GND
BB_I-
BB_I+
GND [NC]
GND
24
23
22
21
20
19
STBY
1
GND
2
LO+
3
LO-
4
GND
5
GND [TEST]
6
CO 0.35 mm
Exposed Pad
Package Drawing
4 mm x 4 mm package dimension
2.60 mm x 2.60 mm exposed pad
0.5 mm pitch
24 pins
0.75 mm height
0.25 mm pad width
0.40 mm pad length
18
VDD
17
GND [NC]
16
RF_OUT
15
GND [NC]
14
GND [NC]
13
GND
7
8
9
10
11
12
R_DIST
GND
BB_Q-
BB_Q+
GND [NC]
GND

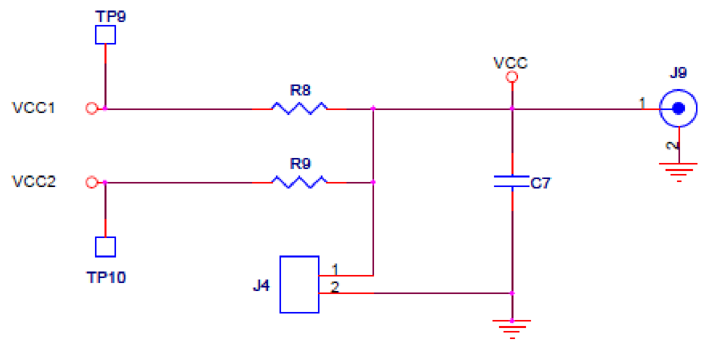
PIN DESCRIPTIONS

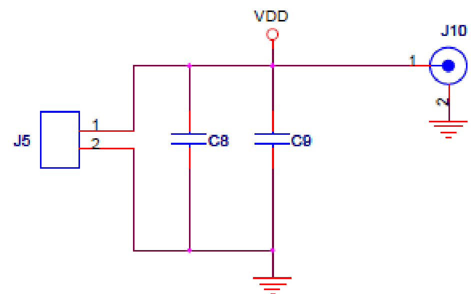
Pins	Name	Function
1	STBY	STBY Mode. Pull this pin high for Standby Mode (<15 mA). Pull low or ground for Normal Operation.
2, 5, 8, 12, 13, 19, 23	GND	Ground these pins.
11, 14, 15, 17, 20	NC	IDT recommends to ground these pins.
3, 4	LO+, LO-	Local oscillator (LO) 50 ohm differential or 25ohm each pin single-ended input. Pins should be ac-coupled. For 50 ohm single-ended operation, ac-couple USED Pin to 50 ohm termination and ac-couple UNUSED pin to GND.
6	TEST	Test pin. Ground this pin.
7	R_DIST	Connect the specified resistor from this pin to ground to set the RF distortion amplifier current.
9, 10	BB_Q-, BB_Q+	*Quadrature* differential baseband input. Internally matched to 100 ohms.
16	RF_OUT	RF output. Must be ac-coupled.
18, 24	VDD	Power Supply. Bypass to GND with capacitors as shown in the Typical Application Circuit as close to pin as possible.
21, 22	BB_I+, BB_I-	*In-Phase* differential baseband input. Internally matched to100 ohms.
	— EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the specified RF performance.

EVKIT SCHEMATIC



EVKIT SCHEMATIC (CONTINUED)





POWER SUPPLIES

All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20uS. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.

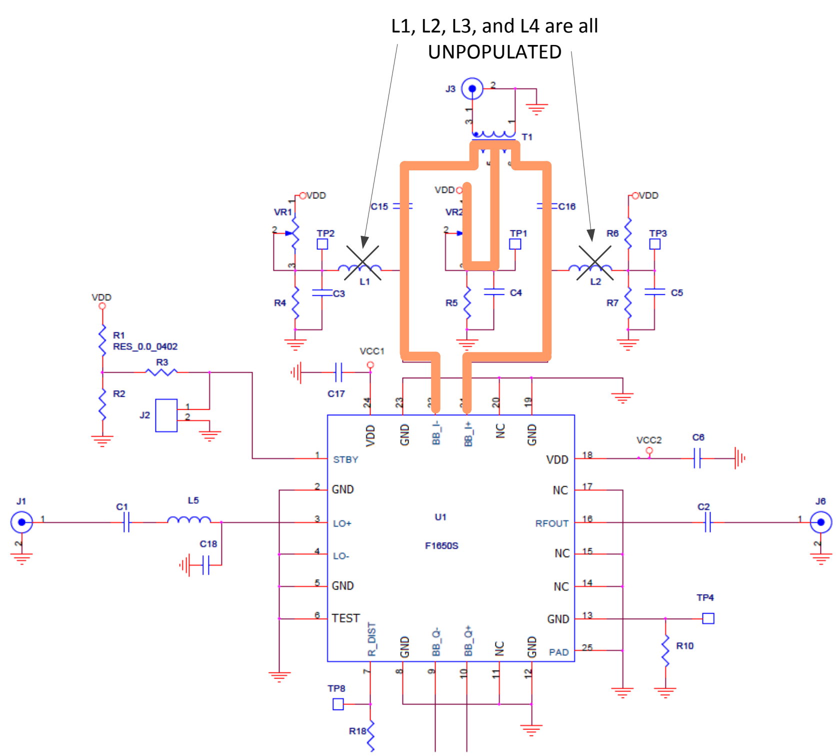
EVKIT BOM

F1650 SE
10/21/2013

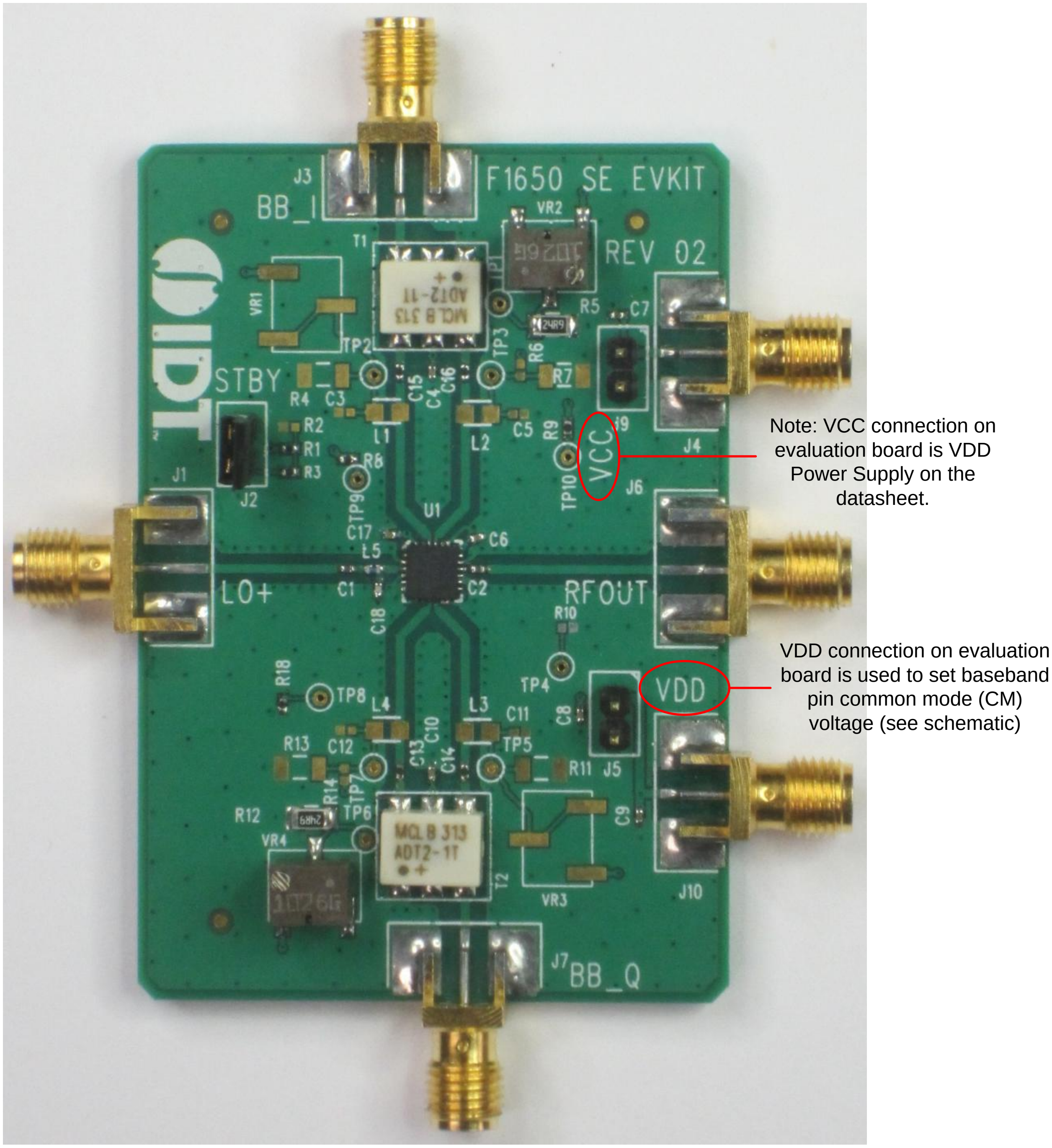
Item #	Value	Size/Rev	Desc	Mfr. Part #	Mfr.	Supplier Part #	Supplier	Part Reference	Qty
1	8pF	0402	CAP CER 8pF 0402 50V 5% C0G	GRM1555C1H8R0DZ01D	MURATA	490-3212-1-ND	Digikey	C2	1
2	10nF	0402	CAP CER 10000PF 16V 10% X7R 0402	GRM155R71C103KA01D	MURATA	490-1313-1-ND	Digikey	C4,6,8,10,17	5
3	39pF	0402	CAP CER 39PF 50V 5% C0G 0402	GRM1555C1H390JZ010	MURATA	490-1286-1-ND	Digikey	C1	1
4	0.6pF	0402	CAP CER 8pF 0402 50V 5% C0G	GJM1555C1HR60BB01D	MURATA	490-6078-1-ND	Digikey	C18	1
5	0.1uF	0402	CAP CER 0.1UF 16V 10% X7R 0402	GRM155R71C104KA88D	MURATA	490-3261-1-ND	Digikey	C7,9	2
6	0	0402	RES 0.0 OHM 1/10W 0402 SMD	ERJ-2GE0R00X	Panasonic	P0.0JCT-ND	Digikey	R3,8,9,C13-16	7
7	6.34K	0402	RES 6.34K OHM 1/10W 1% 0402 SMD	ERJ-2RKF6341X	Panasonic	P6.34KLCT-ND	Digikey	R18	1
8	24.9	1206	RES TF 24.9 OHM 1% 0.25W 1206	RMCF1206FT24R9CT-ND	RMCF	RMCF1206FT24R	Digikey	R5,12	2
9	47K	0402	RES 47.0K OHM 1/16W 1% 0402 SMD	RC0402FR-0747KL	Yageo	311-47.0KLRCT-	Digikey	R1	1
10	1K	2719	TRIMMER 1K OHM 0.25W SMD	TS63Y-1.0KCT-ND	Vishay/Sfernice	TS63Y102KR10	Digikey	VR2,4	2
11	1.8n	0402	0402CS Ceramic Chip Inductor	0402CS-1N8XJLU	CoilCraft	0402CS-1N8XJLU	CoilCraft	L5	1
12	Header 2 Pin	TH 2	CONN HEADER VERT SGL 2POS GOLD	961102-6404-AR	3M	3M9447-ND	Digikey	J2,5,8,9	4
13	SMA_END_LAUNCH	.062	SMA_END_LAUNCH (Small)	142-0711-821	Emerson Johnson	530-142-0711-821	Mouser	J3,4,7,10	4
14	SMA_END_LAUNCH	.062	SMA_END_LAUNCH (Big)	142-0701-851	Emerson Johnson	530-142-0701-851	Mouser	J1,6	2
15	2:1 Balun	SM-22	2:1 Center Tap Balun	ADT2-1T+	Mini Circuits	ADT2-1T+	Mini Circuits	T1,2	2
16	F1650	QFN-24	IQ MOD	F1650	IDT	F1650-010	IDT	U1	1
17	PCB	02	Printed Circuit Board	F1650 SE EVKIT REV 02	Coastal Circuits				1
18	BOM	05	Bill Of Material						
19	DNP	2719						VR1,3	
20	DNP	0402						C3,5,11,12	
21	DNP	0402						R2,6,10,14,16	
22	DNP	1206						R4,7,11,13	
								TOTAL	**38**

APPLYING V_{CM} AT THE BASEBAND INPUTS

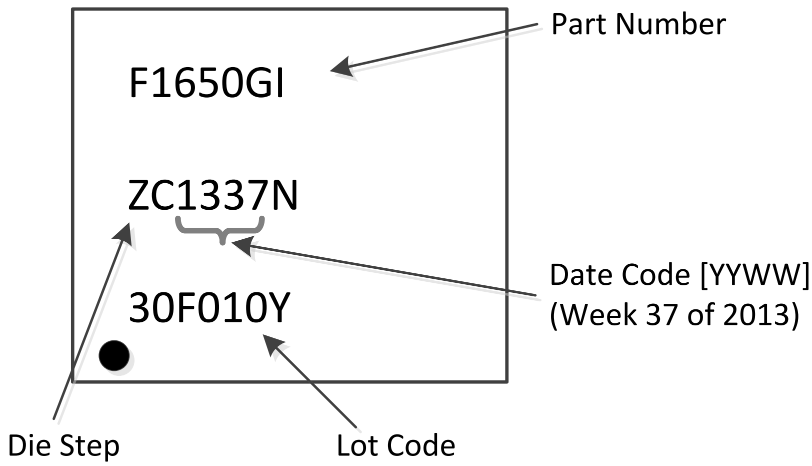
With L1, L2, L3, and L4 unpopulated, the common mode voltage is set by VR2 and VR4. The voltage set by VR2 has a DC path through the balun transformer T1 to pins BB_I+ and BB_I-, as highlighted. This also applies for VR4, T2, and pins BB_Q+ and BB_Q-. With this configuration, the same voltage will be applied to BB_I+ and BB_I- and the same voltage will be applied to BB_Q+ and BB_Q-. The I and Q common mode voltages may be different from each other to null LO (carrier) leakage.



EVKIT PICTURE:



TOP MARKINGS



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