

AXP517P Single Cell NVDC BMU with E-gauge

1 Features

- 3.9V–15V Input Operating Range and Support single Cell Battery
- Battery fuel gauge: E-gauge 3.5
- Support TWSI(Two Wire Serial Interface)
- High efficiency 5A buck mode switch charger
- Boost mode operation with adjustable output from 4.5V to 5.5V
- Integrate control to switch between charger and boost mode
- BATFET control to support shipping mode, wake up and full system reset
- High integration includes all MOSFETS, current sensing and loop compensation
- Support RTCLDO always on, 1.8/2.5/3.0/3.3V for customization
- Support BC1.2, CC logic
- Integrate PD PHY, support PD3.0 except Fast Role Swap function and Extended Message
- ADC for input voltage/ input current/ battery voltage/ battery current/ temperature
- Integrate MPPT (Maximum Power Point Tracking) algorithm
- Protection
 - Input Over-Voltage Protection
 - Battery Thermistor Sense Hot/Cold Charge Suspend
 - Programmable Safety Timer for Charger
 - Die Thermal Balance for Charger
 - Internal temperature sensor and protection

2 Applications

- Tablets, E-ink
- IPC
- Rechargeable portable devices

3 Description

AXP517P is a highly integrated BMU with NVDC power path management and E-gauge for single cell Li-battery. AXP517P can be used with other PMU together to provide an easy and flexible power management solution for SOC. AXP517P also can be used independently to provide battery management solutions for various portable devices.

AXP517P supports high output current up to 5A for fast charging. Besides, AXP517P supports OTG mode. To ensure the security and stability of the system, AXP517P provides multiple channels ADC for voltage/ current/ temperature monitor and integrates protection circuits such as over-voltage protection (OVP), over-current protection (OCP) and over-temperature protection (OTP). Moreover, AXP517P features an unique E-Gauge™(Fuel Gauge) system, making power gauge easy and exact.

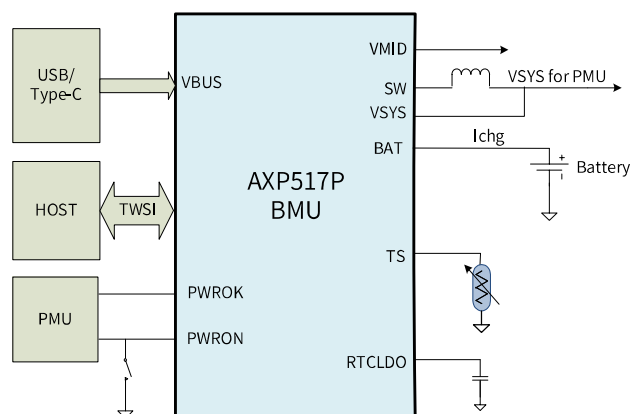
AXP517P supports BC1.2, CC logic and PD protocol. It can automatically detect different adapters and adjust the input current limit.

AXP517P supports TWSI for system to dynamically adjust output voltages, charge current and configure interrupt condition.

Device Information

Part Number	Package	Body Size
AXP517P	QFN-40	5mm * 5mm

Simplified Application Diagram



Revision History

Revision	Date	Author	Description
0.1	Jun. 18, 2026	AWA 1017	Draft

Draft

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4 Pin Configuration and Functions

Figure 4-1 Pin Map

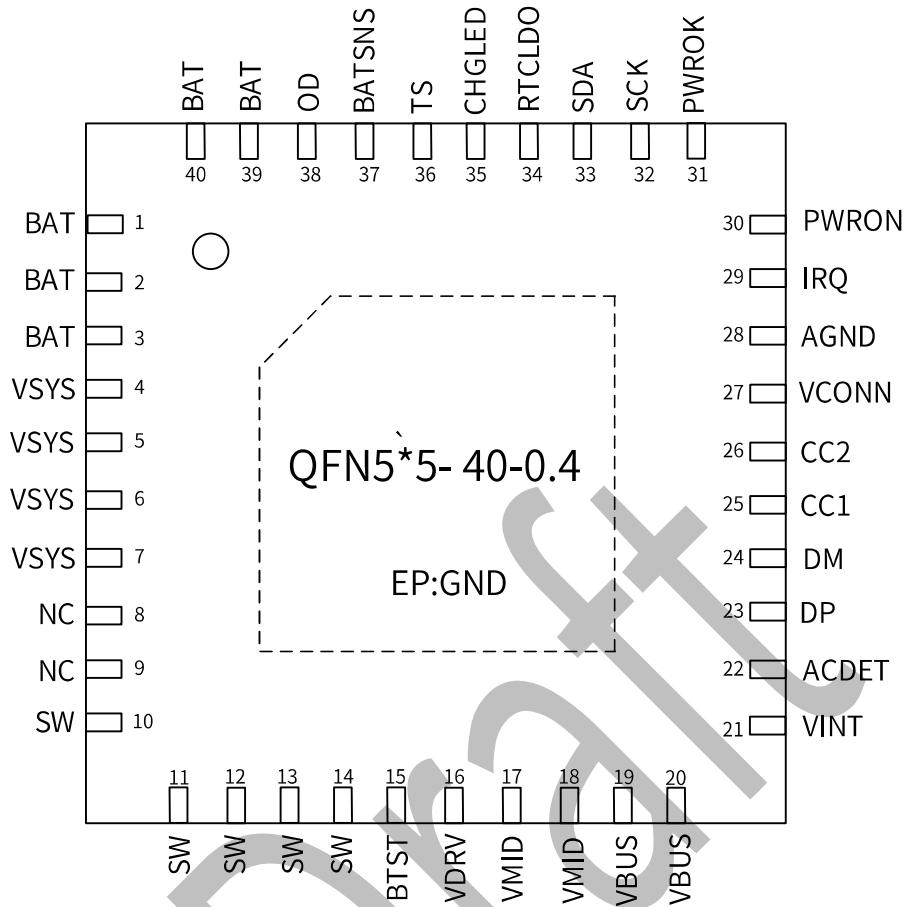


Table 4-1 Pin Description

NO.	Pin Name	I/O ⁽¹⁾	Description
1/2/3/39/40	BAT	P	Battery connection point. The internal BATFET is connected between BAT and VSYS. Connect a 10uF capacitor closely to the BAT pin.
4/5/6/7	VSYS	P	System connection point.
8/9	NC	/	Floating.
10/11/12/13/14	SW	P	Switching node connecting to output inductor.
15	BTST	P	Bootstrap power supply pin. Connect a 47nF capacitor between BTST and SW.
16	VDRV	P	Internal LDO output.
17/18	VMID	P	Boost mode output.
19/20	VBUS	P	Charger Input.
21	VINT	P	Internal power supply, external 1uF capacitor.
22	ACDET	AI	Input sense pin for the PD, can be configured as MPPT-HW-EN input through reg11H[4].
23	DP	DIO	Positive line of the USB data line pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2.

24	DM	DIO	Negative line of the USB data line pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2.
25	CC1	DIO	Type-C connector configuration channel pin.
26	CC2	DIO	Type-C connector configuration channel pin.
27	VCONN	P	PD Phy input source pin.
28	AGND	G	Analog GND.
29	IRQ	DIO	Open-drain interrupt Output. Connect a pull-up resistor.
30	PWRON	DI	BATFET enabled/BMU reset control input. Connect a key between PWRON and GND. Internal pulled up.
31	PWROK	DI	Indication of system power ON/OFF status. It can be connected to PWROK pin of PMU or directly pulled up to above 1.8V.
32	SCK	DI	Clock pin for serial interface.
33	SDA	DIO	Data pin for serial interface.
34	RTCLDO	P	LDO output. It is used to provide power for RTC and so on.
35	CHGLED	DO	Charge status output to indicate various charger operation.
36	TS	AI	Battery Temperature Sensor Input. Connect a negative temperature coefficient thermistor between TS and GND.
37	BATSNS	AI	BAT ADC input
38	OD	DO	GPO, open drain output

(1)O for output, I for input, IO for input/output, D for digital, A for analog, P for power, and G for ground.

5 Specifications

5.1 Absolute Maximum Ratings ⁽¹⁾

Over operating free-air temperature range (unless otherwise noted)

Table 5-1 Absolute Maximum Ratings

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
VBUS	Voltage range(with respect to GND)	-0.3	25	V
ACDET		-0.3	35	V
SW, VMID		-0.3	25	V
BTST-SW		-0.3	6	V
BAT,VSYS		-0.3	7	V
SDA,SCK,IRQ,RTCLDO, TS,PWRON,PWROK,DP,DM, CHGLED,BATSNS, OD,NC		-0.3	7	V
CC1,CC2		-0.3	25	V
VCONN,VDRV		-0.3	7	V
VINT		-0.3	2.2	V
PGND to GND		-0.3	0.3	V
Ta	Operating Temperature Range	-40	85	°C
TJ	Junction Temperature Range	-40	150	°C
Ts	Storage Temperature Range	-65	150	°C
TLEAD	Maximum Soldering Temperature (at leads, 10sec)		300	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

Table 5-2 ESD Ratings

		VALUE	UNIT
V _{ESD}	Human body model(HBM) ⁽¹⁾	±2000	V
	Charged device model(CDM) ⁽²⁾	±750	V

(1) Reference: ESDA/JEDEC JS-001-2024.

(2) Reference: ESDA/JEDEC JS-002-2025.

5.3 Recommended Operating Conditions

Table 5-3 Recommended Operating Conditions

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
VIN	Input voltage(VBUS)	3.9	15	V
IIN	Input current(VBUS)		3.25	A
ISYS	Output current		5	A
VBAT	Battery voltage		4.4	V
IBAT	Fast charging current		5	A

5.4 Thermal Information

Table 5-4 Thermal Information

Thermal Metric ⁽¹⁾		VALUE	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	44.43	°C/W
θ_{JB}	Junction-to-board thermal resistance	21.23	
θ_{JC}	Junction-to-case(top) thermal resistance	3.75	

(1) Thermal metrics are calculated refer to JEDEC document JESD51. The values are based on simulation.

5.5 Electrical Characteristics

T_A=25°C

Table 5-5 Electrical Characteristics

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I _{BAT}	Battery discharge current	no VBUS, BATFET Disabled, Gauge low power mode		25		uA
I _{VBUS}	Input supply current (VBUS) in buck mode	VBUS = 5/9V, BAT = 3.8V, converter switching, BATFET Disabled, I _{sys} = 0A, TCPC disabled (pwrok=0)		2		mA
VBUS/BAT POWER UP						
V _{VBUS_OP}	VBUS operating range		3.9		15	V
V _{VBUS_UVLOZ}	VBUS under voltage threshold		3.4		3.9	V
V _{SLEEP}	Sleep mode falling threshold			90		mV
V _{SLEEPZ}	Sleep mode rising threshold			150		mV
V _{BAT_UVLOZ}	Battery for active TWSI, no VBUS		2.2	2.4	2.6	V
RTCLDO						
V _{RTCLDO}	Output Voltage	I _{RTC_VCC} =1mA		1.8		V
I _{RTCLDO}	Output Current			30		mA
POWER-PATH MANAGEMENT						
V _{sys}	Typical system regulation voltage	I _{sys} = 0A, V _{BAT} > V _{sys_min} , BATFET Disabled		V _{BAT} + 50mV		V
		I _{sys} = 0A, V _{BAT} < V _{sys_min} , BATFET Disabled		V _{sys_min} + 150mV		V
V _{sys_min}	Minimum DC System Voltage Output	V _{BAT} < V _{sys_min} , V _{sys_min} = 3.5V, I _{sys} = 0A		3.65		V
V _{sys_max}	Maximum DC System Voltage Output	V _{BAT} = 4.25V, V _{sys_min} = 3.5V, I _{sys} = 0A		4.3		V
V _{FWD}	BATFET forward voltage in supplement mode	BATFET forward voltage in supplement mode		30		mV
Battery Charger						
V _{BATREG_RANGE}	Typical Charge voltage range			4.208		V
V _{BATREG}	Charge voltage resolution accuracy	V _{BAT} = 4.2V (REG64[2-0]=010) or V _{BAT} = 4.35V (REG64[2-0]=011)	-0.5%		0.5%	
I _{CHG_REG_RANGE}	Typical Fast charge current regulation range		0		5120	mA

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	UNIT
I _{CHG_REG_STEP}	Typical Fast charge current regulation step			64		mA
I _{CHG_REG_ACC}	Fast charge current regulation accuracy	V _{BAT} = 3.7V, I _{CHG} =512mA	-40%		40%	
		V _{BAT} = 3.7V, I _{CHG} =1536mA	-15%		15%	
		V _{BAT} = 3.7V, I _{CHG} =3072mA	-15%		15%	
V _{BATLOWV}	Battery LOWV falling threshold	Fast charge to precharge	2.5	2.9	3.1	V
	Battery LOWV rising threshold	Precharge to fast charge	2.7	3.0	3.3	V
I _{PRECHG_RANGE}	Precharge current range		0		960	mA
I _{PRECHG_STEP}	Typical precharge current step			64		mA
I _{PRECHG_ACC}	Precharge current accuracy	V _{BAT} =2.6V, I _{PRECHG} = 256mA	-40%		40%	
I _{TERM_RANGE}	Termination current range		0		960	mA
I _{TERM_ACC}	Termination current accuracy	V _{BAT} =4.2V, I _{TERM} = 256mA	-40%		40%	
I _{TERM_STEP}	Typical Termination current step			64		mA
V _{SHORT}	Battery short voltage(Trickle charge)	V _{BAT} falling		2		V
V _{RECHG}	Recharge Threshold below V _{BATREG}	V _{BAT} falling, V _{RECHG}		100		mV
R _{ON(BATFET)}	SYS-BAT MOSFET (BATFET) on-resistance(pin to pin)			20		mΩ
Input Voltage / Current Regulation						
V _{INDPM_RANGE}	Typical Input voltage regulation range		3.9		15	V
V _{INDPM_STEP}	Typical Input voltage regulation step			100		mV
V _{INDPM_ACC}	Input voltage regulation accuracy	V _{INDPM} =4.2V or 15V	-3%		3%	
I _{INDPM_RANGE}	Typical Input current regulation range		100		3250	mA
I _{INDPM_STEP}	Typical Input current regulation step			50		mA
BAT OVER-VOLTAGE/CURRENT PROTECTION						
V _{BATOV}	Battery over-voltage threshold	V _{BAT} rising, as percentage of V _{BAT_REG}		104%*		V
V _{BATOV_HYST}	Battery over-voltage hysteresis	V _{BAT} falling, as percentage of V _{BAT_REG}		2%		V
THERMAL REGULATION AND THERMAL SHUTDOWN						
T _{REG}	Junction temperature regulation accuracy	REG65[1-0] = 10		100		°C
T _{SHUT}	Thermal Shutdown Rising Temperature	Temperature rising		145		°C

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	UNIT
T _{SHUT_HYS}	Thermal Shutdown Hysteresis	Temperature falling		25		°C
Boost Mode Operation						
V _{BST_REG_RANGE}	Typical Boost mode regulation voltage range		4.55		5.51	V
V _{BST_REG_STEP}	Typical Boost Mode Regulation voltage step			64		mV
JEITA Thermistor Comparator(buck mode)						
T1	T1 threshold, charge suspended below this temperature, Vt1 rising	Set by REG54,default 0°C @NTC 10K,B=3423K		0°C		°C
V _{t1 falling}	Vt1 falling	Set by REG52				
T2	T2 threshold, charge back to Ichg/2 and 4.2V, below this temperature, Vt2 rising	Set by REG5A,default 10°C @NTC 10K,B=3423K		10°C		°C
T3	T3 threshold, charge back to Ichg and 4.05V, below this temperature, Vt3 falling	Set by REG5B,default 45°C @NTC 10K,B=3423K		45°C		°C
T4	T4 threshold, charge suspended below this temperature, Vt4 falling	Set by REG55,default 55°C @NTC 10K,B=3423K		60°C		°C
V _{t4 rising}	Vt4 rising	Set by REG53				
Logic I/O pin Characteristics (IRQ/PWRON/PWROK)						
V _{IH}	Input high threshold level			1.3		V
V _{IL}	Input low threshold level			0.4		V
I _{IN_BIAS}	High Level Leakage Current	Pull-up rail 1.8V		1		uA
TWSI INTERFACE (SCK, SDA)						
VCC	Input Supply Voltage			1.8/3.3		V
ADDRESS	TWSI Slave Address (7 bits)			0x34		
f _{SCK}	Clock Operating Frequency		100		400	kHz
V _{IH}	Input high threshold level, SCK and SDA	Pull-up rail 1.8V		1.3		V
V _{IL}	Input low threshold level	Pull-up rail 1.8V		0.4		V
V _{OL}	Output low threshold level	Sink Current = 5mA, sink current		0.4		V
CC logic						
V _{RDB_DEF}	Pull-down Voltage in Dead Battery Mode with Source	Source Default Rp is 80μA±20%	0.25		1.5	V

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	UNIT
	Default Rp					
V _{RDB_1.5A}	Pull-down Voltage in Dead Battery Mode with Source 1.5A Rp	Source Default Rp is 180μA±8%	0.45		1.5	V
V _{RDB_3A}	Pull-down Voltage in Dead Battery Mode with Source 3A Rp	Source Default Rp is 330μA±8%	0.85		2.5	V
Rd	Rd in Active Mode	CC is configured as Rd	4.6	5.1	5.6	KΩ
V _{Rd_Snk}	Attach Detection Threshold in Sink Mode	With Rp is connected externally, CC is configured as Rd	0.25		2.04	V
I _{RP_DEF}	Default Pull up current source in Source Mode	CC is configured as Default Rp	64	80	96	μA
I _{RP_1P5}	1.5A Pull up current source in Source Mode	CC is configured as 1.5A Rp	166	180	194	μA
I _{RP_3P0}	3A Pull up current source in Source Mode	CC is configured as 3A Rp	304	330	356	μA
V _{Rd_Src}	Attach Detection Threshold in Source Mode	With Rd is connected externally, CC is configured as Default Rp	0.25		1.5	V
		With Rd is connected externally, CC is configured as 1.5A Rp	0.45		1.5	V
		With Rd is connected externally, CC is configured as 3A Rp	0.85		2.45	V
VCONN Source Control						
R _{VCN}	VCONN FET Conduction Resistance			1		Ω
V _{VCN_PR5}	VCONN Present Threshold		2		2.4	V
CC Detection(VBUS)						
VBUS_PR5_F	VBUS Present Threshold	Assert VBUS_PRESENT bit		3.2		V
V _{Safe0V}	VBUS vSave0V	To trigger VBUS_80 interruption		0.8		V

6 Detail Description

6.1 Overview

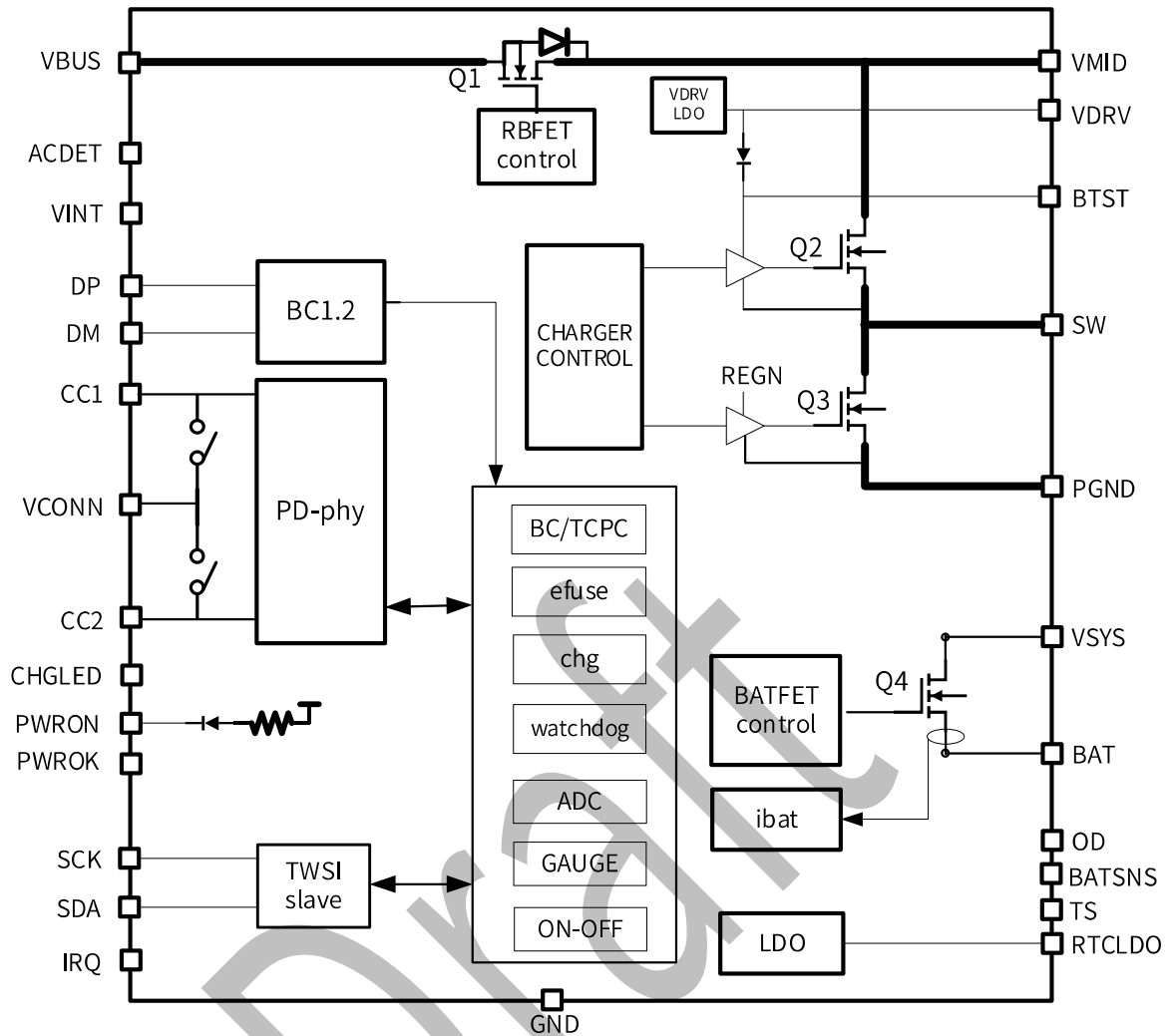
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AXP517P supports BC1.2, CC logic and PD protocol. It can automatically detect different adapters and adjust the input current limit.

AXP517P supports TWSI for system to dynamically adjust output voltages, charge current and configure interrupt condition.

6.2 Function Block Diagram



6.3 TWSI Communication

AXP517P supports TWSI protocol and performs as a TWSI slave device with default address 0x34(7 bits). When AXP517P powers on, SCK/SDA pin of TWSI will be pulled up to external IO Power and then Host can adjust and monitor AXP517P with rich feedback information.

Note: “Host” here refers to processor.

Figure 6-1 Waveform of TWSI

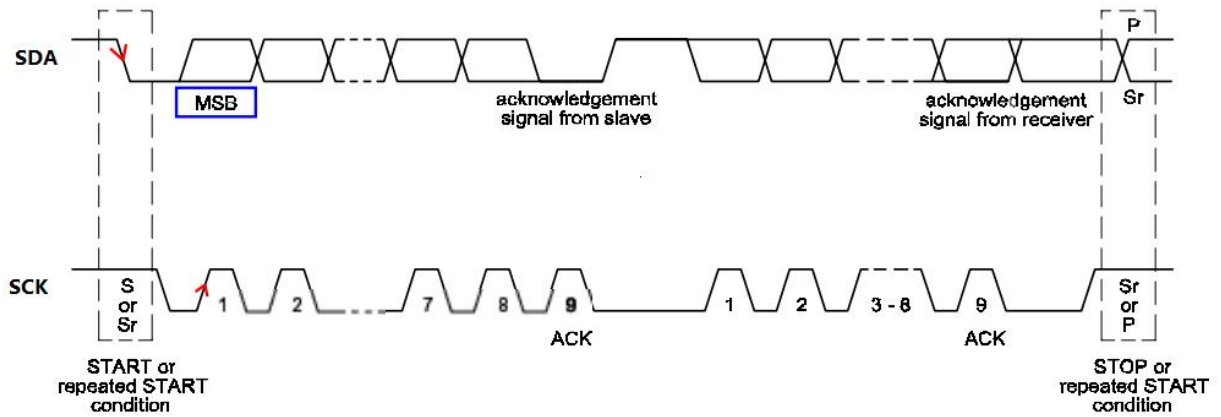


Table 6-1 Read and write address of TWSI

BYTE	BIT							
	MSB	6	5	4	3	2	1	0
WRITE	0	1	1	0	1	0	0	0
READ	0	1	1	0	1	0	0	1

Figure 6-2 Timing of TWSI

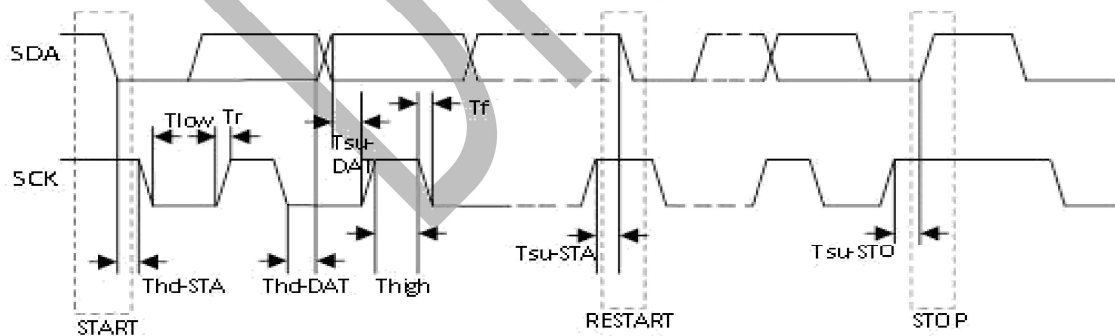


Table 6-2 Timing constants

Parameter	Symbol	Standard mode			Fast mode			Unit
		MIN	TYP	MAX	MIN	TYP	MAX	
SCK clock frequency	Fsck	0	-	100	0	-	400	kHz
Setup time in START	Tsu-STA	4.7	-	-	0.6	-	-	us
Hold time in START	Thd-STA	4.0	-	-	0.6	-	-	us
Setup time in Data	Tsu-DAT	250	-	-	100	-	-	ns
Hold time in Data	Thd-DAT	0	-	-	0	-	0.9	us
Setup time in STOP	Tsu-STO	4.0	-	-	0.6	-	-	us
SCK low level time	Tlow	4.7	-	-	1.3	-	-	us
SCK high level time	Thigh	4.0	-	-	0.6	-	-	us

Parameter	Symbol	Standard mode			Fast mode			Unit
		MIN	TYP	MAX	MIN	TYP	MAX	
SDA/SCK falling time	Tf	-	-	300	20	-	300	ns
SDA/SCK rising time	Tr	-	-	1000	20	-	300	ns

6.4 NVDC

AXP517P uses Narrow VDC(NVDC) architecture with BATFET connecting system and battery.

VBUS as the charger input, connecting to VSYS pin through a switch mode buck charger, provides power to system and charges battery through BATFET. Charge current can be adjusted automatically according to the feedback current which is detected through BATFET. When system current(I_{SYS}) changes, the detected current will change, and then the current change signal will feed back to charge loop to adjust the charge current to the setting value.

AXP517P starts up when an adapter is inserted and the input voltage meets the condition. System voltage(V_{SYS}) will rise up to minimum system voltage(V_{SYS_min}). If V_{SYS} does not reach V_{SYS_min} , the charging process does not start up. V_{SYS_min} can be configured by reg15H[4:0]. When V_{SYS} is higher than V_{SYS_min} , charger enabled signal will be sent.

When it is charging, if battery voltage is lower than V_{SYS_min} , BATFET operates in linear mode(LDO mode) to keep V_{SYS} at $V_{SYS_min}+150mV$. As battery voltage rises above V_{SYS_min} , BATFET is fully on.

When battery voltage is higher than V_{SYS} , BATFET is turned on and BMU enters supplement mode. When in supplement mode, if the discharge current is lower than 2A, BMU controls the voltage(V_{DS}) between system and battery and keeps V_{DS} at about 30mV to avoid entering and exiting supplement mode repeatedly. As discharge current increases, BMU adjusts BATFET to be fully on and V_{DS} increases linearly. If an adapter is not inserted, system current is provided only by battery. At this time, BATFET is at fully on state.

6.5 Power On/Off and reset

6.5.1 Power on reset (POR)

AXP517P is powered from the higher voltage between VBUS and BAT. When VBUS voltage(V_{VBUS}) is higher than V_{VBUS_UVLOZ} or BAT voltage(V_{BAT}) is higher than V_{BAT_UVLOZ} , AXP517P will be power on reset and all registers are reset to the default value. TWSI communication is active and Host can communicate with BMU.

6.5.2 Power up from BAT

If only battery is present and V_{BAT} is higher than V_{BAT_UVLOZ} , BATFET, connecting battery to system, is off by default and need to be turned on by power on sources.

6.5.3 Power up from VBUS

When VBUS is inserted, BMU detects the input voltage to start up the VDRV LDO, the reference voltage and the bias circuit. When V_{VBUS} is higher than V_{VBUS_UVLOZ} , the VBUS insertion IRQ is sent. Then BMU detects the input source whether it is good or not. When VBUS is good and BC1.2/ Type C detection is enabled, BMU detects the input source type and set the input current limit(I_{INLIM}) automatically, and then the buck converter starts up.

6.5.3.1 VDRV LDO

VDRV LDO is the power supply for the internal circuit and MOSFETs. The startup of VDRV LDO requires the following conditions.

1. In buck mode, VBUS voltage(V_{VBUS}) is higher than V_{VBUS_UVLOZ} and BAT voltage(V_{BAT}), and lower than 17.5V(typical).
2. In boost mode, VDRV LDO is enabled automatically.

6.5.3.2 Good source detection

BMU needs to detect the current capability of the input source. Only when the input source meets the following requirements can it start the buck converter.

1. VBUS voltage lower than V_{ACOV}
2. VBUS voltage higher than V_{VBUS_UVLOZ} when pulling I_{BADBUS} (typical 20mA)

Once the input source meets the requirements above, the register bit `reg00H[5](VBUS_GOOD)` is set to 1 to indicate the input source is good. If the input source does not meet the requirements, detection will be done repeatedly every 2 seconds.

6.5.3.3 Input source type detection

AXP517P integrates USB Charging Specification 1.2(BC1.2) and Type C(cc logic) detection. The type and the power supply capability of the input source can be detected and I_{INLIM} (`reg17H[7:0]`) can be set automatically.

After the VBUS_GOOD bit is set to 1 and the VDRV LDO starts up, if BC1.2 or Type C detection is enabled, BMU starts input source type detection automatically. BC1.2 detection and Type C detection are independent and they work in parallel, but the detection result of Type C has higher priority level than that of BC1.2. When the two kinds of detection are both under way, if Type C detection finishes first and I_{INLIM} is set, I_{INLIM} can not be changed by the BC1.2 detection result. However, if BC1.2 detection finishes first and I_{INLIM} is set, I_{INLIM} can be changed by the Type C detection result.

6.5.3.4 Input voltage limit(V_{INDPM})

AXP517P supports wide range of input voltage. V_{INDPM} can be set through `reg16H[6:0]`. The range of V_{INDPM} is from 3.9V to 16.2V and the step is 100mV. The default value can be customized.

When VBUS voltage reaches V_{INDPM} , the buck output current and the charge current will decrease automatically. When the charge current decreases to zero and the power supply is still not enough, V_{SYS} will drop to below V_{BAT} , and BMU will enter the supplement mode.

6.5.3.5 Input current limit(I_{INLIM})

AXP517P integrates current limit protection. I_{INLIM} can be set through `reg17H[7:0]`. The range of I_{INLIM} is from 100mA to 3250mA and the step is 50mA.

When VBUS input current is over the set value of I_{INLIM} , the buck output current and the charge current will decrease automatically. When the charge current decreases to zero and the power supply is still not enough, V_{SYS} will drop to below V_{BAT} , and BMU will enter the supplement mode.

6.5.3.6 Buck converter start up

After the input source is detected good, the buck converter is enabled. If BATFET is in off state, the buck converter powers V_{SYS} only, otherwise the buck converter charges the battery at the same time.

AXP517P integrates soft-start function. When V_{SYS} is lower than 2.2V, I_{INLIM} is forced to be the lower one between 200mA and I_{INLIM} register value. When V_{SYS} is higher than 2.2V, I_{INLIM} is set through register value. The working condition of buck converter can switch between PWM and PFM automatically according to the load.

6.5.3.7 Power off

When VBUS is removed, BMU disables the charger, VDRV LDO and RBFET. The system is supplied by the battery. If the start-up conditions are meet, the associated circuits are enabled again.

When the die is over temperature, BMU disables the buck converter, boost mode and BATFET.

6.5.3.8 Reset

AXP517P has power on reset and system reset.

1. Power on reset(POR)

There are four ways of power on reset.

- VBUS or battery inserts and the voltage meets the start-up conditions.
- PWRON key is low for longer than 16s. The function is configured by reg18H[1].
- Soft POR. Write “1” to reg18H [0].
- Watchdog timeout and reg1AH[5-4]=11.

2. System reset

System reset method just resets some associated registers. There are two ways of system reset.

- PWROK drive low. When the system status bit(reg01H[4]) is set to 0, BMU implements system reset.
- Watchdog timeout and reg1AH[5-4]=01/10. The function is disabled by default.

6.6 Charger

6.6.1 Characteristics

- Range of input voltage:3.9V~15V, PWM charger, supports single cell Li-battery
- High charge efficiency in fast charging mode:93%@2A, 91%@3A, 89%@5A
- Pre-charge current settable($I_{PRE-CHG}$, reg61H[3-0]), default:128mA, range: 0mA~960mA,64mA/step
- Fast charge current settable(I_{CHG} , reg62H[6-0]), default:1024mA, range: 0mA~5120mA,64mA/step
- Termination current settable(I_{TERM} , reg63H[3-0]), default:320mA, range: 0mA~960mA,64mA/step
- Target charge voltage settable(V_{TERM} , reg64H[6-0]), default:4.208V, range:3.44V~5.024V, 16mV/step
- Accuracy of target voltage: $\pm 0.5\%$ (testing ambient temperature:25°C,target voltage:4.208V)

6.6.2 Charging condition

- VBUS is present and available, $V_{VBUS} > V_{BAT} + V_{SLEEPZ}$
- Input source detection finishes (reg00H[5] =1)
- Charging is enabled (reg19H[1] =1)
- VDRV LDO is OK
- Die temperature is lower than T_{SHUT}
- When TS pin is used to detect battery temperature, battery temperature is within the chargeable range
- V_{BAT} is lower than V_{BAT_OVP} and Battery is present
- No charger safety timer fault
- BATFET is not forced to be off (BATFET_DIS bit, reg12H[2]=0)

6.6.3 Charging process

When BMU meets all charging conditions, it can complete the whole charging process without the participation of Host. The charging status can be known from the register bits reg01H[2-0]. The default values of charging parameters are shown as following. Host can modify registers to optimize the values through TWSI.

Table 6-3 Default values of charging parameters

Parameter	Default value
Charging voltage	4.208V
Charging current	1.024A
Pre-charging current	128mA
Termination current	320mA
Temperature profile	Cold/hot
Safety timer in fast-charge	12hours

6.6.3.1 Trickle-charge

When V_{BAT} is lower than 2V, the charger is under trickle-charge mode where charging current is limited to a value of $I_{TRI-CHG}$. $I_{TRI-CHG}$ can be set through reg61H[6-4] and the default value is 128mA.

6.6.3.2 Pre-charge

When V_{BAT} is lower than $V_{BATLOWV}$ (3V), the charger is under pre-charge mode where charging current is limited to a value of $I_{PRE-CHG}$. Safety time in pre-charge is 60 minutes by default(reg67H[1-0]). If pre-charge process times out, BMU will stop charging and send a corresponding IRQ to Host. The function of safety timer can be disabled through reg67H[2].

6.6.3.3 Constant current charge

Once V_{BAT} is higher than $V_{BATLOWV}$ (3V) and lower than V_{TERM} , the charger is under constant current charge mode. It will charge with constant current I_{CHG} . Safety time in cc-charge is 12 hours by default(reg67H[5-4]). If cc-charge process times out, BMU will stop charging and send a corresponding IRQ to Host. The function of safety timer can be disabled through reg67H[6].

6.6.3.4 Constant voltage charge

When V_{BAT} reaches target voltage (V_{TERM}), the charger enters constant voltage charge mode. In this stage, the charger keeps the output voltage constant and step down charging current gradually, in order to fully charge battery.

When V_{BAT} reaches V_{TERM} and the charging current reduces under termination current (I_{TERM}), AXP517P reports charger done, stops charging (charger enabled bit is remains 1) and turns off BATFET. Meanwhile, IRQ is sent to Host.

When AXP517P is in regulation of input current (IDPM), input voltage(VDPM) or temperature(thermal regulation), the function of charging termination is temporarily disabled and the speed of safety timer slows down. Whether to set safety timer during DPM or thermal regulation depends on reg67H[7].

The function of charging termination is configured by reg63H[4].

6.6.3.5 Re-charge

After charging is complete and the adapter is present, if V_{BAT} falls below V_{RECHG} , BMU will automatically enable charger.

6.6.3.6 Battery detection

As long as an adapter is present and usable, battery detection will be enabled to detect whether battery is connected. Battery detection function is enabled by default and can be disabled through reg68H[0]. If the function is disabled, BMU considers that battery is always present. The detection result is saved in reg00H[3].

6.6.4 Charging protection

6.6.4.1 charger safety timer

Once starting pre-charge mode, BMU will enable timer1, which function is configured through reg67H[2]. If BMU cannot enter constant current charge mode from pre-charge within 60 minutes(default), BMU will enter battery safe mode and send IRQ to indicate the battery may be damaged.

When the charger enters into constant current charge mode, BMU will enable timer2, which function is configured through reg67H[6]. If BMU cannot finish the whole charge cycle within 12 hours, BMU will enter battery safe mode and send IRQ to indicate the battery may be damaged.

6.6.4.2 Battery safe mode

In battery safe mode, the charger always charges with 10mA current. BMU can quit battery safe mode with one of the following methods:

- $V_{BAT} > V_{RECHG}$
- Adapter removal
- Charger enabled bit (reg19H[1]) is re-enabled to 1
- Safety timer1 enabled bit(reg67H[2]) or safety timer2 enabled bit(reg67H[6]) is re-enabled to 1

6.6.4.3 Die temperature protection

AXP517P has built-in temperature protection function through ADC to monitor internal temperature.

Under charging mode, the temperature point of thermal regulation can be set through reg65H[1:0]. When die temperature rises up to the setting point, the charging current will be decreased to decrease heat. When thermal regulation works, actual charge current is lower than the setting value and thermal regulation status(reg00H[1]) is set to 1. If the die temperature rises up to T_{SHUT} (145°C), the buck converter and BATFET will be disabled. When the die temperature falls below hysteretic threshold (120°C), the charger will be recovered.

6.6.4.4 Battery temperature protection

AXP517P can monitor battery temperature, when TS pin is used to detect battery temperature and affect the charger (reg50H[4]=0). The battery temperature sensitive resistor is connected between TS pin and GND. The suggestion resistance should be 10Kohm at 25°C ambient temperature. Through TS pin, BMU outputs constant current which can be set through reg50H[1:0] to adapt different resistance. When the resistance is 10Kohm, the current should be set to 50uA. The enabled bit of TS current source is configured through reg50H[3:2]. When current passes through the temperature sensitive resistor, BMU gets a detected voltage and calculates its value through ADC circuit. Take for example, TH11-3H103F temperature sensitive resistor of Mitsubishi Company. Using 50uA current source, the relationship among temperature, equivalent resistance, detected voltage and ADC data is as following.

Table 6-4 Relationship among temperature, equivalent resistance, detected voltage and ADC data

Temperature	equivalent resistance	detected voltage	ADC DATA
-20°C	63.00Kohm	3.150V	189Ch
-15°C	50.15Kohm	2.508V	1398h
-10°C	40.26Kohm	2.013V	FBAh
-5°C	32.55Kohm	1.628V	CB8h
0°C	26.49Kohm	1.325V	A5Ah
5°C	21.68Kohm	1.084V	878h
10°C	17.78Kohm	0.889V	6F2h

15°C	14.63Kohm	0.732V	5B8h
20°C	12.07Kohm	0.604V	4B8h
25°C	10.00Kohm	0.500V	3E8h
30°C	8.320Kohm	0.416V	340h
35°C	6.954Kohm	0.348V	2B8h
40°C	5.839Kohm	0.292V	248h
45°C	4.924Kohm	0.246V	1ECh
50°C	4.171Kohm	0.209V	1A2h
55°C	3.549Kohm	0.177V	162h
60°C	3.032Kohm	0.152V	130h

During battery charging process, if TS pin voltage is lower than VH_{TF}-CHG or higher than VL_{TF}-CHG (VH_{TF}-CHG and VL_{TF}-CHG can be set through reg55H and reg54H). The default value of VL_{TF}-CHG is set around 0°C and VH_{TF}-CHG around 55°C), which indicates battery temperature is too high or too low, then the charger is paused and IRQ is sent to notify Host. When battery temperature is back to the normal range, the charger will recovery automatically.

During BOOST mode, if TS pin voltage is lower than VH_{TF}-WORK or higher than VL_{TF}-WORK (VH_{TF}-WORK and VL_{TF}-WORK can be set through reg57H and reg56H. The default value of VL_{TF}-WORK is set around -10°C and VH_{TF}-WORK around 60°C), which indicates battery temperature is too high or too low, then the boost is paused and IRQ is sent to notify Host. When battery temperature is back to the normal range, the boost will recovery automatically.

High temperature protection threshold hysteresis for VH_{TF}-CHG and VH_{TF}-WORK can be set through reg53H. Low temperature protection threshold hysteresis for VL_{TF}-CHG and VL_{TF}-WORK can be set through reg52H.

Some battery may have no temperature sensitive resistor. Under this situation, TS pin can be pulled down to GND with a 10Kohm resistor externally, or configure a fixed TS voltage through reg5CH/5DH or set as external input of ADC through register reg50H[4].

6.6.4.5 JEITA standard

AXP517P integrated flexible configuration for JEITA standard. JEITA function is set enabled through reg58H[0]. T1, T2, T3 and T4 are set through reg54H, reg5AH, reg5BH and reg55H respectively.

In cool range, the V_{TERM} can be set to be 100mV or 200mV lower than the normal value through reg59H[1-0] and the charging current can be set to be 100% or 50% or 25% of the normal value through reg59H[5-4].

In warm range, the V_{TERM} can be set to be 100mV or 200mV lower than the normal value through reg59H[3-2] and the charging current can be set to be 100% or 50% or 25% of the normal value through reg59H[7-6].

No matter in cool range or warm range, when the set value of charging current is lower than 256mA, the charging current remains unchanged. when the set value of charging current is higher than 256mA, the charging current can be decreased but not lower than 256mA.

Table 6-5 The actual V_{TERM} In warm/cool range

Set value V_{TERM} (V)	The actual V_{TERM} for 100mV lower(V)	The actual V_{TERM} for 200mV lower(V)
4.4	4.3	4.2
4.35	4.25	4.15
4.2	4.1	4.0

6.6.5 Charging indication

CHGLED pin uses open-drain/push-pull output method. Its output drive capability is above 10mA. Detail function control is shown as the following table.

Table 6-6 CHGLED function

reg30H[2:0] = 000 (Type A CHGLED)	Hi-Z	No charging(conditions are not met or battery charge done)
	25% 1Hz pull low/Hi-Z jump	Charger fault(including timer out、die temperature over level1、 battery temperature out of charging range)
	25% 4Hz pull low/Hi-Z jump	Input source or battery over voltage
	Pull low	Charging
reg30H[2:0] = 001 (Type B CHGLED)	Hi-Z	No VBUS, and power supplied by battery
	25% 1Hz pull low/Hi-Z jump	Charging
	25% 4Hz pull low/Hi-Z jump	Fault, including input source or battery over voltage, battery temperature out of charging range, timer out ,die temperature over level1
	Pull low	No battery or charge done, and power supplied by VBUS
reg30H[2:0]=010 Breathing LED	Hi-Z	No VBUS, and power supplied by battery
	Breath LED output(*Note)	Charging
	Pull low	VBUS present and no charging
reg30H[2:0]=011 Breathing LED	Breathing LED controlled by reg30H[6] and reg32H~reg38H	
reg30H[2:0]=110 CFG CHGLED	The output status is controlled by reg30H[5:3]	

Note: LED is on when CHGLED pin is low.

6.7 BOOST

AXP517P supports boost converter operation to deliver battery power to VBUS or VMID. If below conditions are valid, boost will be enabled.

1. VBAT is higher than boost mode disable threshold (REG1EH[3:2], default is 3.0V)
2. VBUS voltage is lower than $V_{BAT} + V_{SLEEP}$
3. Boost mode is enabled (REG19H[4]=1)
4. Voltage at TS pin is within working range (REG56H/57H)
5. The die temperature is lower than T_{SHUT}

In boost mode, the output voltage can be set through reg1EH[7:4]. The switch frequency of boost converter is 1.5MHz which can not be changed.

AXP517P integrates OVP function in boost mode. When over voltage occurs, boost converter will be turned off and IRQ will be sent to Host.

When charging conditions are met, boost converter will be disabled and then charger will be enabled.

6.8 BATFET

6.8.1 BATFET off sources

In order to increase the life of battery and reduce consumption during transportation, system is allowed to turn off BATFET. When BMU is supplied by only battery, V_{SYS} is 0 after BATFET is turned off, which can make the leakage current minimum.

There are some ways to turn off BATFET. Reg00H[4] indicates BATFET status.

Normal sources:

- Write “1” to reg12H[2]. Force BATFET off.
- Write “1” to reg12H[3]. This way is valid when AXP517P is power supplied only by battery. The bit is cleared to 0 automatically.
- Charge done.
- VBUS present but charger disabled(reg19H[1]=0) and not in supplement mode.
- PWRON key is low level for longer than OFFLEVEL(reg1CH[3-2]). The function is configured by reg1CH[7].

Abnormal sources:

- Battery over voltage
- No VBUS and V_{BAT} is lower than V_{BAT_UVLOZ}
- The die temperature is higher than T_{SHUT}
- Charger safety timer fault

6.8.2 BATFET on sources

BATFET can be enabled with the following methods.

- A charger inserts and charging conditions are met, but if fault cases exist, BATFET is not enabled.
- Reg12H[2] is set from 1 to 0.
- Write “1” to reg12H[0]. Force BATFET on.
- PWRON key is low level for longer than ONLEVEL(reg1CH[1-0]).
- IRQ Low level. IRQ pin is low level for more than 4ms. The function is configured by reg1CH[6].

6.9 RBFET

RBFET connects VMID and VBUS. It supports input current limit function. The input current limit value is set through reg17H[7:0].

6.10 ADC

AXP517P integrates a high precision ADC for measuring BAT voltage, VBUS voltage, VSYS voltage, TS voltage, VBUS current, die temperature and battery current.

Table 6-7 ADC channel

No.	Channel function	0000H	0001H	0002H	...	Bit(including sign bit)
1	TS	0mV	0.5mV	1mV	...	14
2	DIE temperature	0mV	0.2mV	0.4mV	...	14
3	VBUS voltage	0mV	2mV	4mV	...	14
4	VBAT voltage	0mV	1mV	2mV	...	14
5	charge current	0mA	0.25mA	0.5mA	...	16
6	dischg current	0mA	0.25mA	0.5mA	...	16
7	VBUS current	0mA	1mA	2mA	...	14
8	VSYS	0mV	1mV	2mV	...	14

Note: In order to get the complete data, TWSI must read the high bits firstly and then the low bits.

Conversion formula:

$$T_{die} = (3552 - ADC) / 1.79 + 25$$

$$I_{dischg} = (ADC - 2^{16}) * 0.25$$

6.11 E-Gauge

The Fuel Gauge system is able to export information about battery capacity percentage (reg74H). The Fuel Gauge can be enabled or disabled through reg0BH[2]. The Battery low warning level can be set through reg1BH, and IRQ will be sent out to alert the platform when the battery capacity percentage is lower than the warning level set through reg1BH.

Once a default battery is selected for a particular design, it is highly recommended to program the battery module to achieve better Fuel Gauge accuracy. Once the battery module data are available, user can write these information to battery parameter (reg70H) after brom is enabled. Additionally, the Fuel Gauge system is capable to learn the battery characteristic automatically.

6.12 MPPT algorithm

AXP517P supports solar charge and integrates Maximum Power Point Tracking algorithm. When ACDET is configured as MPPT-HW-EN input reg11H[4]=1, and the input is high level, and reg22H[0]=1, MPPTEN_STAT(reg22H[1]) will be 1 and MPPT is enabled.

6.13 PD

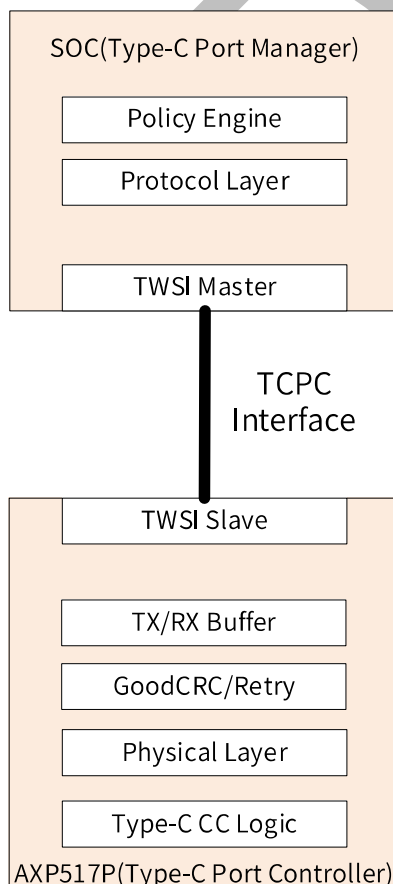
AXP517P integrates PD PHY and supports PD3.0 except Fast Role Swap function and Extended Message.

AXP517P has programmable Rp and Rd settings for each CC line. It does the USB type-C detection including attach and orientation. AXP517P integrates a complete BMC encoding including a receiver and a transmitter.

When the device needs to send information, the protocol layer of the processor constructs the sent message and encodes it according to the rules agreed upon by the chip, and then sends it to the chip's transmit FIFO through TWSI, but the processor also needs to start the chip to send the information.

Please refer to regA6H~regDCH for the detail configuration.

Figure 6-3 System Block Diagram of PD Application



6.14 Watchdog

When wd_clk_en(reg0BH[0]) and wd_en(reg19H[0]) are both set to 1, watchdog function is enabled. The time can be set through reg1AH[2-0]. The timer can be cleared by writing “1” to reg1AH[3]. There are four modes for watchdog timeout and refer to reg1AH[5-4].

6.15 Pin function

6.15.1 IRQ

AXP517P has an IRQ pin which is used to indicate whether there interrupt events occur. The IRQ pin is open-drain and needs to be pulled up externally.

BMU Interrupt Controller monitors the trigger events such as over voltage, PWRON pin signal, over temperature and so on. When the events occur and their IRQ enabled bits are set to 1 (Refer to registers reg40H~44H/ regB2H~B3H), corresponding IRQ status will be set to 1 (Refer to registers reg48H~4CH/ regB0H~B1H), and IRQ pin will be pulled down. When the IRQ signal is detected, Host will scan through the IRQ Status registers and respond accordingly. Meanwhile, Host will reset the IRQ status by writing “1” to the status bit.

6.15.2 GPIO

AXP517P features a GPI and a GPO.

The ACDET pin is an input sense pin for the PD module by default. It can be set as MPPT-HW-EN input via reg11H[4]. When the ACDET pin is configured as MPPT-HW-EN input, if its input is low level, MPPT is disabled. If its input is high level and reg22H[0]=1, MPPT is enabled.

The GPO supports open-drain output mode exclusively and its configuration is controlled by reg11H[7-6].

6.16 Register

6.16.1 Register List

Address	Description	R/W
0X00	BMU status0	R
0X01	BMU status1	R
0X04	Data Buffer0	RW
0X05	BC_detect	R
0X06	BMU fault0	R
0X08	BMU fault1	R
0X0B	Module enable control0	RW
0X0C	Data Buffer1	RW
0X0D	Data Buffer2	RW
0X10	Common configure	RW
0X11	GPIO configure	RW
0X12	BATFET control	RW
0X13	RBFET control	RW
0X14	Die temperature configure	RW
0X15	Minimum system voltage control	RW
0X16	Input voltage limit control	RW
0X17	Input current limit control	RW
0X18	Reset configure	RW
0X19	Module enable control1	RW
0X1A	Watchdog control	RW
0X1B	Low Battery warning threshold setting	RW

Address	Description	R/W
0X1C	PWRON configure	RW
0X1D	VBUS_OV/CHG_PWRON configure	RW
0X1E	Boost configure	RW
0X22	MPPT configure	RW
0X28	BC1.2 control0	RW
0X29	BC1.2 control1	RW
0X2A	BC1.2 control2	RW
0X2B	BC1.2 control3	RW
0X30	CHGLED configure	RW
0X32	Breath LED control0	RW
0X33	Breath LED control1	RW
0X34	Breath LED control2	RW
0X36	Breath LED control3	RW
0X37	Breath LED control4	RW
0X38	Breath LED control5	RW
0X40-0X43	IRQ Enable	RW
0X48-0X4B	IRQ Status	RW
0X50	TS pin configure	RW
0X52	TS_HYSL2H setting	RW
0X53	TS_HYSH2L setting	RW
0X54	VLTF_CHG setting	RW
0X55	VHTF_CHG setting	RW
0X56	VLTF_WORK setting	RW
0X57	VHTF_WORK setting	RW
0X58	JEITA standard Enable control	RW
0x59-0X5B	JEITA standard setting	RW
0X5C-0X5D	TS data configure	RW
0X61	Iprechg/Itrichg setting	RW
0X62	ICC setting	RW
0X63	Iterm setting and control	RW
0X64	CV charger voltage setting	RW
0X65	Thermal regulation threshold setting	RW
0X67	Charger timer configure	RW
0X68	Battery detection control	RW
0X70	Battery parameter	RW
0X71	Fuel gauge control	RW
0X72	Battery temperature	R
0X73	Battery SOH	R
0X74	Battery percentage	R
0X82	TS source select	RW
0X90	ADC Channel enable control	RW
0X91-0X92	BAT voltage ADC data	R
0X93-0X94	BAT current ADC data	R
0X95-0X96	TS voltage ADC data	R
0X97-0X98	VBUS current ADC data	R
0X99-0X9A	VBUS voltage ADC data	R
0X9B	ADC data select	RW
0X9C-0X9D	ADC data	R
0X9E	ADC CONFIG	RW

Address	Description	R/W
0XA6-0XA7	USBTPEC_REV	R
0XA8	USBPD_VER	R
0XA9	USBPD_REV	R
0XAA	PD_INTERFACE_VER	R
0XAB	PD_INTERFACE_REV	R
0XB0-0XB1	PD_ALERT	RW
0XB2-0XB3	PD_ALERT_MASK	RW
0XB4	POWER_STATUS_MASK	RW
0XB5	FAULT_STATUS_MASK	RW
0XB6	EXTENDED_STATUS_MASK	RW
0XB9	TCPC_CONTROL	RW
0XBA	ROLE_CONTROL	RW
0XBB	FAULT_CONTROL	RW
0XBC	POWER_CONTROL	RW
0XBD	CC_STATUS	R
0XBE	POWER_STATUS	R
0XBF	FAULT_STATUS	R
0XC0	EXTENDED_STATUS	R
0XC3	COMMAND	RW
0XC4-0XC7	DEVICE_CAPABILITIES	R
0XCE	MESSAGE_HEADER_INFO	RW
0XCF	RECEIVE_DETECT	RW
0XD0-0XD1	VBUS_VOLTAGE	R
0XD2-0XD3	VBUS_SNK_DISCONNECT_THL	RW
0XD4-0XD5	VBUS_STOP_DISCHARGE_THLD	RW
0XD6-0XD7	VBUS_VLOT_ALM_HI_CFG	RW
0XD8-0XD9	VBUS_VLOT_ALM_LO_CFG	RW
0XDA	RX_BUFFER	R
0XDB	TX_BUF_FRAME_TYPE	RW
0XDC	TX_BUFFER	RW
0XEA	EN_VCONN	RW

6.16.2 Register Description

6.16.2.1 REG 00H: BMU status0

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5	VBUS good indication 0: not good 1: good	RO	POR	0
4	BATFET state 0: off 1: on	RO	POR	0
3	Battery present state 0: absent 1: present	RO	POR	0
2	Battery in Active Mode 0: in Normal 1: in Active Mode	RO	POR	0
1	Thermal regulation status 0: normal 1: in thermal regulation	RO	POR	0
0	Current Limit state 0: not in current limit state 1: in current limit state	RO	POR	0

6.16.2.2 REG 01H: BMU status1

Bit	Description	R/W	Reset	Default
7	Reserved	RO	/	0
6:5	Battery Current Direction 00: Standby 01: charge 10: discharge 11: Reserved	RO	POR	0
4	System status indication 0: System is power off. 1: System is power on.	RO	POR	0
3	VINDPM status 0: not in VINDPM 1: VINDPM	RO	POR	0
2:0	Charging status 000: tri_charge 001: pre_charge 010: constant charge(CC) 011: constant voltage(CV) 100: charge done 101: not charging 11X: Reserved	RO	POR	0

6.16.2.3 REG 04H: Data Buffer0

Bit	Description	R/W	Reset	Default
7-0	Data Buffer	RW	POR	00H

6.16.2.4 REG 05H: BC_detect

Bit	Description	R/W	Reset	Default
7:5	USB BC1.2 Detect result 000: Reserved 001: SDP 010: CDP 011: DCP 1XX: Reserved	RO	POR	000b
4:0	Reserved	RO	/	0

6.16.2.5 REG 06H: BMU fault0

Bit	Description	R/W	Reset	Default
7	Reserved	RO	/	0
6:4	NTC fault status buck mode: 000: normal 001: TS cold 010: TS hot boost mode: 000: normal 101: TS cold 110: TS hot	RO	POR	000b
3:0	Reserved	RO	/	0

6.16.2.6 REG 08H: BMU fault1

Bit	Description	R/W	Reset	Default
7:4	Reserved	RO	/	0
3	VSYS Over Voltage of 5V 0: VSYS < 5V 1: VSYS >= 5V	RW1C	POR	0b
2	VBAT UVLO(2.5V) 0: VBAT >= UVLO(2.5V) 1: VBAT < UVLO(2.5V)	RW1C	POR	0b

1:0	Reserved	RO	/	0
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6.16.2.7 REG 0BH: Module enable control0

Bit	Description	R/W	Reset	Default
7:5	Reserved	RW	/	0
4	BC1.2 detect enable 0:disable 1:enable	RW	POR	EFUSE
3	Type-C CC detect enable 0:disable 1:enable	RW	POR	EFUSE
2	Gauge enable 0:disable 1:enable	RW	POR	1b
1	Reserved	RO	/	0
0	Watchdog enable 0:disable 1:enable	RWAC	POR	0b

6.16.2.8 REG 0CH: Data Buffer1

Bit	Description	R/W	Reset	Default
7-0	Data Buffer	RW	POR	00H

6.16.2.9 REG 0DH: Data Buffer2

Bit	Description	R/W	Reset	Default
7-0	Data Buffer	RW	POR	00H

6.16.2.10 REG 10H: Common configure

Bit	Description	R/W	Reset	Default
7	Reserved	RO	/	0
6	VBUS force discharge enable 0: disable 1: enable	RW	System Reset	0
5	VBUS discharge enable when vbus_uvlo low 0: disable 1: enable	RW	POR	1
4	Internal off-discharge enable for Vsys 0: disable 1: enable	RW	POR	0
3:2	VBUS discharge current select 00: 20mA 01: 10mA 10: 1mA 11: 50uA	RW	System Reset	00b
1	Charge done force SOC of gauge to 100% enable 0: disable 1: enable	RW	POR	1
0	VBUS detect function disable 0: VBUS detect enable. 1: VBUS detect disable(for cooperation with BOOST out of the BMU)	RW	System Reset	0

6.16.2.11 REG 11H: GPIO configure

Bit	Description	R/W	Reset	Default
7	OD function configure	RW	POR	0

	0: floating 1: open drain output			
6	OD output configure 0: hiz 1: low	RW	POR	0
5	Reserved	RO	/	0
4	ACDET function configure 0: Analog input for PD_VBUS sense 1: Digital input for MPPT-HW-EN(GPI)	RW	POR	0
3	Reserved	RO	/	0
2	GPI input status 0: low 1: high	RO	POR	0
1:0	Reserved	RO	/	0

6.16.2.12 REG 12H: BATFET control

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5:4	The delay to close BATFET when reg12H[3]=1 00: 0ms 01: 8ms 10: 16ms 11: 32ms	RW	POR	01b
3	Shipmode enable when Battery only 0: disable shipmode(BATFET enable) 1: enable shipmode(BATFET disable)	RWAC	POR	0
2	Force BATFET disable 0: Normal 1: Force BATFET off	RW	POR	0
1	Reserved	RO	/	0
0	Force BATFET enable 0: Normal 1: Force BATFET on	RW	POR	0

6.16.2.13 REG 13H: RBFET control

Bit	Description	R/W	Reset	Default
7:1	Reserved	RO	/	0
0	Force RBFET enable 0: disable 1: enable	RW	System Reset	0

6.16.2.14 REG 14H: Die temperature configure

Bit	Description	R/W	Reset	Default
7:3	Reserved	RO	/	0
2:1	DIE Over Temperature Protection Level1 configure 00: 115deg 01: 125deg 10: 135deg 11: Reserved	RW	POR	01b
0	DIE Temperature Detection Enable 0: disable 1: enable	RW	POR	1

6.16.2.15 REG 15H: Minimum system voltage control

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4:0	Minimum system voltage limit 1.0+N*0.1 V 00000~10110: Reserved 10111: 3.3V 11000: 3.4V 11001: 3.5V 11010: 3.6V 11011: 3.7V 11100~11111: 3.8	RW	POR	11001b

6.16.2.16 REG 16H: Input voltage limit control

Bit	Description	R/W	Reset	Default
7	Reserved	RO	/	0
6:0	Input voltage limit configuration: 3.6+(N-1)*100mV, N>=1 0000000~0000011: Reserved 0000100: 3.9 0000101: 4.0 0001001: 4.4V	RW	POR	0001001 b

6.16.2.17 REG 17H: Input current limit control

Bit	Description	R/W	Reset	Default
7:2	Input current limit configuration: 100+N*50 mA 000000: 100mA 000001: 150mA 000010: 200mA 111111: 3250mA	RW	POR	EFUSE
1:0	Reserved	RO	/	0

6.16.2.18 REG 18H: Reset configure

Bit	Description	R/W	Reset	Default
7:3	Reserved	RO	/	0
2	reset the gauge besides registers 0: normal 1: reset	RW	POR	0
1	PWRON 16s to POR the BMU enable 0: disable 1: enable	RW	POR	1
0	Software POR 0: normal 1: POR	RWAC	POR	0

6.16.2.19 REG 19H: Module enable control1

Bit	Description	R/W	Reset	Default
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7	Reserved	RO	/	0
6	Gauge in low frequency mode when system is PWROFF and Battery only 0: disable 1: enable	RW	POR	1
5	Reserved	RO	/	0
4	Boost enable 0: disable 1: enable	RW	System Reset	0
3	BUCK enable 0: disable 1: enable	RW	System Reset	1
2	CHGLED enable 0: disable 1: enable	RW	POR	1
1	Battery charge enable 0: disable 1: enable	RW	System Reset	1
0	Watchdog Module enable 0: disable 1: enable	RW	System Reset	0

6.16.2.20 REG 1AH: Watchdog control

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5:4	Watchdog Reset Configuration 00: IRQ only 01: IRQ and Registers System Reset 10: Registers System Reset, BATFET and BUCK Restart 11: POR	RW	POR	00b
3	watchdog clear signal 0: normal 1: clear	RWAC	POR	0b
2:0	TWSI watchdog timer configuration 000: 1s 001: 2s 010: 4s 011: 8s 100: 16s 101: 32s 110: 64s 111: 128s	RW	POR	110b

6.16.2.21 REG 1BH: Low Battery warning threshold setting

Bit	Description	R/W	Reset	Default
7:4	low battery warning threshold 5-20%, 1% per step 0000: 5% 0001: 6% 1111: 20%	RW	POR	1010b
3:0	low battery shutdown threshold 0-15%, 1% per step 0000: 0% 0001: 1% 1111: 15%	RW	POR	0001b

6.16.2.22 REG 1CH: PWRON configure

Bit	Description	R/W	Reset	Default
7	PWRON > OFFLEVEL to close BATFET enable	RW	POR	0

	0: disable 1: enable			
6	IRQ pin low to open BATFET enable 0: disable 1: enable	RW	POR	EFUSE
5:4	IRQLEVEL configuration 00: 1s 01: 1.5s 10: 2s 11: 2.5s	RW	POR	01b
3:2	OFFLEVEL configuration 00: 4s 01: 6s 10: 8s 11: 10s	RW	POR	01b
1:0	ONLEVEL configuration 00: 128ms 01: 512ms 10: 1s 11: 2s	RW	POR	EFUSE

6.16.2.23 REG 1DH: VBUS_OV/CHG_PWRON configure

Bit	Description	R/W	Reset	Default
7:6	VBUS over voltage threshold 00: 16.5V 01: 14.2V 10: 11V 11: 6.5V	RW	POR	00b
5:2	Reserved	RO	/	0
1:0	Voltage threshold of charger to send IRQ 00: 3.6V 01: 3.5V 10: 3.3V 11: 2.8V	RW	POR	10b

6.16.2.24 REG 1EH: Boost configure

Bit	Description	R/W	Reset	Default
7:4	Boost voltage regulation $4.55+0.064*N$ V 0000:4.550V 0001:4.614V 0010:4.678V 1110:5.446V 1111:5.510V	RW	System Reset	1001b
3:2	Boost Disable threshold 00: 3.2V 01: 3.0V 10: 3.4V 11:3.6V	RW	POR	01b
1:0	Reserved	RO	/	0

6.16.2.25 REG 22H: MPPT configure

Bit	Description	R/W	Reset	Default
7:2	Reserved	RO	/	0
1	MPPT_EN status 0: disable 1: enable	RO	POR	0
0	MPPT software enable 0: disable 1: enable	RW	POR	0

6.16.2.26 REG 28H: BC1.2 control0

Bit	Description	R/W	Reset	Default
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7	DCD Detection enable during BC detect. 0: disable 1: enable	RW	POR	0
6:5	DCD Detection time setting when DCD function enable 00: 100ms 01: 300ms 10: 500ms 11: 900ms	RW	POR	01b
4	The D- VLGC Compare enable during the BC Detect in primary detection 0: disable 1: enable	RW	POR	0
3	The BC stays in dead battery status timeout enable when the battery voltage below the dead threshold. 0: disable 1: enable Note : the time is 45 min	RW	POR	0
2	BC detection status indication 0: detect finish 1: in detecting	RO	POR	0
1:0	Reserved	RO	/	0

6.16.2.27 REG 29H: BC1.2 control1

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5	DP/DM floating Detection enable when BC detection is not DCP and CDP. 0: disable 1: enable	RW	POR	1
4:0	Reserved	RO	/	0

6.16.2.28 REG 2AH: BC1.2 control2

Bit	Description	R/W	Reset	Default
7	Reserved	RO	/	0
6	Dead Battery detection enable. 0: disable 1: enable. Note : if the battery is not connect, this function will disable.	RW	POR	0
5	The control is the time setting for pull up the DP to 0.6V when detection result is DCP. 0: delay 8ms 1: on delay	RO	POR	0
4	The control bit for pull up the DP to 0.6V when detection result is DCP 0: disable 1: enable	RW	POR	0
3	The detection result can be change when the rid is change after the BC detect finish. 0: disable 1: enable	RW	POR	0
2:0	Reserved	RO	/	0

6.16.2.29 REG 2BH: BC1.2 control3

Bit	Description	R/W	Reset	Default
7	Force D+/D- detection 0: Not in D+/D- 1: Force D+/D- detection Note : This bit will clear itself.	RW	POR	0
6	automatic D+/D- detection enable(AUTO_DPDM_EN) 0: disable D+/D- detection when VBUS is plugged-in 1: enable D+/D- detection when VBUS is plugged-in	RW	POR	1
5:0	Reserved	RO	/	0

6.16.2.30 REG 30H: CHGLED configure

Bit	Description	R/W	Reset	Default
7	CHGLED pin select 0: Open Drain 1: Push-Pull	RW	POR	0
6	CHGLED pin output breath enable when REG30[2:0]=011b 0: disable 1: enable	RW	System Reset	0b
5:3	CHGLED pin output when REG30[2:0]=110b 000: Hiz 001: Low/Hiz 25%/75% duty 1Hz 010: Low/Hiz 25%/75% duty 4Hz 011: drive low 100: drive high(when CHGLED is push-pull) 101~111: Reserved	RW	System Reset	00b
2:0	CHGLED pin display function configuration 000: display with type A function 001: display with type B function 010: display with breath function controlled by charger 011: display with breath function controlled by registers of breath 100~101: Reserved 110: display controlled by the register REG30[5:3] 111: Reserved	RW	POR	EFUSE

6.16.2.31 REG 32H: Breath LED control0

Bit	Description	R/W	Reset	Default
7:0	CL (the time unit count set for breath function stay in DMIN, the time unit is TUL.) So, $TL = CL * TUL$, TL should larger than PWM period, and default is 1.6s.	RW	POR	64H

6.16.2.32 REG 33H: Breath LED control1

Bit	Description	R/W	Reset	Default
7:0	CH (the time unit count set for breath function stay in DMAX, the time unit is TUH.) So, $TH = CH * TUH$, TL should larger than PWM period, and default is 96ms.	RW	POR	06H

6.16.2.33 REG 34H: Breath LED control2

Bit	Description	R/W	Reset	Default
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7:0	CSR (the time unit count set for breath function stay in every step from DMIN rise to DMAX, the time unit is TUS.) So, $TSR = TUS \times CSR$, TSR should larger than PWM period, and default is 16ms. And the total rise time, $TR = TSR \times NC$, default is 1.6s. CSF is the same.	RW	POR	01H
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6.16.2.34 REG 36H: Breath LED control3

Bit	Description	R/W	Reset	Default
7:0	Breath function total duty step count setting between DMIN and DMAX, NS. So, the breath Maximal duty(DMAX) is $(NMIN+NS)/M$, default is 100%. Note: $(NMIN+NS) \leq M$	RW	POR	64H

6.16.2.35 REG 37H: Breath LED control4

Bit	Description	R/W	Reset	Default
7:0	For breath function Minimal duty setting, NMIN (the high level clock number in every PWM period, the clock frequency is f_0). So, the breath Minimal duty(DMIN) is $NMIN/M$, default is 0%.	RW	POR	00H

6.16.2.36 REG 38H: Breath LED control5

Bit	Description	R/W	Reset	Default
7:0	M(the total clock number in every PWM output period, the clock frequency is f_0). So f_{PWM} (the PWM output frequency) is f_0/M , default is 5kHz.	RW	POR	64H

6.16.2.37 REG 40H: IRQ Enable 0

Bit	Description	R/W	Reset	Default
7	SOC drop to Warning Level IRQ enable 0: disable 1: enable	RW	System Reset	1b
6	SOC drop to Shutdown Level IRQ enable 0: disable 1: enable	RW	System Reset	1b
5	Reserved	RO	/	1b
4	Gauge New SOC IRQ enable 0: disable 1: enable	RW	System Reset	1b
3	Charge to normal IRQ enable 0: disable 1: enable	RW	POR	0b
2	BOOST Over Voltage IRQ enable 0: disable 1: enable	RW	System Reset	0b
1	VBUS Over Voltage IRQ enable 0: disable 1: enable	RW	System Reset	1b
0	VBUS Fault IRQ enable 0: disable 1: enable	RW	System Reset	1b

6.16.2.38 REG 41H: IRQ Enable 1

Bit	Description	R/W	Reset	Default
7	VBUS Insert IRQ enable 0: disable 1: enable	RW	POR	1b
6	VBUS Remove IRQ enable	RW	System	1b

	0: disable 1: enable		Reset	
5	Battery Insert IRQ enable 0: disable 1: enable	RW	System Reset	1b
4	Battery Remove IRQ enable 0: disable 1: enable	RW	System Reset	1b
3	PWRON pin Short PRESS IRQ enable 0: disable 1: enable	RW	System Reset	1b
2	PWRON pin Long PRESS IRQ enable 0: disable 1: enable	RW	POR	1b
1	PWRON pin Negative Edge IRQ enable 0: disable 1: enable	RW	System Reset	0b
0	PWRON pin Positive Edge IRQ enable 0: disable 1: enable	RW	System Reset	0b

6.16.2.39 REG 42H: IRQ Enable 2

Bit	Description	R/W	Reset	Default
7	Watchdog Expire IRQ enable 0: disable 1: enable	RW	System Reset	0b
6-5	Reserved	RO	/	0b
4	Battery charge done IRQ enable 0: disable 1: enable	RW	System Reset	1b
3	Charger start IRQ enable 0: disable 1: enable	RW	System Reset	1b
2	DIE Over Temperature level1 IRQ enable 0: disable 1: enable	RW	System Reset	1b
1	Charger Safety Timer1/2 expire IRQ enable 0: disable 1: enable	RW	System Reset	1b
0	Battery Over Voltage Protection IRQ enable 0: disable 1: enable	RW	System Reset	1b

6.16.2.40 REG 43H: IRQ Enable 3

Bit	Description	R/W	Reset	Default
7	BC1.2 detect finished IRQ enable 0: disable 1: enable	RW	System Reset	1b
6	BC1.2 detect result change IRQ enable 0: disable 1: enable	RW	System Reset	1b
5	Reserved	RO	/	0b
4	Battery Over Temperature Quit IRQ enable 0: disable 1: enable	RW	System Reset	1b
3	Battery Over Temperature in Charge mode IRQ enable 0: disable 1: enable	RW	System Reset	1b
2	Battery Under Temperature in Charge mode IRQ enable 0: disable 1: enable	RW	System Reset	1b
1	Battery Over Temperature in Work mode IRQ enable 0: disable 1: enable	RW	System Reset	1b
0	Battery Under Temperature in Work mode IRQ enable 0: disable 1: enable	RW	System Reset	1b

6.16.2.41 REG 48H: IRQ Status 0

Bit	Description	R/W	Reset	Default
7	SOC drop to Warning Level IRQ	RW1C	System	0b

	0: no irq 1: irq when SOC >= Warning Level or SOC < shutdown Level to clear it		Reset	
6	SOC drop to Shutdown Level IRQ 0: no irq 1: irq when SOC >= Shutdown Level to clear it	RW1C	System Reset	0b
5	Reserved	RO	/	0b
4	Gauge New SOC IRQ 0: no irq 1: irq	RW1C	System Reset	0b
3	Charge to normal IRQ 0: no irq 1: irq	RW1C	POR	0b
2	BOOST Over Voltage IRQ 0: no irq 1: irq	RW1C	System Reset	0b
1	VBUS Over Voltage IRQ 0: no irq 1: irq	RW1C	System Reset	0b
0	VBUS Fault IRQ 0: no irq 1: irq	RW1C	System Reset	0b

6.16.2.42 REG 49H: IRQ Status 1

Bit	Description	R/W	Reset	Default
7	VBUS Insert IRQ 0: no irq 1: irq VBUS Remove to clear it	RW1C	POR	0b
6	VBUS Remove IRQ 0: no irq 1: irq VBUS Insert to clear it	RW1C	System Reset	0b
5	Battery Insert IRQ 0: no irq 1: irq Battery Remove to clear it	RW1C	System Reset	0b
4	Battery Remove IRQ 0: no irq 1: irq Battery Insert to clear it	RW1C	System Reset	0b
3	PWRON pin Short PRESS IRQ 0: no irq 1: irq	RW1C	System Reset	0b
2	PWRON pin Long PRESS IRQ 0: no irq 1: irq	RW1C	POR	0b
1	PWRON pin Negative Edge IRQ 0: no irq 1: irq	RW1C	System Reset	0b
0	PWRON pin Positive Edge IRQ 0: no irq 1: irq	RW1C	System Reset	0b

6.16.2.43 REG 4AH: IRQ Status 2

Bit	Description	R/W	Reset	Default
7	Watchdog Expire IRQ 0: no irq 1: irq	RW1C	System Reset	0b
6-5	Reserved	RO	/	0b
4	Battery charge done IRQ 0: no irq 1: irq Battery charge start to clear it	RW1C	System Reset	0b
3	Battery charge start IRQ 0: no irq 1: irq Battery charge done to clear it	RW1C	System Reset	0b

2	DIE Over Temperature level1 IRQ 0: no irq 1: irq DIE Temperature to normal to clear it	RW1C	System Reset	0b
1	Charger Safety Timer1/2 expire IRQ 0: no irq 1: irq	RW1C	System Reset	0b
0	Battery Over Voltage Protection IRQ 0: no irq 1: irq Battery Voltage to normal to clear it	RW1C	System Reset	0b

6.16.2.44 REG 4BH: IRQ Status 3

Bit	Description	R/W	Reset	Default
7	BC1.2 detect finished IRQ. 0: no irq 1: irq VBUS remove, bc1.2 detect again will clear it.	RW1C	System Reset	0b
6	BC1.2 detect result change IRQ 0: no irq 1: irq VBUS remove will clear it	RW1C	System Reset	0b
5	Reserved	RO	/	0b
4	Battery Over Temperature Quit in Charge mode IRQ 0: no irq 1: irq bcot_irq to clear it	RW1C	System Reset	0b
3	Battery Over Temperature in Charge mode IRQ 0: no irq 1: irq bcotq_irq to clear it	RW1C	System Reset	0b
2	Battery Under Temperature in Charge mode IRQ 0: no irq 1: irq Battery Temperature to normal to clear it	RW1C	System Reset	0b
1	Battery Over Temperature in Work mode IRQ 0: no irq 1: irq Battery Temperature to normal to clear it	RW1C	System Reset	0b
0	Battery Under Temperature in Work mode IRQ 0: no irq 1: irq Battery Temperature to normal to clear it	RW1C	System Reset	0b

6.16.2.45 REG 50H: TS pin configure

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4	TS PIN function select: 0: TS pin is the battery temperature sensor input and will affect the charger 1: TS pin is the external fixed input and doesn't affect the charger	RW	POR	EFUSE
3:2	TS current source on/off enable 00: off 01/10: on when TS channel of ADC is enabled 11: always on	RW	POR	EFUSE
1:0	current source to TS pin configuration 00: 20uA 01: 40uA 10: 50uA 11: 60uA	RW	POR	10b

6.16.2.46 REG 52H: TS_HYSL2H setting

Bit	Description	R/W	Reset	Default
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7:0	hysteresis for TS from low go to normal Thys = N*16mV (default 32mV)	RW	POR	2H
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6.16.2.47 REG 53H: TS_HYSH2L setting

Bit	Description	R/W	Reset	Default
7:0	hysteresis for TS from high go to normal Thys = N*4mV (default 4mV)	RW	POR	1H

6.16.2.48 REG 54H: VLTFCHG setting

Bit	Description	R/W	Reset	Default
7:0	VLTF in voltage of charge configuration VLTF = N*32 mV (default is about 0deg) This is also T1 of JEITA	RW	POR	29H

6.16.2.49 REG 55H: VHTFCHG setting

Bit	Description	R/W	Reset	Default
7:0	VHTF in voltage of charge configuration VHTF = N*2 mV (default is about 55deg) This is also T4 of JEITA	RW	POR	58H

6.16.2.50 REG 56H: VLTFWORK setting

Bit	Description	R/W	Reset	Default
7:0	VLTF in voltage of work configuration VLTF = N*32 mV (default is about -10deg)	RW	POR	3EH

6.16.2.51 REG 57H: VHTFWORK setting

Bit	Description	R/W	Reset	Default
7:0	VHTF in voltage of work configuration VHTF = N*2 mV (default is about 60deg)	RW	POR	4CH

6.16.2.52 REG 58H: JEITA standard Enable control

Bit	Description	R/W	Reset	Default
7:1	Reserved	RO	/	0
0	JEITA Standard Enable 0: disable 1: enable	RW	POR	EFUSE

6.16.2.53 REG 59H: JEITA current/voltage configuration

Bit	Description	R/W	Reset	Default
7:6	Current fall of Warm in JEITA Standard 00: 100% 01: 50% 10: 25% 11: Reserved	RW	POR	00b
5:4	Current fall of Cool in JEITA Standard 00: 100% 01: 50% 10: 25% 11: Reserved	RW	POR	01b
3:2	Voltage fall of Warm in JEITA Standard 00: Not change 01: 100mV lower 10: 200mV lower 11: Reserved	RW	POR	01b
1:0	Voltage fall of Cool in JEITA Standard 00: Not change 01: 100mV lower 10: 200mV lower	RW	POR	00b

	11: Reserved			
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6.16.2.54 REG 5AH: JEITA Cool configuration

Bit	Description	R/W	Reset	Default
7:0	Cool Temperature(T2) in voltage of charge configuration VHTF = N*16 mV (default is about 10deg)	RW	POR	37H

6.16.2.55 REG 5BH: JEITA Warm configuration

Bit	Description	R/W	Reset	Default
7:0	Warm Temperature(T3) in voltage of charge configuration VHTF = N*8 mV (default is about 45deg)	RW	POR	1EH

6.16.2.56 REG 5CH: TS_data_h configure

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0b
5:0	TS_data_h[13:8]	RW	POR	2H

6.16.2.57 REG 5DH: TS_data_l configure

Bit	Description	R/W	Reset	Default
7:0	TS_data_l[7:0] Note: TS_data_configure is valid when reg82H[3]=1.	RW	POR	58H

6.16.2.58 REG 61H: Iprechg/Itrichg setting

Bit	Description	R/W	Reset	Default
7	Reserved	RO	/	0
6:4	Tricharge current limit: 32*N mA 000: not valid 001: 32mA 010: 64mA 110: 192mA 111: 224mA	RW	POR	011b
3:0	Precharge current limit: 64*N mA 0000: 0mA 0001: 64mA 0010: 128mA 0100: 896mA 0101: 960mA	RW	POR	0010b

6.16.2.59 REG 62H: ICC setting

Bit	Description	R/W	Reset	Default
7	Reserved	RO	/	0
6:0	constant current charge current limit: 64*N mA if N<=80 0000000: 0mA 0000001: 64mA 0000010: 128mA 0010000: 1024mA 1001111: 5056mA 1010000: 5120mA 1010001~1111111: Reserved	RW	POR	0010000 b

6.16.2.60 REG 63H: Iterm setting and control

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5	DPM to disable charger terminal 0: enable charger terminal	RW	POR	0b

	1: disable charger terminal			
4	Charging termination of current enable 0: disable 1: enable	RW	System Reset	1b
3:0	Termination current limit: 64*N mA 0000: 0mA 0001: 64mA 0010: 128mA 0111: 896mA 1000: 960mA	RW	POR	0101b

6.16.2.61 REG 64H: CV charger voltage setting

Bit	Description	R/W	Reset	Default
7	Reserved	RO	/	0
6:0	Charge voltage limit 3.104+0.016*N 0000000~0010100: Reserved 0010101: 3.44V 1000101: 4.208V 1001110: 4.352V	RW	POR	1000101b

6.16.2.62 REG 65H: Thermal regulation threshold setting

Bit	Description	R/W	Reset	Default
7:2	Reserved	RO	/	0
1:0	Thermal regulation threshold 00: 60deg 01: 80deg 10: 100deg 11: 120deg	RW	System Reset	10b

6.16.2.63 REG 67H: Charger timer configure

Bit	Description	R/W	Reset	Default
7	safety timer1/2 setting during DPM or thermal regulation 0: safety timer not slowed during input DPM or thermal regulation 1: safety timer slowed during input DPM or thermal regulation	RW	POR	1b
6	Fast charge safe timer enable 0: disable 1: enable	RW	POR	0b
5:4	Fast charge safety timer configuration 00: 5hours 01: 8hours 10: 12hours 11: 20hours	RW	POR	10b
3	Reserved	RO	/	0
2	pre-charge safe timer enable 0: disable 1: enable	RW	POR	0b
1:0	pre-charge safe timer configuration 00: 40mins 01: 50mins 10: 60mins 11: 70mins	RW	POR	10b

6.16.2.64 REG 68H: Battery detection control

Bit	Description	R/W	Reset	Default
7:1	Reserved	RO	/	0
0	battery detection enable 0: disable 1: enable	RW	POR	1

6.16.2.65 REG 70H: Battery parameter

Bit	Description	R/W	Reset	Default
7:0	Battery parameter ROM	RO	POR	xx

6.16.2.66 REG 71H: Fuel gauge control

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5	Reserved	RO	/	0
4	ROM or SRAM select 1: select sram; 0: select rom;	RW	POR	0b
3:1	Reserved	RO	/	0
0	brom writer control 1:enable 0:disable	RW	POR	0b

6.16.2.67 REG 72H: Battery temperature

Bit	Description	R/W	Reset	Default
7:0	battery temperature	RO	POR	00h

6.16.2.68 REG 73H: Battery SOH

Bit	Description	R/W	Reset	Default
7:0	battery SOH	RO	POR	00h

6.16.2.69 REG 74H: Battery Battery percentage

Bit	Description	R/W	Reset	Default
7:0	battery percentage	RO	POR	00h

6.16.2.70 REG 82H: TS source select

Bit	Description	R/W	Reset	Default
7:4	Reserved	RO	/	0
3	TS data source select 0: TS ADC 1: TS data configure	RW	POR	0
2:0	Reserved	RO	/	0

6.16.2.71 REG 90H: ADC Channel enable control

Bit	Description	R/W	Reset	Default
7	VBUS current measure ADC channel enable 0: disable 1: enable	RW	POR	0b
6	BAT discharge current measure ADC channel enable 0: disable 1: enable	RW	POR	1b
5	BAT charge current measure ADC channel enable 0: disable 1: enable	RW	POR	1b
4	Die temperature measure ADC channel enable 0: disable 1: enable	RW	POR	1b
3	System voltage measure ADC channel enable 0: disable 1: enable	RW	POR	0b
2	VBUS voltage measure ADC channel enable 0: disable 1: enable	RW	POR	0b

1	TS pin measure ADC channel enable 0: disable 1: enable	RW	POR	1b
0	Battery voltage measure ADC channel enable 0: disable 1: enable	RW	POR	1b

6.16.2.72 REG 91H: vbat_h

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0b
5:0	vbat[13:8]	RO	POR	0b

6.16.2.73 REG 92H: vbat_l

Bit	Description	R/W	Reset	Default
7:0	vbat[7:0]	RO	POR	0b

6.16.2.74 REG 93H: ibat_h

Bit	Description	R/W	Reset	Default
7:0	ibat[15:8]	RO	POR	0b

6.16.2.75 REG 94H: ibat_l

Bit	Description	R/W	Reset	Default
7:0	ibat[7:0]	RO	POR	0b

6.16.2.76 REG 95H: ts_h

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0b
5:0	ts[13:8]	RO	POR	0b

6.16.2.77 REG 96H: ts_l

Bit	Description	R/W	Reset	Default
7:0	ts[7:0]	RO	POR	0b

6.16.2.78 REG 97H: ibus_h

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0b
5:0	ibus[13:8]	RO	POR	0b

6.16.2.79 REG 98H: ibus_l

Bit	Description	R/W	Reset	Default
7:0	ibus[7:0]	RO	POR	0b

6.16.2.80 REG 99H: vbus_h

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0b
5:0	vbus[13:8]	RO	POR	0b

6.16.2.81 REG 9AH: vbus_l

Bit	Description	R/W	Reset	Default
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7:0	vbus[7:0]	RO	POR	0b
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6.16.2.82 REG 9BH: ADC data select

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4	ts_offset measure ADC channel enable 0: disable 1: enable	RW	POR	0b
3:0	adc_data_h/adc_data_l select configure: 0000: Tdie 0001: vsys 0010~0101: Reserved 0110: Ichg 0111: Idischg 1000~1111: Reserved	RW	POR	0000b

6.16.2.83 REG 9CH: adc_data_h

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5:0	adc_data_h[13:8]	RO	POR	0b

6.16.2.84 REG 9DH: adc_data_l

Bit	Description	R/W	Reset	Default
7:0	adc_data_l[7:0]	RO	POR	0b

6.16.2.85 REG 9EH: ADC CONFIG

Bit	Description	R/W	Reset	Default
7	ts_offset auto cancellation enable 0: disable 1: enable	RW	POR	0b
6:0	Reserved	RO	/	0

6.16.2.86 REG A6H: USBTYPEPEC_REV

Bit	Description	R/W	Reset	Default
7:0	USBTYPEPEC_REV	RO	System Reset	0x22

6.16.2.87 REG A7H: USBTYPEPEC_REV

Bit	Description	R/W	Reset	Default
7:0	Reserved	RO	System Reset	0x00

6.16.2.88 REG A8H: USBPD_VER

Bit	Description	R/W	Reset	Default
7:0	USBPD_VER	RO	System Reset	0x11

6.16.2.89 REG A9H: USBPD_REV

Bit	Description	R/W	Reset	Default
7:0	USBPD_REV	RO	System Reset	0x30

6.16.2.90 REG AAH: PD_INTERFACE_VER

Bit	Description	R/W	Reset	Default
7:0	PD_INTERFACE_VER	RO	System Reset	0x13

6.16.2.91 REG ABH: PD_INTERFACE_REV

Bit	Description	R/W	Reset	Default
7:0	PD_INTERFACE_REV	RO	System Reset	0x20

6.16.2.92 REG B0H: PD_ALERTL

Bit	Description	R/W	Reset	Default
7	VBUS_ALARM_H I 0: Cleared 1: A high-voltage alarm has occurred	RW1C	System Reset	0b
6	TX_SUCCESS 0: Cleared 1: Reset or SOP* message transmission successful	RW1C	System Reset	0b
5	TX_DISCARD 0: Cleared 1: Reset or SOP* message transmission not sent due to incoming receive message	RW1C	System Reset	0b
4	TX_FAIL 0: Cleared 1: SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission	RW1C	System Reset	0b
3	RX_HARD_RESET 0: Cleared 1: Received Hard Reset message	RW1C	System Reset	0b
2	RX_SOP_MSG_STATUS 0: Cleared 1: RECEIVE_BUFFER register changed	RW1C	System Reset	0b
1	POWER_STATUS 0: Cleared 1: Port status changed	RW1C	System Reset	0b
0	CC_STATUS 0: Cleared 1: CC_STATUS is changed	RW1C	System Reset	0b

6.16.2.93 REG B1H: PD_ALERTH

Bit	Description	R/W	Reset	Default
7-6	Reserved	R	System Reset	0b
5	Extended_Status 0: Cleared 1: Extended Status changed	RW1C	System Reset	0b
4	Reserved	R	System Reset	0b
3	VBUS_SINK_DIS_DET 0: Cleared 1: A VBUS sink disconnect threshold crossing has been detected(AUTO_DISC_DISCNCT=1)	RW1C	System Reset	0b
2	RXBUF_OVFLOW 0: Rx buffer is functioning properly 1: Rx buffer has overflowed	RW1C	System Reset	0b
1	FAULT 0: No Fault	RW1C	System Reset	0b

	1: A Fault has occurred			
0	VBUS_ALARM_LO 0: Cleared 1: A low-voltage alarm has occurred	RW1C	System Reset	0b

6.16.2.94 REG B2H: PD_ALERT_MASKL

Bit	Description	R/W	Reset	Default
7	M_VBUS_ALARM_HI 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b
6	M_TX_SUCCESS 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b
5	M_TX_DISCARD 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b
4	M_TX_FAIL 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b
3	M_RX_HARD_RESET 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b
2	M_RX_SOP_MSG_STATUS 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b
1	M_POWER_STATUS 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b
0	M_CC_STATUS 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b

6.16.2.95 REG B3H: PD_ALERT_MASKH

Bit	Description	R/W	Reset	Default
7-6	Reserved	R	System Reset	0b
5	M_Extended_Status 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b
4	Reserved	R	System Reset	0b
3	M_VBUS_SINK_DIS_DET 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b
2	M_RXBUF_OVFLOW 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b
1	M_FAULT 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b
0	M_VBUS_ALARM_LO 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b

6.16.2.96 REG B4H: POWER_STATUS_MASK

Bit	Description	R/W	Reset	Default
7	M_DEBUG_ACCESSORY 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b
6	M_TCPC_INIT_STATUS 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b
5-4	Reserved	R	System Reset	0b
3	M_VBUS_PRESENT_DETC 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b
2	M_VBUS_PRESENT 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b
1	M_VCONN_PRESENT 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b
0	Reserved	R	System Reset	0b

6.16.2.97 REG B5H: FAULT_STATUS_MASK

Bit	Description	R/W	Reset	Default
7-6	Reserved	R	System Reset	0b
5	M_AUTO_DISC_FAIL 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b
4	M_FORCE_DISC_FAIL 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b
3-2	Reserved	R	System Reset	0b
1	M_VCON_OC 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b
0	M_TWSI_ERROR 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b

6.16.2.98 REG B6H: EXTENDED_STATUS_MASK

Bit	Description	R/W	Reset	Default
7-1	Reserved	R	System Reset	0b
0	M_vSafe0V_Status 0: Interrupt masked 1: Interrupt unmasked	RW	System Reset	1b

6.16.2.99 REG B9H: TCPC_CONTROL

Bit	Description	R/W	Reset	Default
7-2	Reserved	R	System Reset	0b
1	BIST_TEST_MODE 0: Normal Operation. Incoming messages enabled by RECEIVE_DETECT passed to TCPM via Alert	RW	System Reset	0b

	1: BIST Test Mode. Incoming messages enabled by RECEIVE_DETECT result in GoodCRC response but may not be passed to the TCPM via Alert. TCPM may temporarily store incoming messages in the Rx Buffer, but this may or may not result in a Receive SOP* Message Status or a Rx Buffer Overflow alert			
0	PLUG_ORIENT 0: When VCONN is enabled (0xBC[0]=1), apply it to the CC2 pin. Monitor the CC1 pin for BMC communications 1: When VCONN is enabled (0xBC[0]=1), apply it to the CC1 pin. Monitor the CC2 pin for BMC communications	RW	System Reset	0b

6.16.2.100 REG BAH: ROLE_CONTROL

Bit	Description	R/W	Reset	Default
7	Reserved	R	System Reset	0b
6	DRP 0: No DRP. Bit3-0 determine Rp/Rd/open settings 1: DRP. The TCPM toggles CC1&CC2 after receiving COMMAND.Look4Connection and until a connection is detected	RW	System Reset	0b
5-4	RP_VALUE 00: Rp default 01: Rp 1.5A 10: Rp 3.0A 11: Reserved	RW	System Reset	0b
3-2	CC2 00: Reserved 01: Rp (Use Rp definition in bit5-4) 10: Rd 11: Open (Disconnect or do not care)	RW	System Reset	10b
1-0	CC1 00: Reserved 01: Rp (Use Rp definition in bit5-4) 10: Rd 11: Open (Disconnect or do not care)	RW	System Reset	10b

6.16.2.101 REG BBH: FAULT_CONTROL

Bit	Description	R/W	Reset	Default
7-4	Reserved	R	System Reset	0b
3	DIS_VBUS_DISC_FAULT_TIMER 0: VBUS Discharge Fault Detection Timer enabled 1: VBUS Discharge Fault Detection Timer disabled This enables the timers for both FAULT_STATUTS.AutoDischargeFailed and FAULT_STATUS.ForceDischargeFailed Required	RW	System Reset	0b
2-1	Reserved	R	System Reset	0b
0	DIS_VCON_OC 0: Fault detection circuit disabled 1: Fault detection circuit enabled when EN_VCONN=1	RW	System Reset	0b

6.16.2.102 REG BCH: POWER_CONTROL

Bit	Description	R/W	Reset	Default
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7	Reserved	R	System Reset	0b
6	VBUS_VOL_MONITOR 0: VBUS_VOLTAGE Monitoring is enabled 1: VBUS_VOLTAGE Monitoring is disabled (default) Controls only VBUS_VOLTAGE Monitoring. VBUS_VOLTAGE shall report all zeroes if disabled.	RW	System Reset	1b
5	DIS_VOL_ALARM 0: Voltage Alarms Power status reporting is enabled 1: Voltage Alarms Power status reporting is disabled (default) Controls VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG.	RW	System Reset	1b
4	AUTO_DISC_DISCNCT 0: The TCPC shall not automatically discharge VBUS based on VBUS voltage (default) 1: The TCPC shall automatically discharge	RW	System Reset	0b
3	BLEED_DISC 0: Disable bleed discharge of VBUS (default) 1: Enable bleed discharge of VBUS	RW	System Reset	0b
2	FORCE_DISC 0: Disable forced discharge (default) 1: Enable forced discharge of VBUS	RW	System Reset	0b
1-0	Reserved	R	System Reset	0b

6.16.2.103 REG BDH: CC_STATUS

Bit	Description	R/W	Reset	Default
7-6	Reserved	R	System Reset	0b
5	Look4Connection 0: TCPC is NOT actively looking for a connection. A transition from 1 to 0 indicates a potential connection has been found 1: The TCPC is looking for a connection (toggling as a DRP or looking for a connection as Sink/Source only condition)	R	System Reset	0b
4	Connect_RESULT 0: The TCPC is currently presenting Rp 1: The TCPC is currently presenting Rd	R	System Reset	0b
3-2	CC2_STATUS If (ROLE_CONTROL.CC2 = Rp) or (Connect_RESULT = 0) 00: SRC.Open (Open, Rp) 01: SRC.Ra (below maximum vRa) 10: SRC.Rd (within the vRd range) 11: reserved If (ROLE_CONTROL.CC2 = Rd) or (Connect_RESULT = 1) 00: SNK.Open (Below maximum vRa) 01: SNK.Default (Above minimum vRdConnect) 10: SNK.Power1.5 (Above minimum vRdConnect) Detects Rp 1.5A 11: SNK.Power3.0 (Above minimum vRdConnect) Detects Rp 3.0A If ROLE_CONTROL.CC2 = 00b, this field is set to 00b If ROLE_CONTROL.CC2 = Open, this field is set to 00b and	R	System Reset	0b

	this change does not cause an Alert.CCStatus This field always returns 00b if (CC_STATUS[5] = 1), that means the CCStatus is not updated to these bits or (POWER_CONTROL.EN_VCONN = 1 and TCPC_CONTROL.PLUG_ORIENT = 0). Otherwise, the returned value depends upon ROLE_CONTROL.CC2			
1-0	CC1_STATUS If (ROLE_CONTROL.CC1 = Rp) or (Connect_RESULT = 0) 00: SRC.Open (Open, Rp) 01: SRC.Ra (below maximum vRa) 10: SRC.Rd (within the vRd range) 11: reserved If (ROLE_CONTROL.CC1 = Rd) or Connect_RESULT= 1) 00: SNK.Open (Below maximum vRa) 01: SNK.Default (Above minimum vRdConnect) 10: SNK.Power1.5 (Above minimum vRdConnect) Detects Rp-1.5A 11: SNK.Power3.0 (Above minimum vRdConnect) Detects Rp-3.0A If ROLE_CONTROL.CC1 = 00b, this field is set to 00b If ROLE_CONTROL.CC1 = Open, this field is set to 00b and this change doesn't cause an Alert.CCStatus This field always returns 00b if (CC_STATUS[5] = 1), that means the CCStatus is not updated to these bits or (POWER_CONTROL.EN_VCONN = 1 and TCPC_CONTROL.PLUG_ORIENT = 1). Otherwise, the returned value depends upon ROLE_CONTROL.CC1	R	System Reset	0b

6.16.2.104 REG BEH: POWER_STATUS

Bit	Description	R/W	Reset	Default
7	DEBUG_ACC_CONNECT 0: No Debug Accessory connected (default) 1: Debug Accessory connected	R	System Reset	0b
6	TCPC_INITIAL 0: The TCPC has completed initialization and all registers are valid 1: The TCPC is still performing internal initialization	R	System Reset	0b
5-4	Reserved	R	System Reset	0b
3	VBUS_PRESENT_DETC 0: VBUS Detection Disabled 1: VBUS Detection Enabled Indicates whether the TCPC is monitoring for VBUS Present and vSafe0V level, or the detection circuits have been powered off	R	System Reset	0b
2	VBUS_PRESENT This bit reflects the status of VBUS. It is an edge-triggered comparator. Only a valid rising or falling edge of VBUS can change this bit. The VBUS Detection is enabled by 0xC3 write 33 0: VBUS Disconnected (VBUS < VBUS_PRS)	R	System Reset	0b

	1: VBUS Connected (VBUS>VBUS_PRS)			
1	VCONN_PRESENT 0: VCONN is not present (VCONN<VCN_PRS) 1: This bit is asserted when VCONN present CC1 or CC2 (VCONN>VCN_PRS) When POWER_CONTROL[0]=0b, this bit is set as 0	R	System Reset	0b
0	Reserved	R	System Reset	0b

6.16.2.105 REG BFH: FAULT_STATUS

Bit	Description	R/W	Reset	Default
7-6	Reserved	R	System Reset	0b
5	AUTO_DISC_FAIL 0: No discharge failure 1: Discharge commanded by the TCPM failed If POWER_CONTROL.AutoDischargeDisconnect is set, the TCPC shall report discharge fails if VBUS is not below vSafe0V within tSafe0V.	RW1C	System Reset	0b
4	FORCE_DISC_FAIL 0: No discharge failure 1: Discharge commanded by the TCPM failed The TCPC shall report a discharge fails if VBUS is not below vSafe0V within tSafe0V.	RW1C	System Reset	0b
3-2	Reserved	R	System Reset	0b
1	VCON_OC This bit is set if the current exceeds the VCON_OC. 0: No Fault detected 1: Over-current VCONN fault latched	RW1C	System Reset	0b
0	TWSI_ERROR 0: No Error 1: TWSI error has occurred	RW1C	System Reset	0b

6.16.2.106 REG C0H: EXTENDED_STATUS

Bit	Description	R/W	Reset	Default
7-1	Reserved	R	System Reset	0b
0	vSafe0V 0: VBUS is not at vSafe0Vr 1: VBUS is at vSafe0V	RO	System Reset	0b

6.16.2.107 REG C3H: COMMAND

Bit	Description	R/W	Reset	Default
7-0	COMMAND 0x00: Default Value after POR. 0x22: DisableVbusDetect. Disable VBUS present and vSafe0V detection. This is an invalid COMMAND2 if the TCPC has sourcing or sinking power over VBUS enabled. 0x33: EnableVbusDetect. Enable VBUS present and vSafe0V detection. 0x99: Look4Connection. Start DRP Toggling if ROLE_CONTROL.DRP=1b. If ROLE_CONTROL.CC1/CC2= 01b start with Rp, if ROLE_CONTROL.CC1/CC2=10b start with Rd. 0xAA: RxOneMore. Configure the TCPC to automatically	RW	System Reset	0b

	clear the RECEIVE_DETECT register after sending the next GoodCRC. 0xDD: ResetTransmitBuffer. The TCPC resets the pointer of the TRANSMIT_BUFFER register to offset 1 and the contents of TRANSMIT_BUFFER becomes invalid when this COMMAND is issued by the TCPM. 0xEE: ResetReceiveBuffer. The TCPC resets the pointer of RECEIVE_BUFFER when this COMMAND is issued by the TCPM. If the pointer of RECEIVE_BUFFER.RX_BUF_BYTE_x is at 132 or less, writing this COMMAND would reset the pointer to 1.			
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6.16.2.108 REG C4H: DEVICE_CAPABILITIES_1L

Bit	Description	R/W	Reset	Default
7-5	ROLES_SUPPORT 110b: Source, Sink, DRP	R	System Reset	110b
4	ALL_SOP_SUPPORT 1: All SOP* messages are supported	R	System Reset	1b
3	SOURCE_VCONN 1: TCPC is capable of switching VCONN	R	System Reset	1b
2	CAP_SINK_VBUS 0: TCPC is not capable controlling the sink path to the system load	R	System Reset	0b
1	SOURCE_HV_VBUS 0: TCPC is not capable of sourcing nondefault voltages over VBUS	R	System Reset	0b
0	SOURCE_VBUS 0: TCPC is not capable of controlling the source path to VBUS	R	System Reset	0b

6.16.2.109 REG C5H: DEVICE_CAPABILITIES_1H

Bit	Description	R/W	Reset	Default
7	Reserved	R	System Reset	0b
6	CPB_VBUS_OC 0: VBUS OCP is not reported by the TCPC	R	System Reset	0b
5	Reserved	R	System Reset	0b
4	CPB_BLEED_DISC 1: Bleed Discharge is implemented in the TCPC	R	System Reset	1b
3	CPB_FORCE_DISC 1: Force Discharge is implemented in the TCPC	R	System Reset	1b
2	VBUS_MEASURE_ALARM 1: VBUS voltage measurement and VBUS Alarms	R	System Reset	1b
1-0	SOURCE_RP_SUPPORT 10: Rp 3.0A, 1.5A, and default Rp values which may be configured by the TCPM via the ROLE_CONTROL register	R	System Reset	10b

6.16.2.110 REG C6H: DEVICE_CAPABILITIES_2L

Bit	Description	R/W	Reset	Default
7	SINK_DISCONNECT_DET 1: VBUS_SINK_DISCONNECT_THRESHOLD implemented, VBUS falling below VBUS_SINK_DISCONNECT_THRESHOLD is used as indication of Sink disconnect.	R	System Reset	1b

6	STOP_DISC_THD 1: VBUS_STOP_DISCHARGE_THRESHOLD implemented	R	System Reset	1b
5-4	VBUS_VOL_ALARM_LSB 00: TCPC uses all allocated bits for its voltage and alarm thresholds for an effective threshold step of 25 mV	R	System Reset	00b
3-1	VCONN_POWER 010: 2.0W	R	System Reset	010b
0	VCONN_OCP 1: TCPC is capable of detecting a VCONN over-current fault	R	System Reset	1b

6.16.2.111 REG C7H: DEVICE_CAPABILITIES_2H

Bit	Description	R/W	Reset	Default
7-0	Reserved	R	System Reset	0b

6.16.2.112 REG CEH: MESSAGE_HEADER_INFO

Bit	Description	R/W	Reset	Default
7-5	Reserved	R	System Reset	0b
4	CABLE_PLUG 0: Message originated from Source, Sink, or DRP 1: Message originated from a Cable Plug	RW	System Reset	0b
3	DATA_ROLE 0: UFP 1: DFP	RW	System Reset	0b
2-1	USBDP_SPECREV 00: Revision 1.0 01: Revision 2.0 10: Revision 3.0 11: Reserved	RW	System Reset	01b
0	POWER_ROLE 0: Sink 1: Source	RW	System Reset	0b

6.16.2.113 REG CFH: RECEIVE_DETECT

Bit	Description	R/W	Reset	Default
7	Reserved	R	System Reset	0b
6	EN_CABLE_RST 0: TCPC does not detect Cable Reset signaling (default) 1: TCPC detects Cable Reset signaling	RW	System Reset	0b
5	EN_HARD_RST 0: TCPC does not detect Hard Reset signaling (default) 1: TCPC detects Hard Reset signaling	RW	System Reset	0b
4	EN_SOP2DB 0: TCPC does not detect SOP_DBG'' message (default) 1: TCPC detects SOP_DBG'' message	RW	System Reset	0b
3	EN_SOP1DB 0: TCPC does not detect SOP_DBG' message (default) 1: TCPC detects SOP_DBG' message	RW	System Reset	0b
2	EN_SOP'' 0: TCPC does not detect SOP'' message (default) 1: TCPC detects SOP'' message	RW	System Reset	0b
1	EN_SOP' 0: TCPC does not detect SOP' message (default) 1: TCPC detects SOP' message	RW	System Reset	0b

	0: TCPC does not detect SOP' message (default) 1: TCPC detects SOP' message			
0	EN_SOP 0: TCPC does not detect SOP message (default) 1: TCPC detects SOP message	RW	System Reset	0b

6.16.2.114 REG D0H: VBUS_VOLTAGE_L

Bit	Description	R/W	Reset	Default
7-0	vbus_volt_measure[7:0]	R	System Reset	0b

6.16.2.115 REG D1H: VBUS_VOLTAGE_H

Bit	Description	R/W	Reset	Default
7-3	Reserved	R	System Reset	0b
2-0	vbus_volt_measure[10:8]	R	System Reset	0b

6.16.2.116 REG D2H: VBUS_SNK_DISCONNECT_THLD_L

Bit	Description	R/W	Reset	Default
7-0	VBUS_SNK_DISCONNECT_THLD[7:0] 14mV/step, the default value is 3.5V When this register is programmed to a non-zero value and AUTO_DISCHARGE_DISCONNECT is enabled, the TCPC will use this field instead of VBUS_PRESENT to know when a detach has occurred and then discharge to vSafe0V. This threshold register is disabled if programmed to zero.	RW	System Reset	FAH

6.16.2.117 REG D3H: VBUS_SNK_DISCONNECT_THLD_H

Bit	Description	R/W	Reset	Default
7-3	Reserved	R	System Reset	0b
2-0	VBUS_SNK_DISCONNECT_THLD[10:8]	RW	System Reset	0b

6.16.2.118 REG D4H: VBUS_STOP_DISCHARGE_THLD_L

Bit	Description	R/W	Reset	Default
7-0	VBUS_STOP_DISCHARGE_THLD[7:0] 14mV/step, the default value is 0.8V When VBUS Stop Discharge Threshold register is programmed to a non-zero value and TCPC is a VBUS Source, the TCPC will discharge to value programmed into this register. If this register is programmed to all zeros, then TCPC will discharge to vSafe0V. If Software requires discharge to voltage other than vSafe0V, then software must program this register to desired voltage. When TUSB422 is a VBUS Sink and a detach occurs, discharge will always stop at vSafe0V.	RW	System Reset	39H

6.16.2.119 REG D5H: VBUS_STOP_DISCHARGE_THLD_H

Bit	Description	R/W	Reset	Default
7-3	Reserved	R	System Reset	0b
2-0	VBUS_STOP_DISCHARGE_THLD[10:8]	RW	System Reset	0b

6.16.2.120 REG D6H: VBUS_VLOT_ALM_HI_CFG_L

Bit	Description	R/W	Reset	Default
7-0	VBUS_VLOT_ALM_HI_CFG[7:0] 14mV/step When DISABLE_VOLTAGE_ALARMS = 0, a VBUS voltage higher than value programmed into this register will cause VBUS_ALARM_HI alert flag to get set. This threshold is always enabled. SW needs to program to a value greater than VBUS to prevent VBUS_ALARM_HI alert from continuously being set.	RW	System Reset	0b

6.16.2.121 REG D7H: VBUS_VLOT_ALM_HI_CFG_H

Bit	Description	R/W	Reset	Default
7-3	Reserved	R	System Reset	0b
2-0	VBUS_VLOT_ALM_HI_CFG[10:8]	RW	System Reset	0b

6.16.2.122 REG D8H: VBUS_VLOT_ALM_LO_CFG_L

Bit	Description	R/W	Reset	Default
7-0	VBUS_VLOT_ALM_LO_CFG[7:0] 14mV/step When DISABLE_VOLTAGE_ALARMS = 0, a VBUS voltage lower than value programmed into this register will cause VBUS_ALARM_LO alert flag to get set.	RW	System Reset	0b

6.16.2.123 REG D9H: VBUS_VLOT_ALM_LO_CFG_H

Bit	Description	R/W	Reset	Default
7-3	Reserved	R	System Reset	0b
2-0	VBUS_VLOT_ALM_LO_CFG[10:8]	RW	System Reset	0b

6.16.2.124 REG DAH: RX_BUFFER(FIFO)

Bit	Description	R/W	Reset	Default
7-0	RX_BYTE_COUNT RX_OBJ +3(RX_HEADER and RX_FRAME_TYPE)	R	System Reset	0b

6.16.2.125 REG DAH: RX_BUFFER(FIFO)

Bit	Description	R/W	Reset	Default
7-3	Reserved	R	System Reset	0b
2-0	RX_FRAME_TYPE Type of received frame 000: Received SOP 001: Received SOP' 010: Received SOP'' 011: Received SOP_DBG' 100: Received SOP_DBG'' 110: Received Cable Reset 111: Reserved	R	System Reset	0b

6.16.2.126 REG DAH: RX_BUFFER(FIFO)

Bit	Description	R/W	Reset	Default
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7-0	RX_HEADER_0/RX_HEADER_1(2 Bytes)	R	System Reset	0b
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6.16.2.127 REG DAH: RX_BUFFER(FIFO)

Bit	Description	R/W	Reset	Default
7-0	RX_OBJ1~RX_OBJ7(4*7 Bytes)	R	System Reset	0b

6.16.2.128 REG DBH: TX_BUF_FRAME_TYPE

Bit	Description	R/W	Reset	Default
7-6	Reserved	R	System Reset	0b
5-4	TX_RETRY_CNT 00: No message retry is required 01: Automatically retry message transmission once 10: Automatically retry message transmission twice 11: Automatically retry message transmission three times	RW	System Reset	0b
3	Reserved	R	System Reset	0b
2-0	TX_SOP_TYPE 000: Transmit SOP 001: Transmit SOP' 010: Transmit SOP'' 011: Transmit SOP_DBG' 100: Transmit SOP_DBG'' 101: Transmit Hard Reset 110: Transmit Cable Reset 111: Transmit BIST Carrier Mode 2 (TCPC shall exit the BIST mode no later than tBISTContMode(40ms)max).	RW	System Reset	0b

6.16.2.129 REG DCH: TX_BUFFER(FIFO)

Bit	Description	R/W	Reset	Default
7-0	TX_BYTE_COUNT TX_OBJ +2(TX_HEADER)	RW	System Reset	0b

6.16.2.130 REG DCH: TX_BUFFER(FIFO)

Bit	Description	R/W	Reset	Default
7-0	TX_HEADER_0/TX_HEADER_1(2 Bytes)	RW	System Reset	0b

6.16.2.131 REG DCH: TX_BUFFER(FIFO)

Bit	Description	R/W	Reset	Default
7-0	TX_OBJ1~TX_OBJ7(4*7 Bytes)	RW	System Reset	0b

6.16.2.132 REG DCH: TX_BUFFER(FIFO)

Bit	Description	R/W	Reset	Default
7-0	TX_OBJ1~TX_OBJ7(4*7 Bytes)	RW	System Reset	0b

6.16.2.133 REG EAH: EN_VCONN

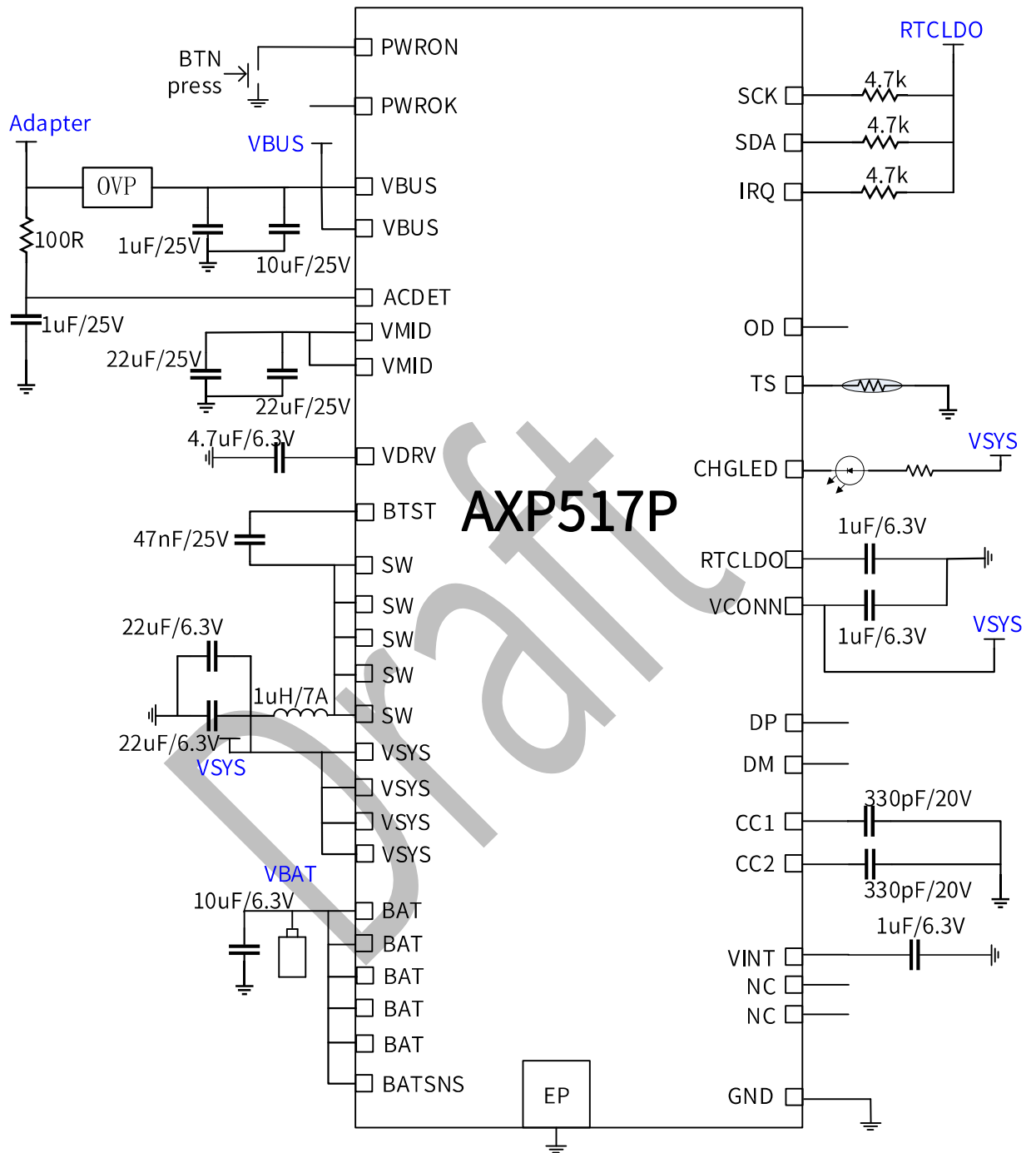
Bit	Description	R/W	Reset	Default
7-6	Reserved	R	System Reset	0b
5	EN_VCONN This bit control the path from VCONN pin to the repopulated CC pin (unattached CC). 0: Disable VCONN Path(default)	RW	System Reset	0b

	1: Enable VCONN Source to unattached CC			
4-0	Reserved	R	System Reset	0b

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7 Application Information

7.1 Typical Application



8 Package, Carrier, Storage and Baking Information

8.1 Package

AXP517P package is QFN5*5, 40-pin. Figure 8-1 shows AXP517P package.

Figure 8-1 Package Information

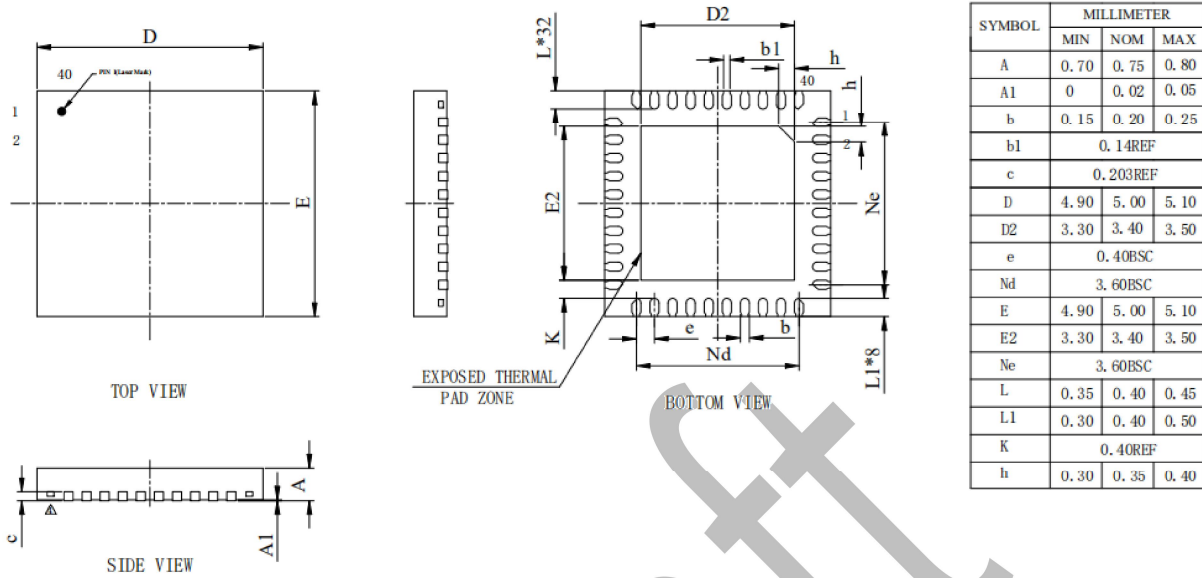


Figure 8-2 AXP517P Marking

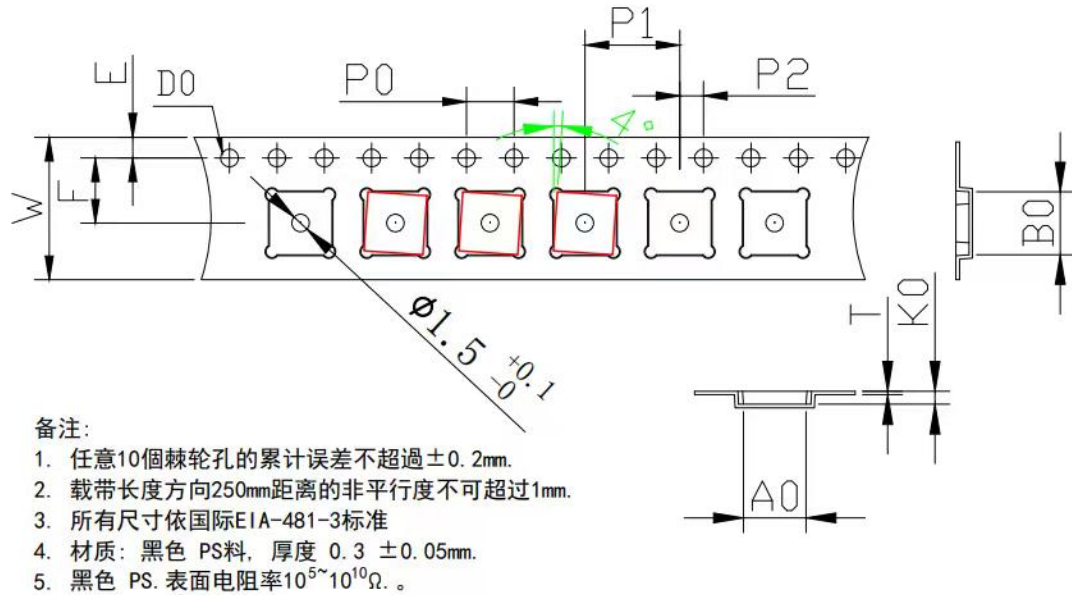


Table 8-1 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	AXP517P	Product name	Fixed
2	LLLLLLL	Lot number	Dynamic
3	XXXXX	Date code	Dynamic
4		X-POWERS logo	Fixed
5	White dot	Package pin 1	Fixed

8.2 Carrier

Figure 8-3 Tray Dimension Drawing



ITEM	W	A0	B0	K0	P0	P1	P2	F	S	E	D0	T
DIM	12 ± 0.30	5.30 ± 0.1	5.30 ± 0.1	0.85 ± 0.1	4.0 ± 0.1	8.0 ± 0.1	2.0 ± 0.1	5.5 ± 0.1	0.0 ± 0.1	1.75 ± 0.1	1.5 ± 0.1	0.3 ± 0.05

Table 8-2 Packing Quantity Information

Type	Quantity	Part Number
Tape	3000pcs/Tape	AXP517P

8.3 Storage

8.3.1 Moisture Sensitivity Level(MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. All MSL are defined in the following table.

Table 8-3 MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	$\leq 30^\circ\text{C}/85\%\text{RH}$
2	1 year	$\leq 30^\circ\text{C}/60\%\text{RH}$
2a	4 weeks	$\leq 30^\circ\text{C}/60\%\text{RH}$
3	168 hours	$\leq 30^\circ\text{C}/60\%\text{RH}$
4	72 hours	$\leq 30^\circ\text{C}/60\%\text{RH}$
5	48 hours	$\leq 30^\circ\text{C}/60\%\text{RH}$
5a	24 hours	$\leq 30^\circ\text{C}/60\%\text{RH}$
6	Time on Label(TOL)	$\leq 30^\circ\text{C}/60\%\text{RH}$

AXP517P device samples are classified as MSL3.

8.3.2 Bagged Storage Conditions

The shelf life of AXP517P are defined in the following table.

Table 8-4 Bagged Storage Conditions

Packing mode	Vacuum packing
Storage temperature	20°C~26°C
Storage humidity	40%~60%RH
Shelf life	12 months

8.3.3 Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration of AXP517P is as follows.

Table 8-5 Out-of-bag Duration

Storage temperature	20°C~26°C
Storage humidity	40%~60%RH
Moisture Sensitivity Level(MSL)	3
Floor life	168 hours

For no mention of storage rules in this document, please refer to the latest *IPC/JEDEC J-STD-020C*.

8.4 Baking

It is not necessary to bake AXP517P if the conditions specified in Section 8.3.2 and Section 8.3.3 have not been exceeded. It is necessary to bake AXP517P if any condition specified in Section 8.4.2 and Section 8.4.3 have been exceeded.

Table 8-6 Baking Conditions

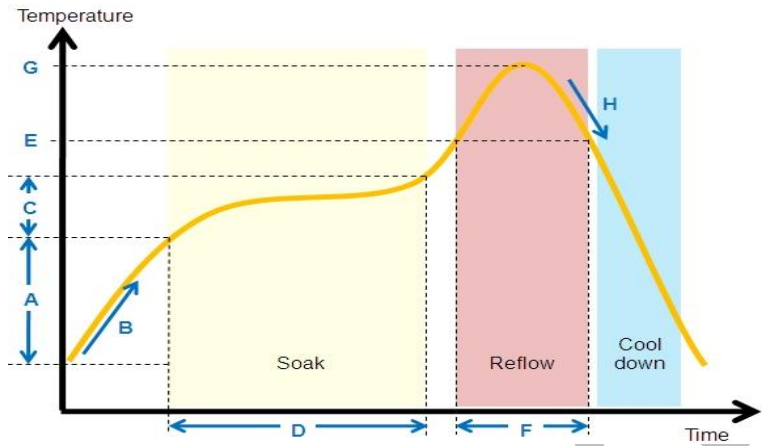
Surrounding	Condition	Note
Nitrogen	Tape: 60°C/72 hours, ≤5% RH	Bake no more than once.

9 Reflow Profile

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste.

The following figure shows the typical reflow profile of AXP517P device sample.

Figure 9-1 AXP517P Typical Reflow Profile



Reflow profile conditions of AXP517P device sample is given in the following table.

Table 9-1 AXP517P Reflow Profile Conditions

QTI typical SMT reflow profile conditions (for reference only)		
Step		Reflow condition
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25°C -> 150°C
B	Preheat ramp up rate	1.5~2.5 °C /sec
C	Soak temperature range	150°C -> 190°C
D	Soak time	80~110 sec
E	Liquidus temperature	217°C
F	Time above liquidus	60~90 sec
G	Peak temperature	240~250°C
H	Cool down temperature rate	≤4°C /sec

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