UMW HCPL-4506-xxxE

1.Description

HCPL-4506 contain a GaAsP LED . The LED is optically coupled to an integrated high gain photo detector. Minimized propagation delay difference between devices makes these optocouplers excellent solutions for improving inverter efficiency through reduced switching dead time. An on-chip 20-kΩ output pull-up resistor can be enabled by shorting output pins 6 and 7, thus eliminating the need for an external pull-up resistor in common IPM applications. Specifications and performanc e plots are given for typical IPM applications.

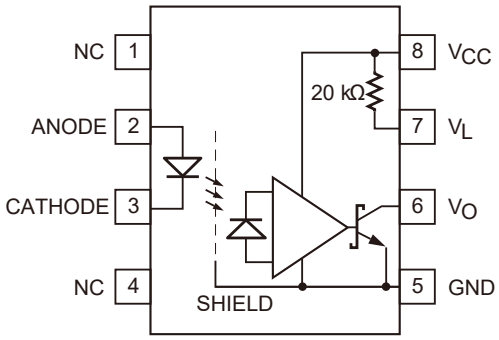
2.Features

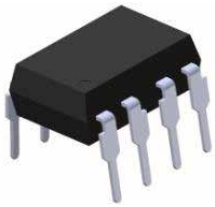
- High speed 1Mbit/s
- High isolation voltage between input and output (Viso=5000 Vrms)
- Guaranteed performance from 0°C to 70°C
- Wide operating temperature range of -40°C to 100°C
- Pb free and RoHS compliant
- CTR > 44% at I_F=10mA

3.Applications

- IPM isolation
- Isolated IGBT/MOSFET gate drive
- AC and brushless DC motor drives
- Industrial inverters

4.Pinning Information





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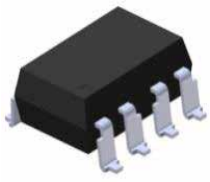

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Truth Table

LED	V_O
OFF	LOW
ON	HIGH

A 0.1-μF bypass capacitor must be connected between pins V_{CC} and V_{EE}.

5.Absolute Maximum Ratings T_A= 25°C

Parameter		Symbol	Value	Units
Input	Forward current	I_F	25	mA
	Peak forward current (50% duty, 1ms P.W)	I_{FP}	50	mA
	Peak transient current (≤1μs P.W,300pps)	I_{Ftrans}	1	A
	Reverse voltage	V_R	5	V
	Power dissipation	P_{IN}	45	mW
Output	Power dissipation *1	P_O	100	mW
	Average Output current	$I_{O(AVG)}$	8	mA
	Peak Output current	$I_{IO(PK)}$	16	mA
	Output voltage	V_O	-0.5 to 30	V
	Supply voltage	V_{CC}	-0.5 to 30	V
Total Power Dissipation		P_{TOT}	145	mW
Isolation Voltage *2		V_{ISO}	5000	V_{rms}
Operating Temperature		T_{OPR}	-40 to 100	°C
Storage Temperature		T_{STG}	-55 to 125	°C
Soldering Temperature *3		T_{SOL}	260	°C

*1 Derate linearly above 90°C free-air temperature at a rate of 3.0 mW/°C.

*2 AC for 1 minute, R.H.=40 ~ 60% R.H. In this test, pins 1,2,3 & 4 are shorted together,and pins 5,6,7 & 8 are shorted together.

*3 For 10 seconds.

6.Electrical Characteristics (T_A=0 to 70°C unless specified otherwise)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input						
Forward Voltage	V_F	I_F=16mA		1.45	1.7	V
Reverse Voltage	B_{VR}	I_R=10μA	5	20		V
Temperature coefficient of forward voltage	$\Delta V_F/\Delta T_A$	I_F=16mA		-1.6		mV/°C
Output						
Logic High Supply Current [1]	I_{CCH}	V_F=0.8V, V_O=Open		0.6	1.2	mA
Logic Low Supply Current [1]	I_{CCL}	I_F=10mA, V_O=Open		0.6	1.2	mA
Transfer						
Logic High Output Current	I_{OH}	V_F=0.8V		6	45	μA
Logic Low Output Voltage	VOL	I_F=10mA, V_{CC}=4.5V,I_O=2.4mA		0.1	0.6	V
Input Threshold Current [1]	I_{TH}	V_O=0.8V,I_O=0.75mA		1.5	5	mA
Low Level Output Current	I_{OL}	I_F=10mA, V_O=0.6V		4.4	9	mA
Current Transfer Ratio [2]	CTR	I_F=10mA, V_{CC}=4.5V, I_O=0.6V	44	90		%
Isolation Voltage	V_{ISO}	RH<50%, T_A=25°C, I_{I-O}≤50μA	5000			V_{RMS}

7.Switching Characteristics

(T_A=0 to 70°C unless specified otherwise, I_F=10mA, V_{CC}=5V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Propagation Delay Time to Logic Low at Output [3,4,1]	T_{PHL}	$I_{F(on)}$=10mA, $V_{F(off)}$=0.8V		20	200	400	ns
Propagation Delay Time to High Output Level [3,4,1]	T_{PLH}	V_{CC}=15.0V, C_L=100pF,		220	450	650	ns
Pulse Width Distortion [5]	PWD	V_{THLH}=2V, V_{THHL}=1.5V			250	500	ns
Output High Level Common Mode Transient Immunity [6]	$\|CM_H\|$	I_F=0mA V_O>3V	V_{CC}=15V, C_L=100pF V_{CM}=1500Vp-p, T_A=25°C		30		kV/μs
Output Low Level Common Mode Transient Immunity [7]	$\|CM_L\|$	I_F=16mA V_O<1V			30		kV/μs

1. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 can improve performance by filtering power supply line noise.
2. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current (I_O) to the forward LED input current (I_F) times 100.
3. Pulse: f = 20 kHz, Duty Cycle = 10%.
4. The R_L = 20 kΩ, C_L = 100 pF load represents a typical IPM (Intelligent Power Module) load.
5. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given device.
6. Common mode transient immunity in a Logic High level is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 3.0 V).
7. Common mode transient immunity in a Logic Low level is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic Low state (i.e.,V_O<1.0V).

8.Typical Characteristic

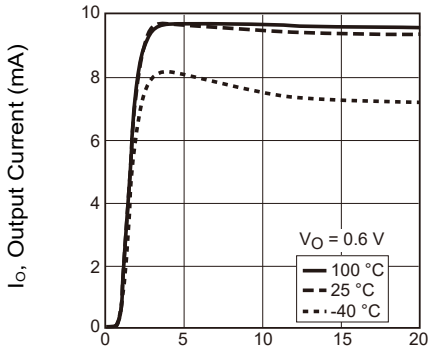


Figure 1: Typical Transfer Characteristics

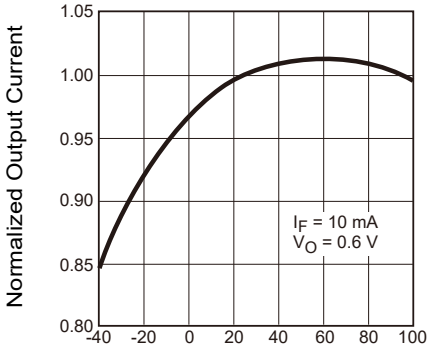


Figure 2: Normalized Output Current vs. Temperature

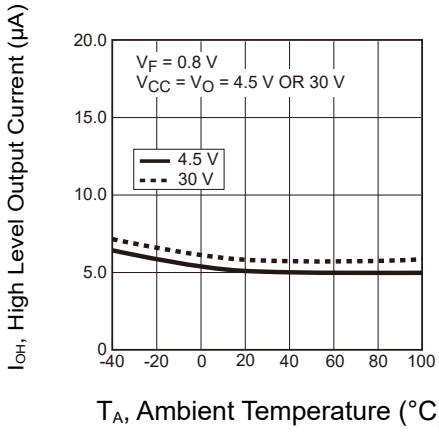


Figure 3: High Level Output Current vs. Temperature

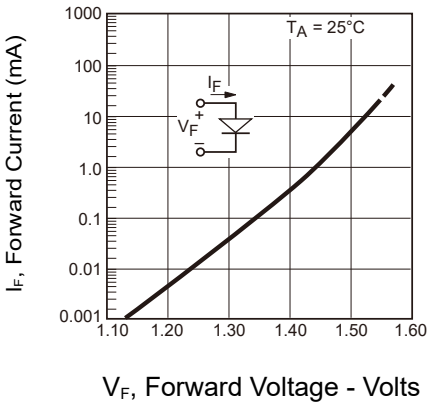


Figure 4: Forward Voltage

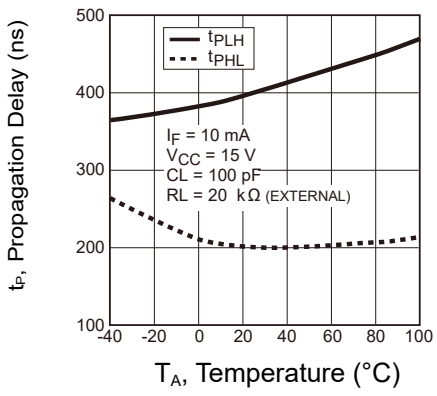


Figure 5: Propagation Delay with External 20kΩ R_L vs. Temperature

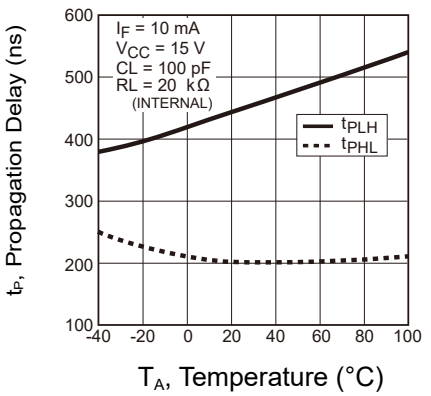


Figure 6: Propagation Delay with Internal 20kΩ R_L vs. Temperature

9.Test Circuit

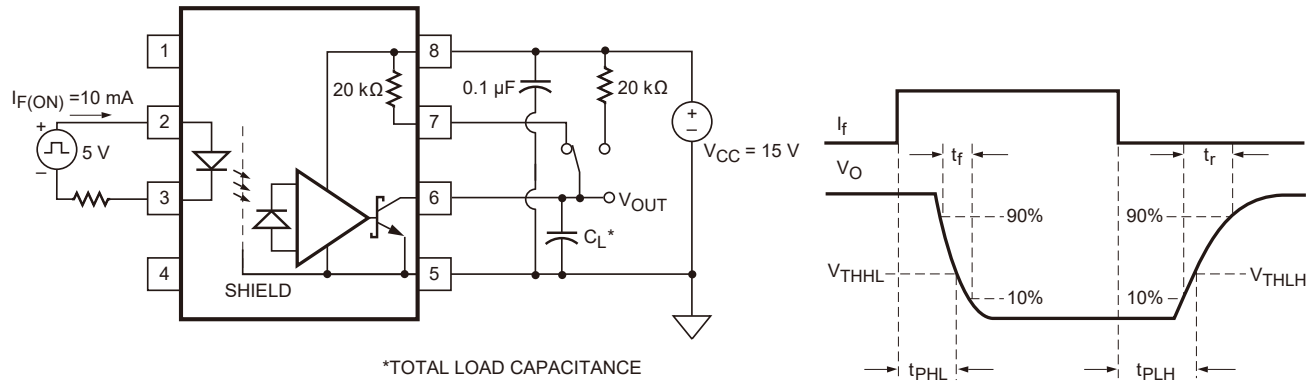


Figure 7: Propagation Delay Test Circuit

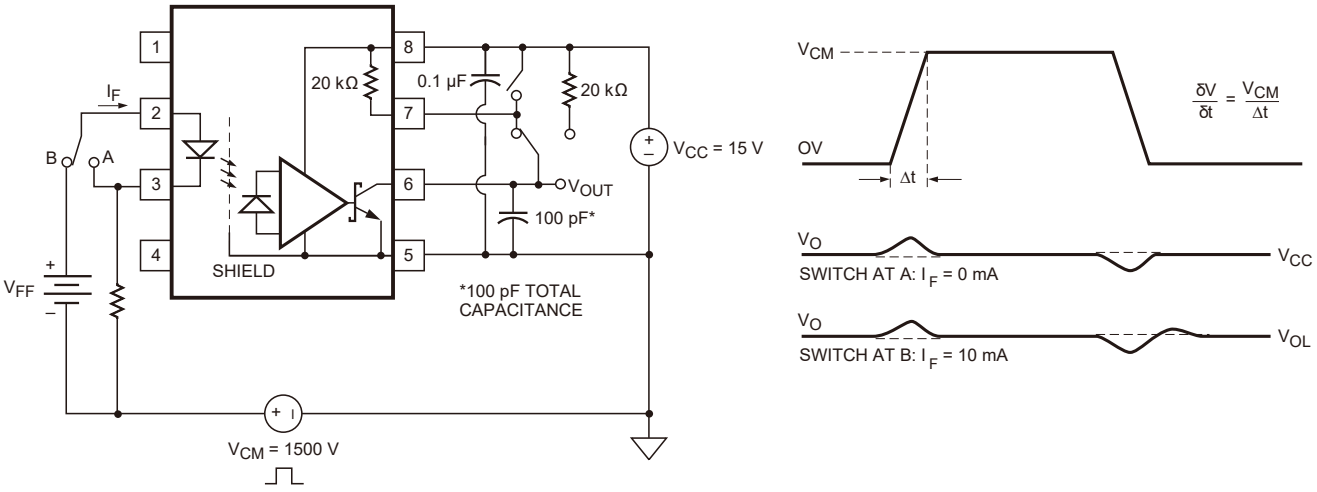
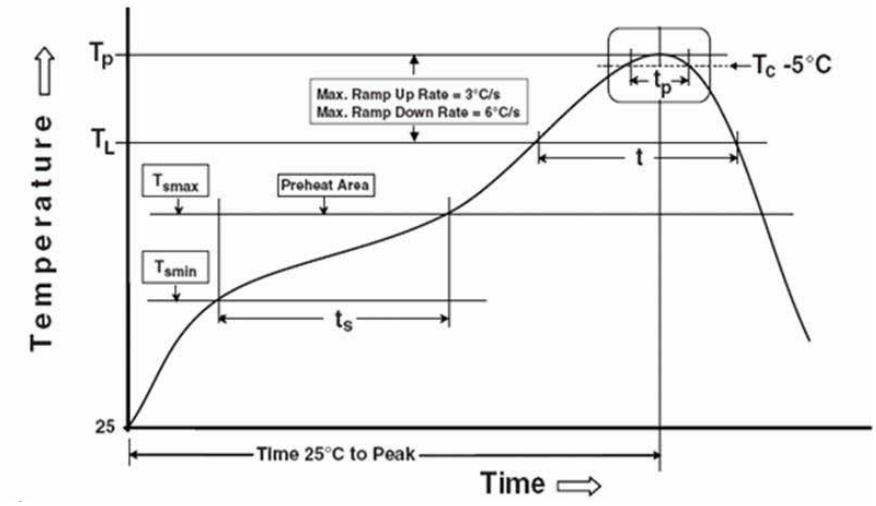


Figure 8: CMR Test Circuit, Typical CMR Waveform

10.Precautions for Use

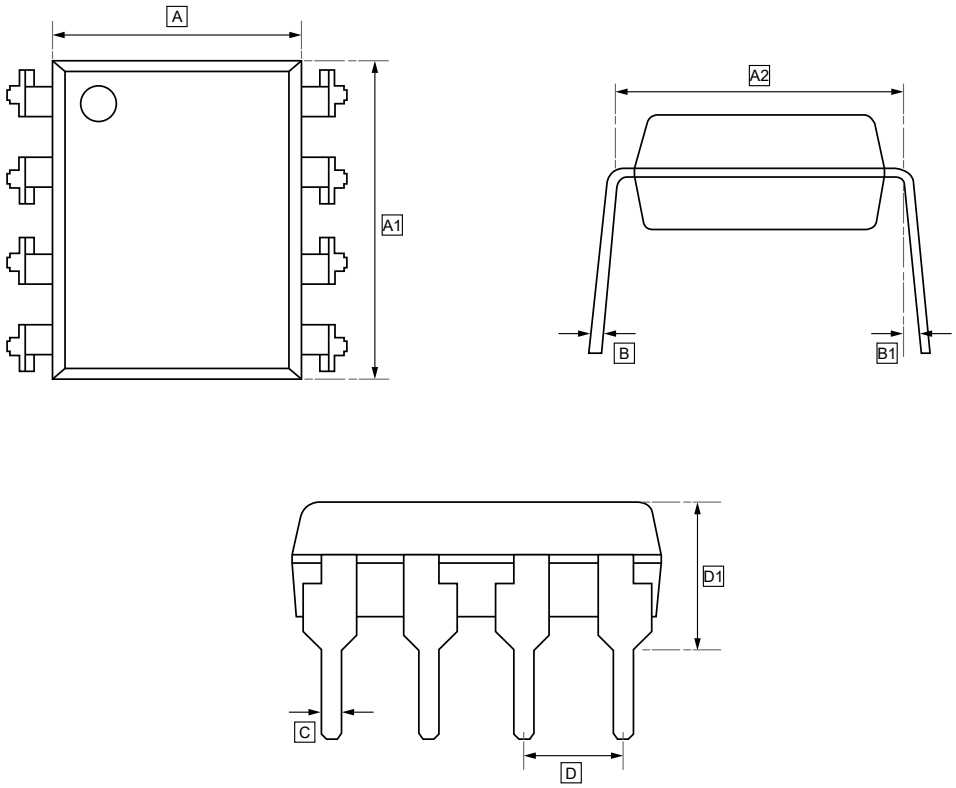


1. Soldering Condition

1.1 (A) Maximum Body Case Temperature Profile for evaluation of Reflow Profile

Preheat	
Temperature min (T_{smin})	150°C
Temperature max (T_{smax})	200°C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3°C/second max
Other	
Liquidus Temperature (T_L)	216°C
Time above Liquidus Temperature (t_L)	60-100 sec
Peak Temperature (T_p)	260°C
Time within 5°C of Actual Peak Temperature: T_p - 5°C	30s
Ramp- Down Rate from Peak Temperature	6°C /second max
Time 25°C to peak temperature	8 minutes max
Reflow times	3 times

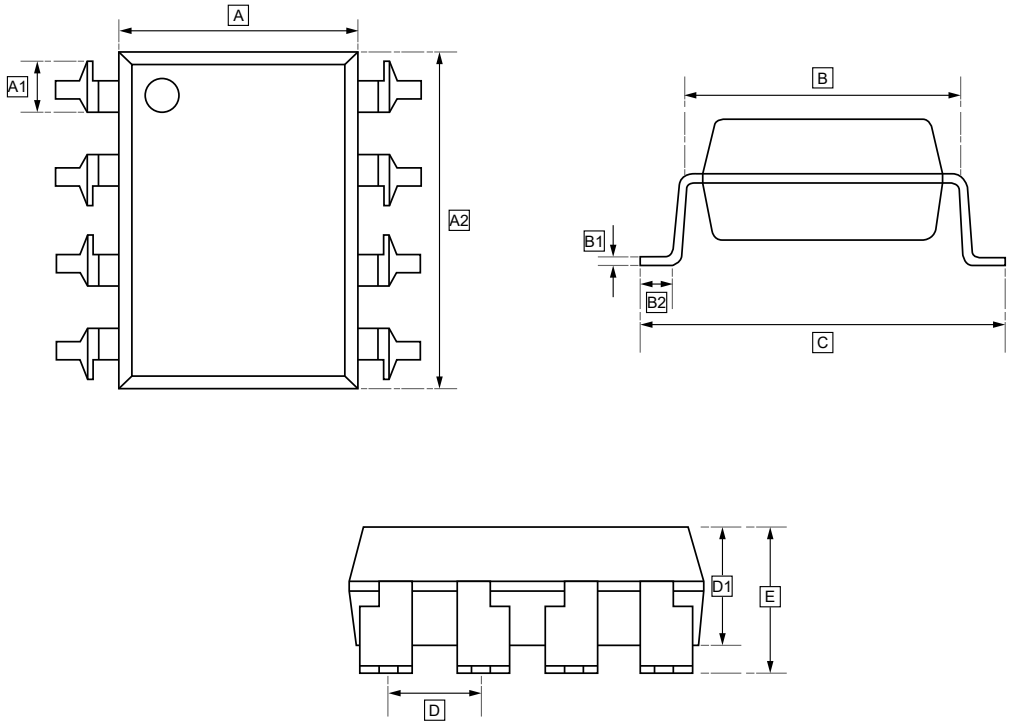
11.1 DIP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	B	B1	C	D	D1
Min	6.30	9.46	7.62	0.25	5°	0.40	2.54	4.20
Max	6.90	10.06	TYP.		15°	0.60	TYP.	4.80

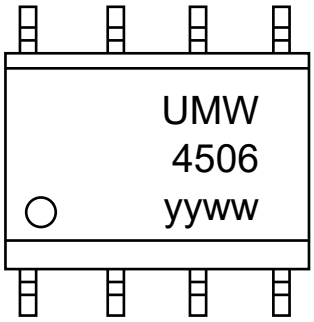
11.2 SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	B	B1	B2	C	D	D1	E
Min	6.30	1.45	9.46	7.62	0.25	0.6	-	2.54	3.20	4.00
Max	6.90		10.06	TYP		-	10.3	TYP	3.80	4.60

12.Ordering Information



yy: Year Code
ww: Week Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW HCPL-4506-000E	4506	DIP-8	2250	Tube and box
UMW HCPL-4506-500E	4506	SOP-8	1000	Tape and reel

13.Disclaimer

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