

TSK60N50M

500V N-Channel MOSFET

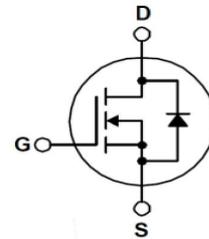
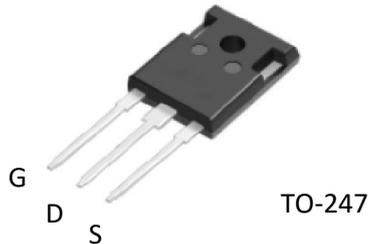
General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Features

60A,500V,Max.RDS(on)=0.095Ω
@ VGS =10V

- ◆ Drain-Source breakdown voltage: BVDSS=500V (Min.)
- ◆ Low drain-source On resistance: RDS(on)=122mΩ (Max.)
- ◆ 100% avalanche tested
- ◆ RoHS compliant device



Absolute Maximum Ratings T_c=25°C unless otherwise specified

Symbol	Parameter	Value	Units
V _{DSS}	Drain-Source Voltage	500	V
V _{GS}	Gate-Source Voltage	±30	V
I _D	Drain Current *	T _C = 25°C	60
		T _C = 100°C	40
I _{DM}	Pulsed Drain Current *	240	A
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	2569	mJ
I _{AR}	Repetitive avalanche current (Note 2)	68	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	100	mJ
P _D	Power Dissipation (T _C = 25°C)	1000	W
T _J	Junction temperature	150	°C
T _{stg}	Storage temperature range	-55~150	°C

* Limited only maximum junction temperature

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Thermal Resistance, Junction-to-Case	--	0.125	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

Electrical Characteristics $T_c=25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}$, $I_D = 30\text{ A}$	--	0.088	0.095	Ω
R_g	Internal gate resistance	Open drain, $f=1\text{ MHz}$	--	0.8	--	Ω

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	500	--	--	V
I_{DSS}	Drain-source cut-off current	$V_{DS}=500\text{ V}$, $V_{GS} = 0\text{ V}$	--	--	25	μA
		$V_{DS}=500\text{ V}$, $T_c=125\text{ }^\circ\text{C}$	--	--	100	μA
I_{GSS}	Gate leakage current	$V_{DS}=0\text{ V}$, $V_{GS}=\pm 20\text{ V}$	--	--	± 250	Na

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$	--	9592	--	pF
C_{oss}	Output Capacitance		--	728	--	pF
C_{rss}	Reverse Transfer Capacitance		--	68	--	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Time (Note 3,4)	$V_{DD}=250\text{ V}$, $I_D = 60\text{ A}$, $R_G = 25\text{ }\Omega$	--	102	--	ns
t_r	Turn-On Rise Time (Note 3,4)		--	56	--	ns
$t_{d(off)}$	Turn-Off Delay Time (Note 4,5)		--	476	--	ns
t_f	Turn-Off Fall Time (Note 3,4)		--	79	--	ns
Q_g	Total Gate Charge (Note 3,4)	$V_{DS}=400\text{ V}$, $I_D = 60\text{ A}$, $V_{GS} = 10\text{ V}$	--	193	--	nC
Q_{gs}	Gate-Source Charge (Note 3,4)		--	43	--	nC
Q_{gd}	Gate-Drain Charge (Note 3,4)		--	63	--	nC

Source-Drain Diode Maximum Ratings and Characteristics

I_S	Continuous Source-Drain Diode Forward Current	--	--	60	A	
I_{SM}	Pulsed Source-Drain Diode Forward Current	--	--	240		
V_{SD}	Source-Drain Diode Forward Voltage	$I_S=60\text{ A}$, $V_{GS} = 0\text{ V}$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$I_S=50\text{ A}$, $V_{GS} = 0\text{ V}$ $di_p/dt = 100\text{ A}/\mu\text{s}$ (Note 3, 4)	--	602	--	ns
Q_{rr}	Reverse Recovery Charge		--	6.35	--	μC

NOTES:

1. Repeated rating: Pulse width limited by safe operating area
2. $L=1\text{ mH}$, $I_{AS}=68\text{ A}$, $V_{DD}=50\text{ V}$, $R_G=25\text{ }\Omega$, Starting $T_J=25\text{ }^\circ\text{C}$
3. Pulse test: Pulse width $\leq 300\text{ }\mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

Typical Characteristics Curve

Fig. 1 Typical Output Characteristics

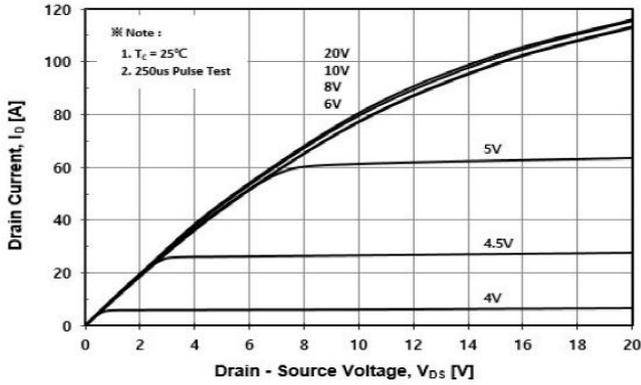


Fig. 2 Typical Transfer Characteristics

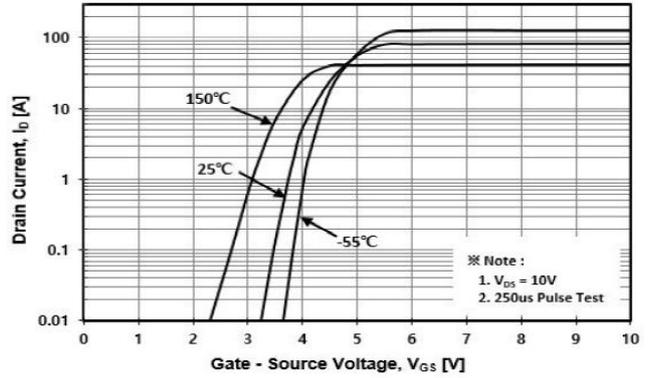


Fig.3 On-Resistance Variation with Drain Current and Gate Voltage

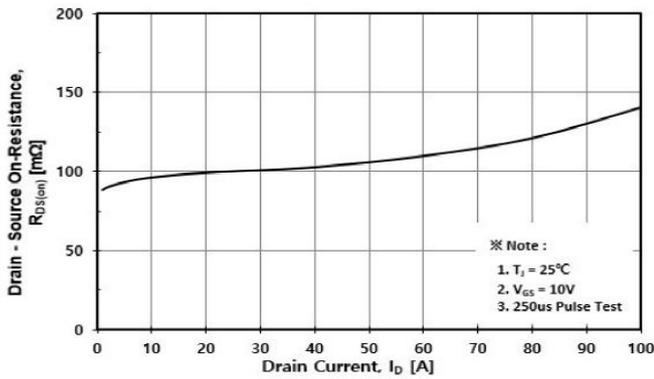


Fig. 4 Body Diode Forward Voltage Variation with Source Current

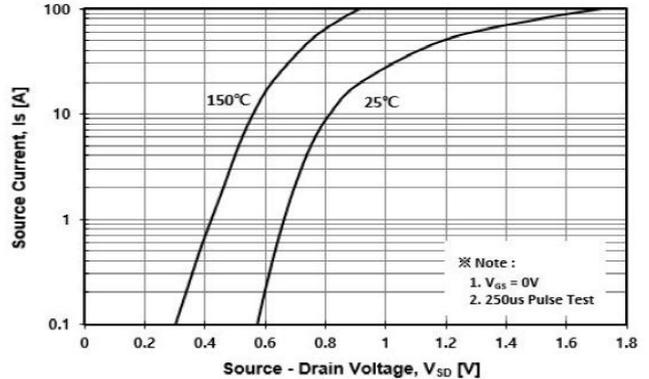


Fig. 5 Typical Capacitance Characteristics

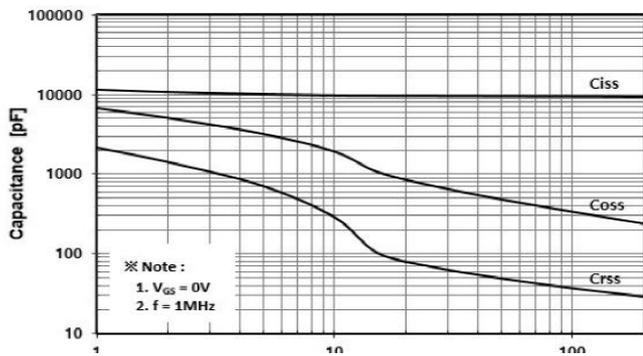
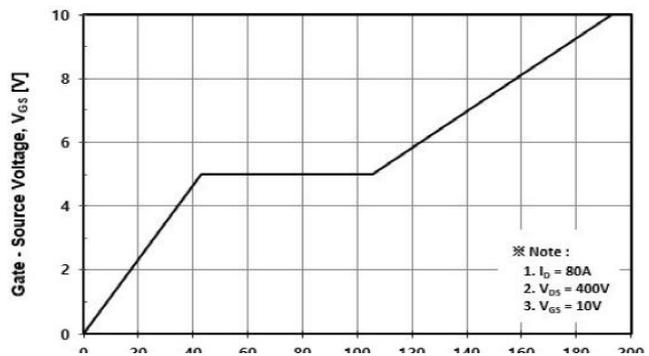


Fig. 6 Typical Total Gate Charge Characteristics



Typical Characteristics Curve (Continue)

Fig. 7 Breakdown Voltage Variation vs. Temperature

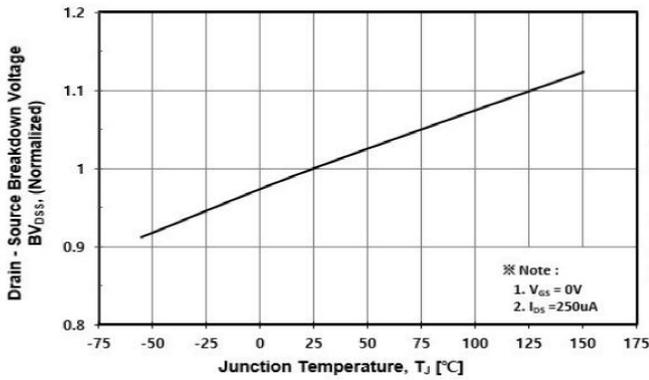


Fig. 8 On-Resistance Variation vs. Temperature

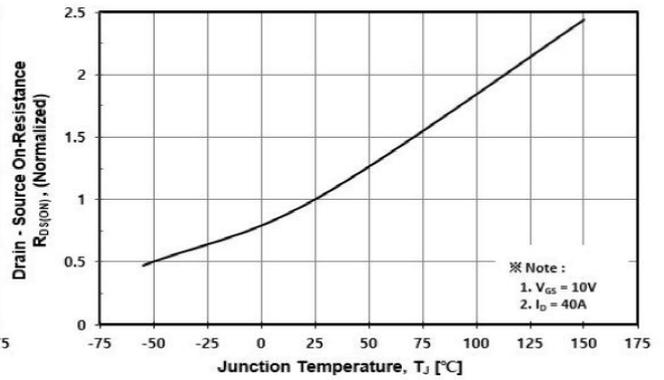


Fig. 9 Maximum Drain Current vs. Case Temperature

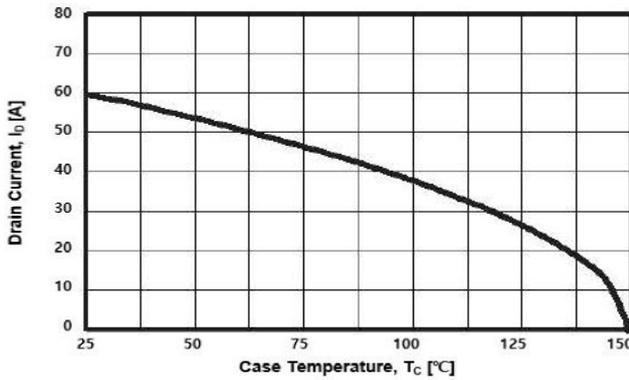


Fig. 10 Maximum Safe Operating Area

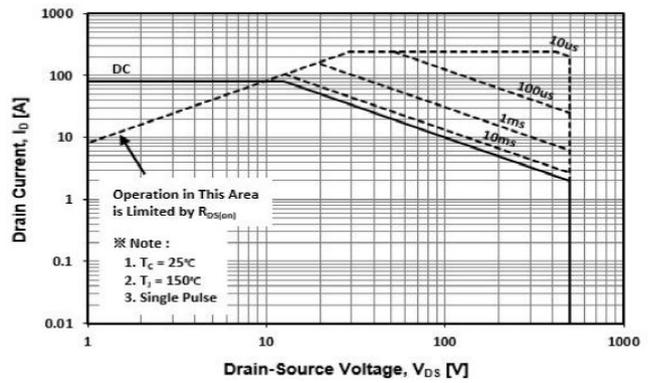


Fig. 11 Transient Thermal Impedance

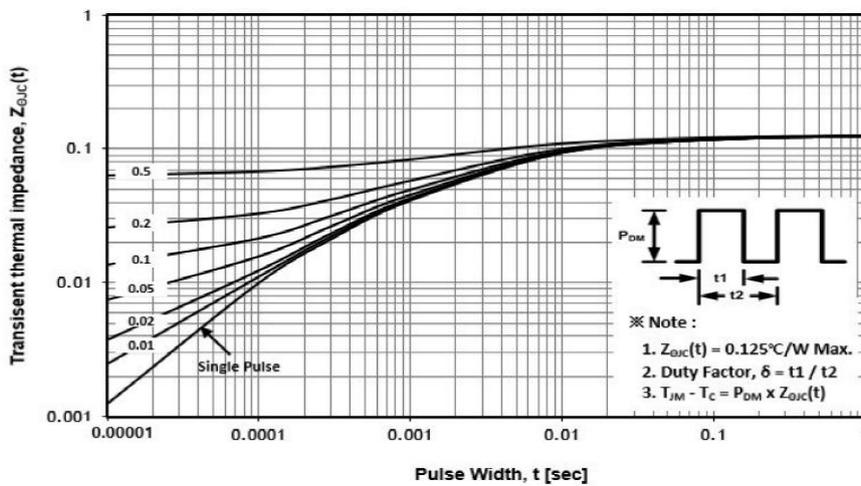


Fig. 12 Gate Charge Test Circuit & Waveform

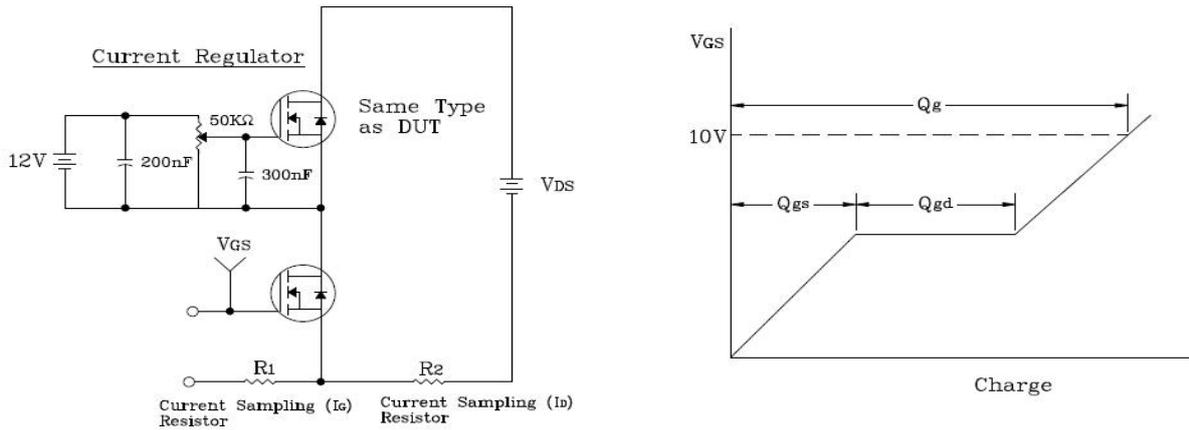


Fig. 13 Resistive Switching Test Circuit & Waveform

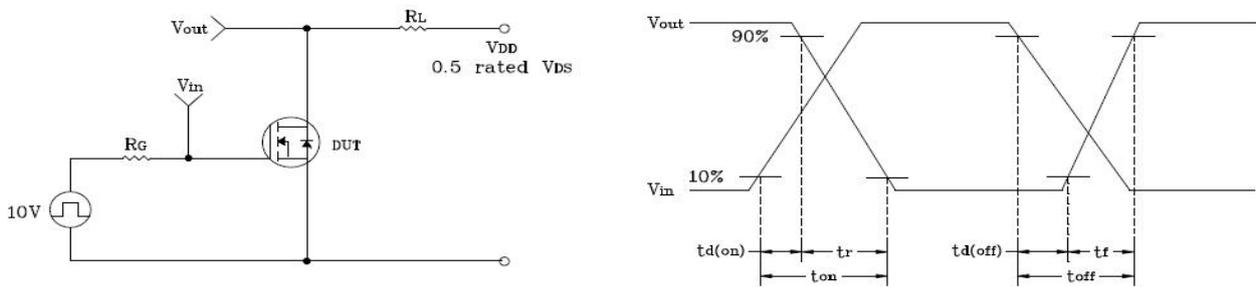


Fig. 14 EAS Test Circuit & Waveform

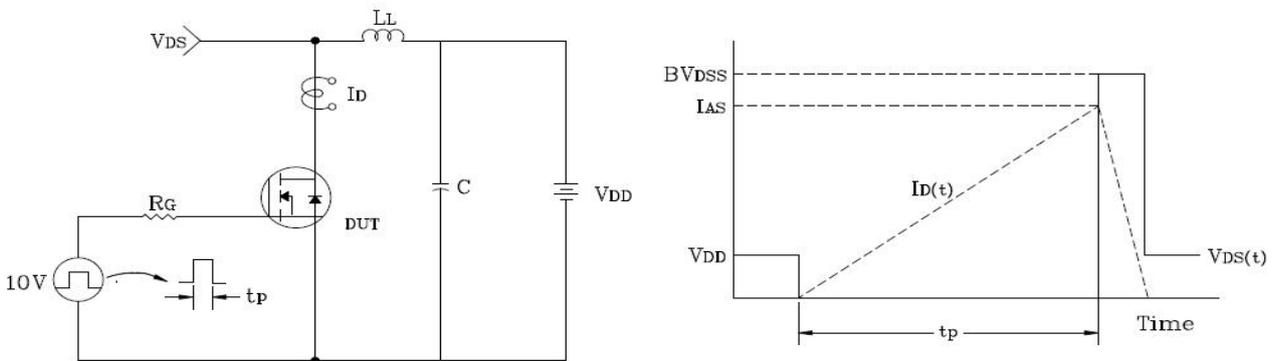


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform

