

1. General Description

The 74LVC4245 is an octal dual supply translating transceiver featuring 3-state bus compatible outputs in both send and receive directions. It is designed to interface between a 3 V and 5 V bus in a mixed 3 V and 5 V supply environment. The device features an output enable input (\overline{OE}) and a send/receive input (DIR) for direction control. A HIGH on \overline{OE} causes the outputs to assume a high-impedance OFF-state, effectively isolating the buses. In suspend mode, when either supply is zero, there is no current path between supplies. $V_{CCA} \geq V_{CCB}$, except in suspend mode. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

2. Features and Benefits

- Wide supply voltage range
 - $V_{CC(A)}$: 1.2 V to 5.5 V
 - $V_{CC(B)}$: 1.2 V to 5.5 V
- High noise immunity
- Complies with JEDEC standards:
 - JESD8-7 (1.2 V to 1.95 V)
 - JESD8-5 (1.8 V to 2.7 V)
 - JESD8C (2.7 V to 3.6 V)
 - JESD36 (4.5 V to 5.5 V)
- Suspend mode
- Latch-up performance exceeds 250 mA
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- Inputs accept voltages up to 5.5 V
- Low power consumption: 30 μ A maximum I_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- ESD protection:

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Octal dual supply translating transceiver; 3-state

Draft datasheet, Rev. 1.0

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- HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2500 V
- CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options

3. Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
74LVC4245APW	TSSOP-24L	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	2500

4. Function Diagram

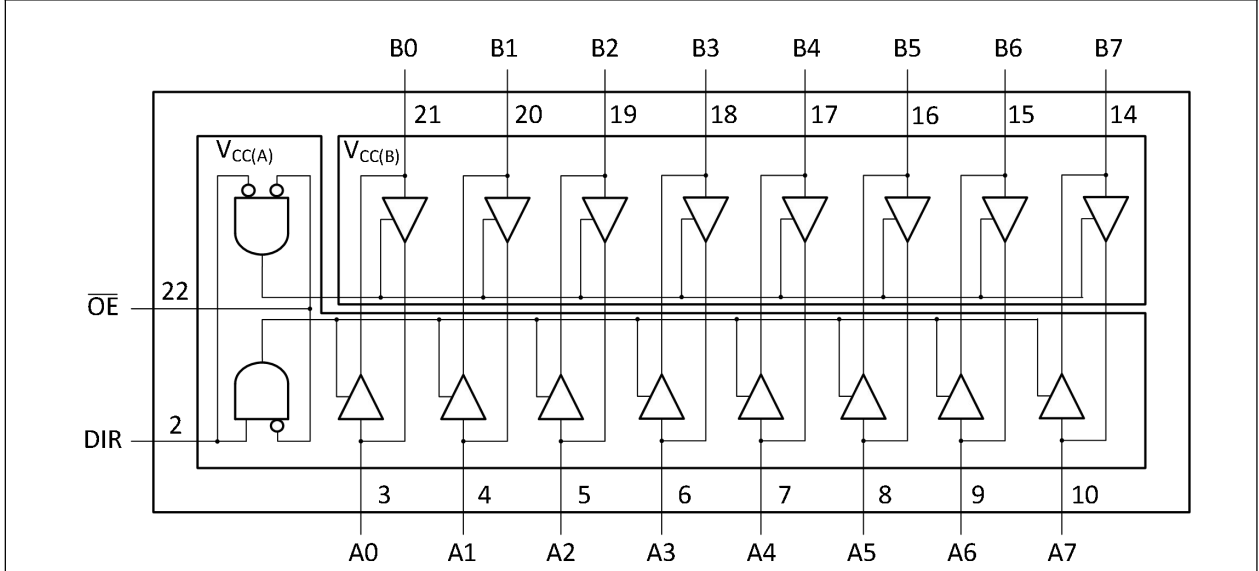


Fig. 1. Logic symbol

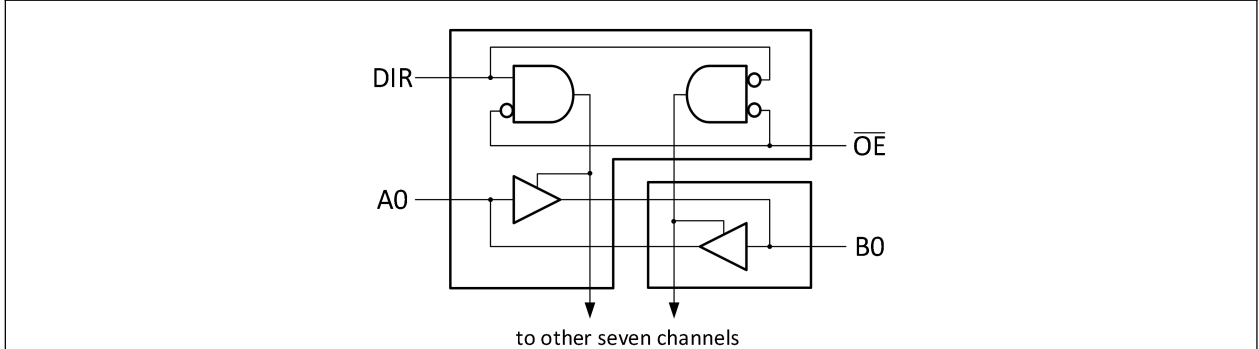
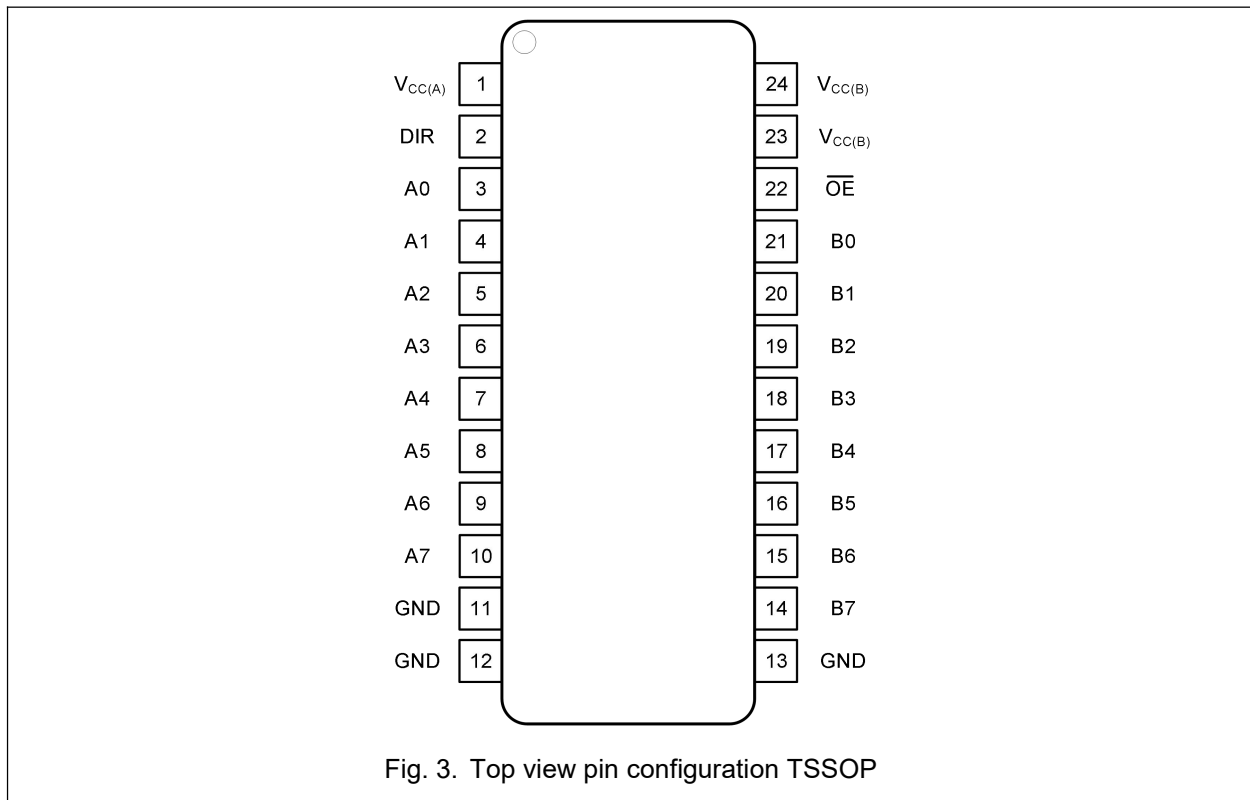


Fig. 2. Logic diagram (one channel)

5. Pinning Information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{CC(A)}$	1	Supply voltage A (An inputs/outputs, \overline{OE} and DIR inputs are referenced to $V_{CC(A)}$)
DIR	2	Direction control
A0, A1, A2, A3, A4, A5, A6, A7	3, 4, 5, 6, 7, 8, 9, 10	Data input or output
GND [1]	11, 12, 13	Ground (0 V)
B0, B1, B2, B3, B4, B5, B6, B7	21, 20, 19, 18, 17, 16, 15, 14	Data input or output
\overline{OE}	22	Output enable input (active LOW)
$V_{CC(B)}$	23, 24	Supply voltage B (Bn inputs/outputs are referenced to $V_{CC(B)}$)

[1] All GND pins must be connected to ground (0V).

6. Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Supply voltage	Input		Input/output	
	\overline{OE} [2]	DIR [2]	An [2]	Bn [2]
1.2 V to 5.5 V	L	L	A = B	input
1.2 V to 5.5 V	L	H	input	B = A
1.2 V to 5.5 V	H	X	Z	Z
GND [1]	X	X	Z	Z

[1] If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

[2] The An inputs/outputs, DIR and OE input circuit is referenced to $V_{CC(A)}$; The Bn inputs/outputs circuit is referenced to $V_{CC(B)}$.

7. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 4. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	6.5	V
$V_{CC(B)}$	supply voltage B		-0.5	6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50		mA
V_I	input voltage	[1]	-0.5	6.5	V
I_{OK}	output clamping current	$V_O < 0$ V	-50		mA
V_O	output voltage	Active mode [1][2][3]	-0.5	$V_{CCO} + 0.5$	V
		Suspend or 3-state mode [1]	-0.5	6.5	V
I_O	output current	$V_O = 0$ V to V_{CCO} [2]		± 50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$; per V_{CC} pin		100	mA
I_{GND}	ground current	per GND pin	-100		mA
P_{tot}	total power dissipation			500	mW
T_{stg}	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] $V_{CCO} + 0.5$ V should not exceed 6.5 V.

8. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. MDD does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.2	5.5	V
$V_{CC(B)}$	supply voltage B		1.2	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	Active mode [1]	0	V_{CCO}	V
		Suspend or 3-state mode	0	5.5	V
T_{amb}	ambient temperature		-40	125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CCI} = 1.2 \text{ V}$ [2]		20	ns/V
		$V_{CCI} = 1.4 \text{ V to } 1.95 \text{ V}$		20	ns/V
		$V_{CCI} = 2.3 \text{ V to } 2.7 \text{ V}$		20	ns/V
		$V_{CCI} = 3 \text{ V to } 3.6 \text{ V}$		10	ns/V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		5	ns/V

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the input port.

9. Static Characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V). Typical values measured at $T_{amb} = 25^{\circ}\text{C}$ (unless otherwise noted).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IH}	HIGH-level input voltage	data input [1]						
		$V_{CCI} = 1.2\text{ V}$	$0.8V_{CCI}$			$0.8V_{CCI}$		V
		$V_{CCI} = 1.4\text{ V to }1.95\text{ V}$	$0.65V_{CCI}$			$0.65V_{CCI}$		V
		$V_{CCI} = 2.3\text{ V to }2.7\text{ V}$	1.7			1.7		V
		$V_{CCI} = 3\text{ V to }3.6\text{ V}$	2.2			2.2		V
		$V_{CCI} = 4.5\text{ V to }5.5\text{ V}$	$0.7V_{CCI}$			$0.7V_{CCI}$		V
		DIR, \overline{OE} input						
		$V_{CCI} = 1.2\text{ V}$	$0.8V_{CC(A)}$			$0.8V_{CC(A)}$		V
		$V_{CCI} = 1.4\text{ V to }1.95\text{ V}$	$0.65V_{CC(A)}$			$0.65V_{CC(A)}$		V
		$V_{CCI} = 2.3\text{ V to }2.7\text{ V}$	1.7			1.7		V
		$V_{CCI} = 3\text{ V to }3.6\text{ V}$	2.0			2.0		V
		$V_{CCI} = 4.5\text{ V to }5.5\text{ V}$	$0.7V_{CC(A)}$			$0.7V_{CC(A)}$		V
V_{IL}	LOW-level input voltage	data input [1]						
		$V_{CCI} = 1.2\text{ V}$			$0.2V_{CCI}$		$0.2V_{CCI}$	V
		$V_{CCI} = 1.4\text{ V to }1.95\text{ V}$			$0.35 V_{CCI}$		$0.35 V_{CCI}$	V
		$V_{CCI} = 2.3\text{ V to }2.7\text{ V}$			0.7		0.7	V
		$V_{CCI} = 3\text{ V to }3.6\text{ V}$			0.8		0.8	V
		$V_{CCI} = 4.5\text{ V to }5.5\text{ V}$			$0.3V_{CCI}$		$0.3V_{CCI}$	V
		DIR, \overline{OE} input						
		$V_{CCI} = 1.2\text{ V}$			$0.2V_{CC(A)}$		$0.2V_{CC(A)}$	V
		$V_{CCI} = 1.4\text{ V to }1.95\text{ V}$			$0.35 V_{CC(A)}$		$0.35 V_{CC(A)}$	V
		$V_{CCI} = 2.3\text{ V to }2.7\text{ V}$			0.7		0.7	V
		$V_{CCI} = 3\text{ V to }3.6\text{ V}$			0.8		0.8	V
		$V_{CCI} = 4.5\text{ V to }5.5\text{ V}$			$0.3V_{CC(A)}$		$0.3V_{CC(A)}$	V

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Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
V _{OH}	HIGH-level output voltage	V _I = V _{IH}						
		I _O = -100 μA; V _{CCO} = 1.2 V to 4.5 V	V _{CCO} - 0.1			V _{CCO} - 0.1		V
		I _O = -3 mA; V _{CCO} = 1.4 V	1.0			1.0		V
		I _O = -8 mA; V _{CCO} = 1.65 V	1.2			1.2		V
		I _O = -12 mA; V _{CCO} = 2.3 V	1.9			1.9		V
		I _O = -24 mA; V _{CCO} = 3.0 V	2.4			2.4		V
		I _O = -32 mA; V _{CCO} = 4.5 V	3.8			3.8		V
V _{OL}	LOW-level output voltage	V _I = V _{IL}						
		I _O = 100 μA; V _{CCO} = 1.2 V to 4.5 V			0.1		0.1	V
		I _O = 3 mA; V _{CCO} = 1.4 V			0.3		0.3	V
		I _O = 8 mA; V _{CCO} = 1.65 V			0.45		0.45	V
		I _O = 12 mA; V _{CCO} = 2.3 V			0.3		0.3	V
		I _O = 24 mA; V _{CCO} = 3.0 V			0.55		0.55	V
		I _O = 32 mA; V _{CCO} = 4.5 V			0.55		0.55	V
I _I	input leakage current	DIR, \overline{OE} input; V _I = 0 V to 5.5 V ; V _{CCI} = 1.2 V to 5.5 V			±2		±10	μA
I _{OZ}	OFF-state output current	A or B port; V _O = 0 V or V _{CCO} ; V _{CCO} = 1.2 V to 5.5 V [2]			±2		±10	μA
		suspend mode A port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = 5.5 V; V _{CC(B)} = 0 V [2]			±2		±10	μA
		suspend mode B port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = 0 V; V _{CC(B)} = 5.5 V [2]			±2		±10	μA
I _{OFF}	power-off leakage current	A port; V _I or V _O = 0 V to 5.5 V; V _{CC(A)} = 0 V; V _{CC(B)} = 1.2 V to 5.5 V			±2		±10	μA
		B port; V _I or V _O = 0 V to 5.5 V;			±2		±10	μA



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		$V_{CC(B)} = 0\text{ V}; V_{CC(A)} = 1.2\text{ V to } 5.5\text{ V}$						
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Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
I_{CC}	supply current	A port; $V_I = 0\text{ V}$ or V_{CCI} ; $I_O = 0\text{ A}$ [1]						
		$V_{CC(A)}, V_{CC(B)} = 1.2\text{V to } 5.5\text{V}$			15		20	μA
		$V_{CC(A)} = 5.5\text{V}; V_{CC(B)} = 0\text{V}$			15		20	μA
		$V_{CC(A)} = 0\text{V}; V_{CC(B)} = 5.5\text{V}$	-2			-4		μA
		B port; $V_I = 0\text{ V}$ or V_{CCI} ; $I_O = 0\text{ A}$						
		$V_{CC(A)}, V_{CC(B)} = 1.2\text{V to } 5.5\text{V}$			15		20	μA
		$V_{CC(B)} = 0\text{V}; V_{CC(A)} = 5.5\text{V}$	-2			-4		μA
		$V_{CC(B)} = 5.5\text{V}; V_{CC(A)} = 0\text{V}$			15		20	μA
		A plus B port ($I_{CC(A)} + I_{CC(B)}$); $I_O = 0\text{ A}; V_I = 0\text{ V}$ or V_{CCI}						
		$V_{CC(A)}, V_{CC(B)} = 1.2\text{V to } 5.5\text{V}$			25		30	μA
ΔI_{CC}	additional supply current	per input; $V_{CC(A)}, V_{CC(B)} = 3.0\text{V to } 5.5\text{V}$						
		DIR and \overline{OE} input; DIR or \overline{OE} input at $V_{CC(A)} - 0.6\text{V}$; A port at $V_{CC(A)}$ or GND; B port = open			50		75	μA
		A port; A port at $V_{CC(A)} - 0.6\text{ V}$; DIR at $V_{CC(A)}$; B port = open [4]			50		75	μA
		B port; B port at $V_{CC(B)} - 0.6\text{ V}$; DIR at $V_{CC(B)}$; A port = open [4]			50		75	μA

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] To guarantee the node switches, an external driver must source/sink at least I_{BHLO} / I_{BHHO} when the input is in the range V_{IL} to V_{IH} .

[4] For non bus hold parts only (74LVC4245).

10. Dynamic Characteristics

Table 7. Dynamic characteristics for temperature range -40 °C to +85 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6. for waveforms see Fig. 3 and Fig. 4. [1]

Symbol	Parameter	Conditions	$V_{CC(B)}$										Unit
			1.5V±0.1V		1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)} = 1.5 V \pm 0.1 V$													
t_{pd}	propagation time	An to Bn	0.9	43.2	0.9	39.2	0.8	36.3	0.7	35.1	0.7	35.1	ns
		Bn to An	0.9	43.2	0.9	39.2	0.8	36.3	0.7	35.1	0.7	35.1	ns
t_{dis}	disable time	\overline{OE} to An	1.5	72.5	1.5	72.5	1.5	72.5	1.5	72.5	1.4	72.5	ns
		\overline{OE} to Bn	1.5	72.5	1.5	72.5	1.5	72.5	1.5	72.5	1.4	72.5	ns
t_{en}	enable time	\overline{OE} to An	0.4	92.2	0.4	92.2	0.4	92.2	0.4	92.2	0.4	92.2	ns
		\overline{OE} to Bn	0.4	92.2	0.4	92.2	0.4	92.2	0.4	92.2	0.4	92.2	ns
$V_{CC(A)} = 1.8 V \pm 0.15 V$													
t_{pd}	propagation time	An to Bn	0.9	38.6	0.9	30.5	0.8	26.9	0.7	26.3	0.7	25.8	ns
		Bn to An	0.9	38.6	0.9	30.5	0.8	26.9	0.7	26.3	0.7	25.8	ns
t_{dis}	disable time	\overline{OE} to An	1.5	46.3	1.5	46.3	1.5	46.3	1.5	46.3	1.4	46.3	ns
		\overline{OE} to Bn	1.5	46.3	1.5	46.3	1.5	46.3	1.5	46.3	1.4	46.3	ns
t_{en}	enable time	\overline{OE} to An	0.4	63.2	0.4	58.1	0.4	54.6	0.4	54.1	0.4	53.1	ns
		\overline{OE} to Bn	0.4	63.2	0.4	58.1	0.4	54.6	0.4	54.1	0.4	53.1	ns
$V_{CC(A)} = 2.5 V \pm 0.2 V$													
t_{pd}	propagation time	An to Bn	1.2	33.0	1.2	24.7	1.0	19.7	1.0	18.3	0.9	17.1	ns
		Bn to An	1.2	33.0	1.2	24.7	1.0	19.7	1.0	18.3	0.9	17.1	ns
t_{dis}	disable time	\overline{OE} to An	1.4	25.1	1.4	25.1	1.4	25.1	1.4	25.1	1.4	25.1	ns
		\overline{OE} to Bn	1.4	25.1	1.4	25.1	1.4	25.1	1.4	25.1	1.4	25.1	ns
t_{en}	enable time	\overline{OE} to An	1.0	38.3	1.0	33.1	1.0	29.5	1.0	28.0	1.0	27.0	ns
		\overline{OE} to Bn	1.0	38.3	1.0	33.1	1.0	29.5	1.0	28.0	1.0	27.0	ns
$V_{CC(A)} = 3.3 V \pm 0.3 V$													
t_{pd}	propagation time	An to Bn	0.8	31.2	0.8	22.6	0.8	16.2	0.7	14.5	0.6	13.6	ns
		Bn to An	0.8	31.2	0.8	22.6	0.8	16.2	0.7	14.5	0.6	13.6	ns
t_{dis}	disable time	\overline{OE} to An	1.6	20.2	1.6	20.2	1.6	20.2	1.6	20.2	1.6	20.2	ns
		\overline{OE} to Bn	1.6	20.2	1.6	20.2	1.6	20.2	1.6	20.2	1.6	20.2	ns
t_{en}	enable time	\overline{OE} to An	0.8	31.5	0.8	25.8	0.8	22.4	0.8	21.1	0.8	20.8	ns
		\overline{OE} to Bn	1.8	31.5	0.8	25.8	0.8	22.4	0.8	21.1	0.8	20.8	ns
$V_{CC(A)} = 5.0 V \pm 0.5 V$													
t_{pd}	propagation time	An to Bn	0.7	29.8	0.7	21.3	0.4	14.8	0.3	12.6	0.3	11.2	ns
		Bn to An	0.7	29.8	0.7	21.3	0.4	14.8	0.3	12.6	0.3	11.2	ns
t_{dis}	disable time	\overline{OE} to An	0.3	15.6	0.3	15.6	0.3	15.6	0.3	15.6	0.3	15.6	ns
		\overline{OE} to Bn	0.3	15.6	0.3	15.6	0.3	15.6	0.3	15.6	0.3	15.6	ns
t_{en}	enable time	\overline{OE} to An	0.7	29.1	0.7	21.2	0.7	18.5	0.7	16.8	0.7	15.9	ns
		\overline{OE} to Bn	0.7	29.1	0.7	21.2	0.7	18.5	0.7	16.8	0.7	15.9	ns

 [1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

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Table 8. Dynamic characteristics for temperature range -40 °C to +125 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6. for waveforms see Fig. 3 and Fig. 4. [1]

Symbol	Parameter	Conditions	V _{CC(B)}										Unit
			1.5V±0.1V		1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V_{CC(A)} = 1.5 V ± 0.1 V													
t _{pd}	propagation time	An to Bn	0.9	43.3	0.9	38.9	0.8	36.3	0.7	35.1	0.7	35.1	ns
		Bn to An	0.9	43.3	0.9	38.9	0.8	36.3	0.7	35.1	0.7	35.1	ns
t _{dis}	disable time	$\overline{\text{OE}}$ to An	1.5	74.5	1.5	74.5	1.5	74.5	1.5	74.5	1.4	74.5	ns
		$\overline{\text{OE}}$ to Bn	1.5	74.5	1.5	74.5	1.5	74.5	1.5	74.5	1.4	74.5	ns
t _{en}	enable time	$\overline{\text{OE}}$ to An	0.4	94.2	0.4	94.2	0.4	94.2	0.4	94.2	0.4	94.2	ns
		$\overline{\text{OE}}$ to Bn	0.4	94.2	0.4	94.2	0.4	94.2	0.4	94.2	0.4	94.2	ns
V_{CC(A)} = 1.8 V ± 0.15 V													
t _{pd}	propagation time	An to Bn	0.9	38.4	0.9	30.8	0.8	27.8	0.7	26.4	0.7	25.3	ns
		Bn to An	0.9	38.4	0.9	30.8	0.8	27.8	0.7	26.4	0.7	25.3	ns
t _{dis}	disable time	$\overline{\text{OE}}$ to An	1.5	50.3	1.5	50	1.5	50.2	1.5	50.4	1.4	50.3	ns
		$\overline{\text{OE}}$ to Bn	1.5	50.3	1.5	50	1.5	50.2	1.5	50.4	1.4	50.3	ns
t _{en}	enable time	$\overline{\text{OE}}$ to An	0.4	67.2	0.4	61.8	0.4	58.5	0.4	58.2	0.4	57.1	ns
		$\overline{\text{OE}}$ to Bn	0.4	67.2	0.4	61.8	0.4	58.5	0.4	58.2	0.4	57.1	ns
V_{CC(A)} = 2.5 V ± 0.2 V													
t _{pd}	propagation time	An to Bn	1.2	33.4	1.2	25.4	1.0	19.7	1.0	18.5	0.9	17.3	ns
		Bn to An	1.2	33.4	1.2	25.4	1.0	19.7	1.0	18.5	0.9	17.3	ns
t _{dis}	disable time	$\overline{\text{OE}}$ to An	1.4	29.1	1.4	28.8	1.4	29	1.4	29.2	1.4	29.1	ns
		$\overline{\text{OE}}$ to Bn	1.4	29.1	1.4	28.8	1.4	29	1.4	29.2	1.4	29.1	ns
t _{en}	enable time	$\overline{\text{OE}}$ to An	1.0	42.3	1.0	36.8	1.0	33.4	1.0	32.1	1.0	31.0	ns
		$\overline{\text{OE}}$ to Bn	1.0	42.3	1.0	36.8	1.0	33.4	1.0	32.1	1.0	31.0	ns
V_{CC(A)} = 3.3 V ± 0.3 V													
t _{pd}	propagation time	An to Bn	0.8	32.2	0.8	23.2	0.8	16.8	0.7	15.5	0.6	14.6	ns
		Bn to An	0.8	32.2	0.8	23.2	0.8	16.8	0.7	15.5	0.6	14.6	ns
t _{dis}	disable time	$\overline{\text{OE}}$ to An	1.6	24.2	1.6	23.9	1.6	24.1	1.6	24.3	1.6	24.2	ns
		$\overline{\text{OE}}$ to Bn	1.6	24.2	1.6	23.9	1.6	24.1	1.6	24.3	1.6	24.2	ns
t _{en}	enable time	$\overline{\text{OE}}$ to An	0.8	35.5	0.8	29.5	0.8	26.3	0.8	25.2	0.8	24.8	ns
		$\overline{\text{OE}}$ to Bn	0.8	35.5	0.8	29.5	0.8	26.3	0.8	25.2	0.8	24.8	ns
V_{CC(A)} = 5.0 V ± 0.5 V													
t _{pd}	propagation time	An to Bn	0.7	30.4	0.7	22.1	0.4	15.5	0.3	13.4	0.3	11.9	ns
		Bn to An	0.7	30.4	0.7	22.1	0.4	15.5	0.3	13.4	0.3	11.9	ns
t _{dis}	disable time	$\overline{\text{OE}}$ to An	0.3	19.6	0.3	19.3	0.3	19.5	0.3	19.7	0.3	19.6	ns
		$\overline{\text{OE}}$ to Bn	0.3	19.6	0.3	19.3	0.3	19.5	0.3	19.7	0.3	19.6	ns
t _{en}	enable time	$\overline{\text{OE}}$ to An	0.7	33.1	0.7	24.9	0.7	22.4	0.7	20.9	0.7	19.9	ns
		$\overline{\text{OE}}$ to Bn	0.7	33.1	0.7	24.9	0.7	22.4	0.7	20.9	0.7	19.9	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

Table 9. Typical power dissipation capacitance at $V_{CC(A)} = V_{CC(B)}$ and $T_{amb} = 25\text{ °C}$

Voltages are referenced to GND (ground = 0 V). [1][2]

Symbol	Parameter	Conditions	$V_{CC(A)}$ and $V_{CC(B)}$				Unit
			1.8 V	2.5 V	3.3 V	5.0 V	
C_{PD}	power dissipation capacitance	A port: (direction A to B); B port: (direction B to A)	1	1	1	1	pF
		A port: (direction B to A); B port: (direction A to B)	16	16	17	18	pF

 [1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

 f_i = input frequency in MHz;

 f_o = output frequency in MHz;

 C_L = output load capacitance in pF;

 V_{CC} = supply voltage in V;

 N = number of inputs switching;

 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

 [2] $f_i = 10\text{ MHz}$; $V_I = \text{GND to } V_{CC}$; $t_r = t_f = 1\text{ ns}$; $C_L = 0\text{ pF}$; $R_L = \infty\ \Omega$.

10.1. Waveforms and test circuit

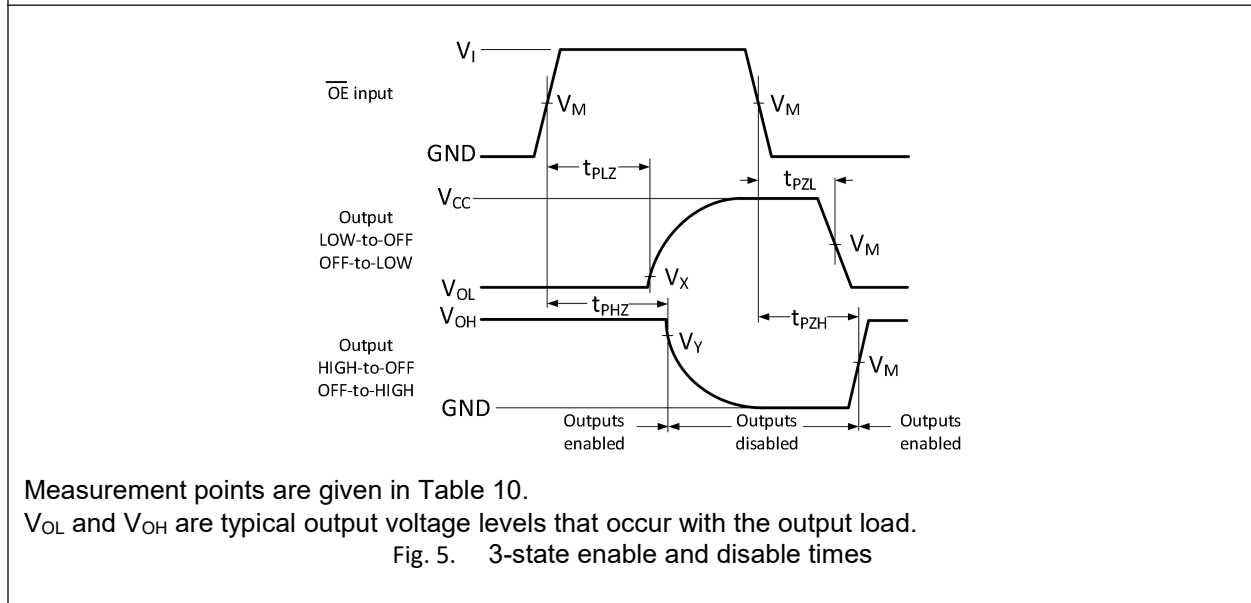
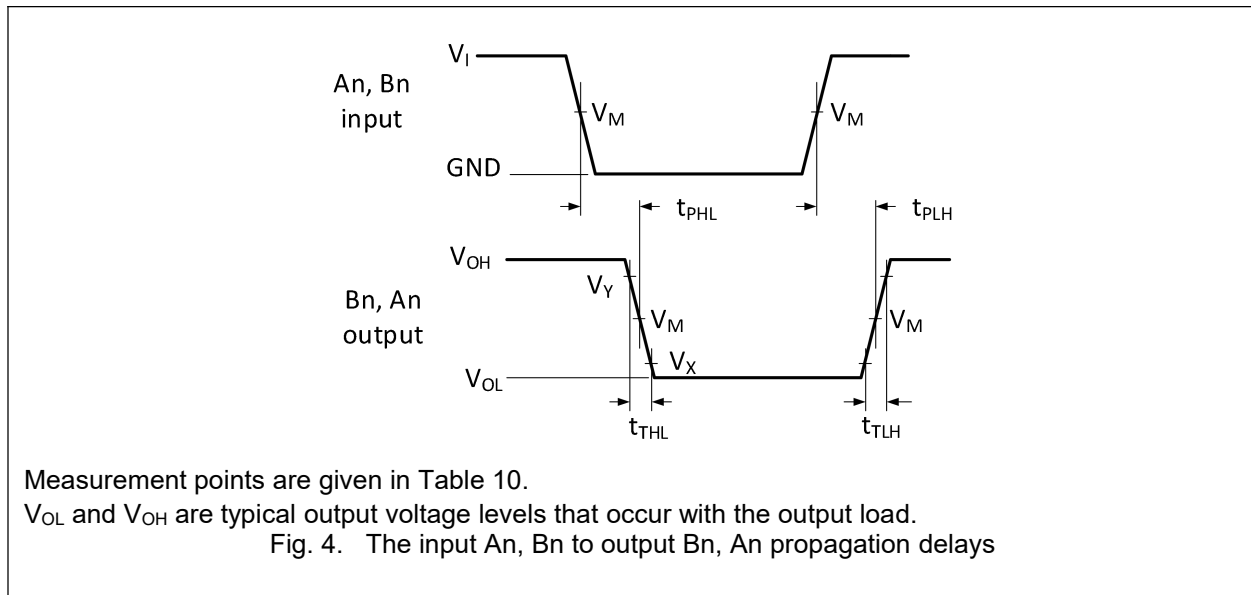


Table 10. Measurement points

Supply voltage	Input [1]	Output [2]		
$V_{CC(A)}, V_{CC(B)}$	V_M	V_M	V_X	V_Y
1.2 V to 1.6 V	$0.5V_{CC1}$	$0.5V_{CC0}$	$V_{OL} + 0.1 V$	$V_{OH} - 0.1 V$
1.65 V to 2.7 V	$0.5V_{CC1}$	$0.5V_{CC0}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
3.0 V to 5.5 V	$0.5V_{CC1}$	$0.5V_{CC0}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

[1] V_{CC1} is the supply voltage associated with the data input port.

[2] V_{CC0} is the supply voltage associated with the output port.

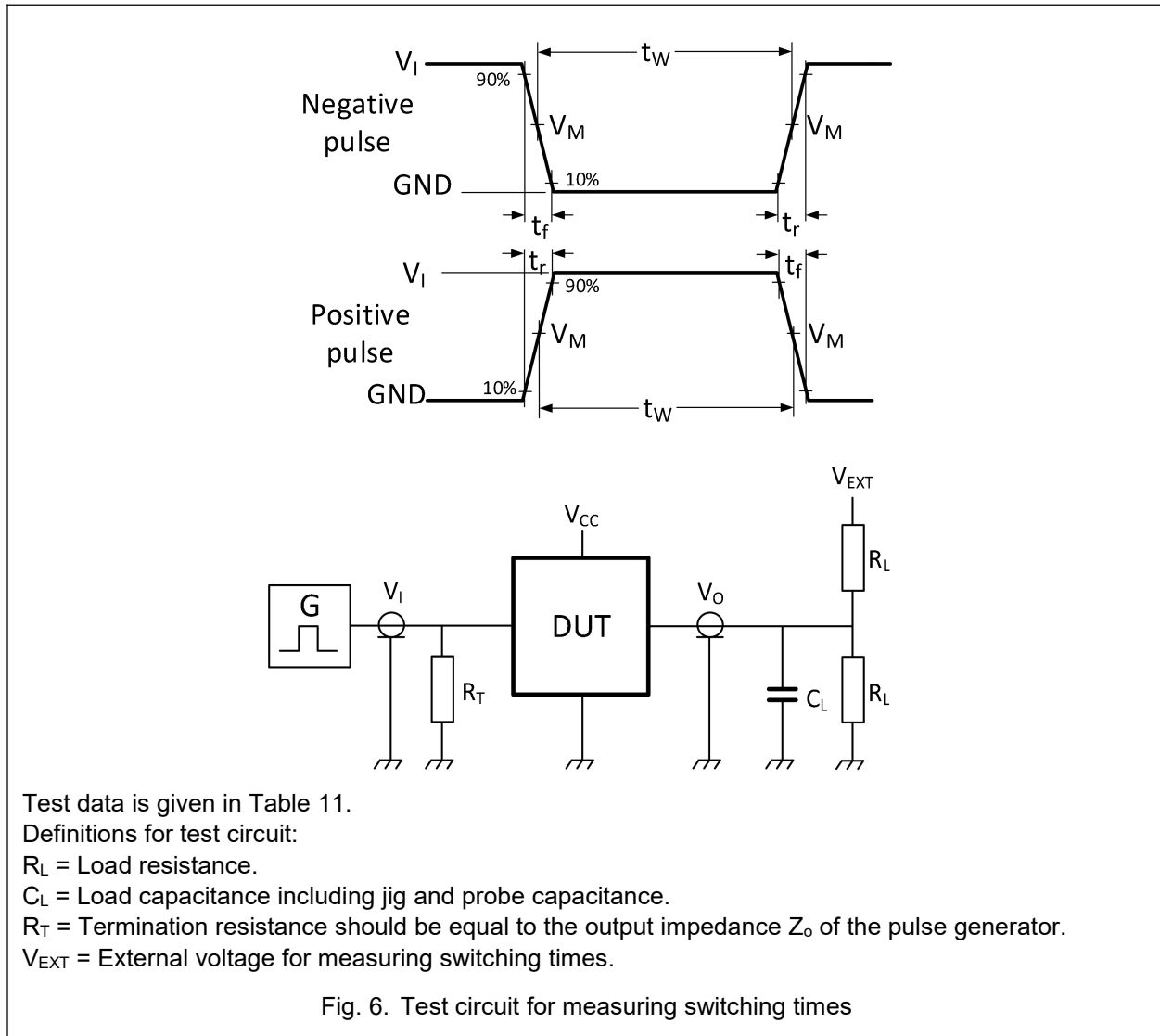


Table 11. Test data

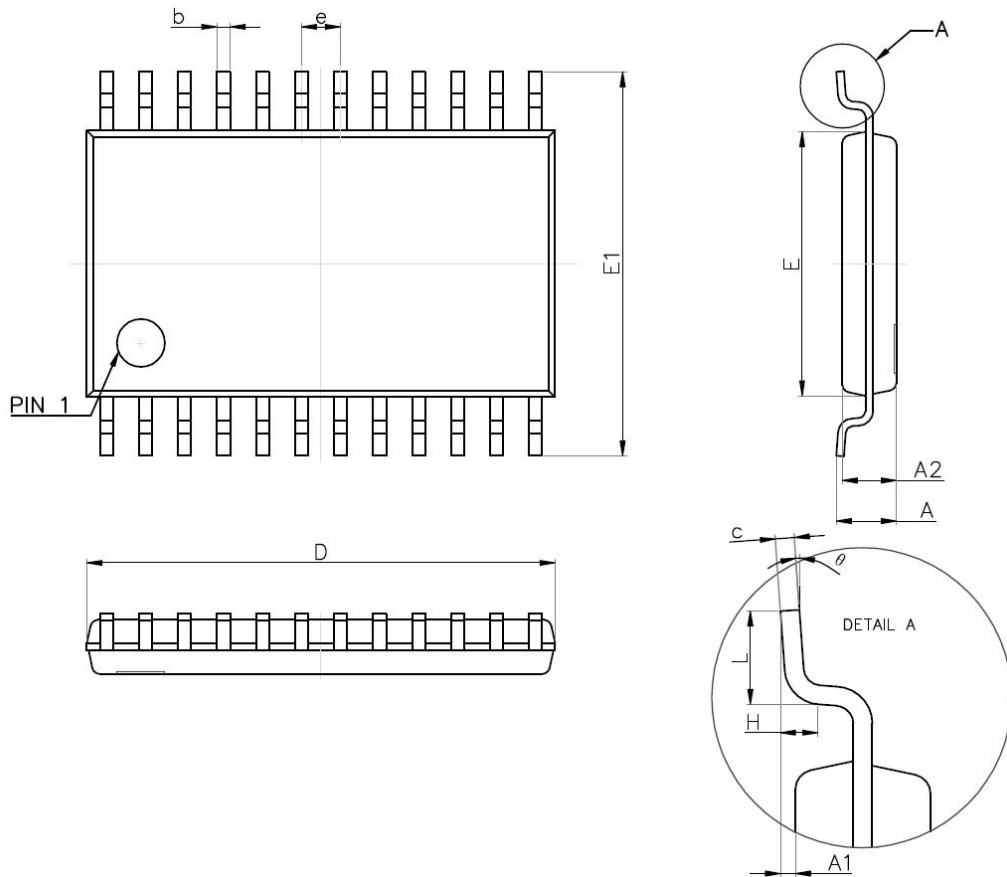
Supply voltage	Input		Load		V_{EXT}		
$V_{CC(A)}, V_{CC(B)}$	V_I [1]	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ} [2]
1.2 V to 5.5 V	V_{CCI}	≤ 2.5 ns	15 pF	2k Ω	open	GND	2 V_{CCO}

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.

11. Package Outline

TSSOP-24L



Symbol	Dimensions In Millimeters		Dimensions In Millimeters	
	Min.	Max.	Min.	Max.
A	-	1.20	6.20	6.60
A1	0.05	0.15	0.65BSC	
A2	0.80	1.05	0.45	0.75
A3	0.39	0.49	1.00REF	
b	0.20	0.28	0°	8°
b1	0.19	0.25		
c	0.13	0.17		
c1	0.12	0.14		
D	6.40	6.60		
E1	4.30	4.50		

12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model

13. Revision History

Table 13. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
74LVC4245 Rev. 1.0	Feb 10, 2025	Draft datasheet		