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NXS0104PW-TP

4-Bit Bidirectional Level Shifter for Both Open-Drian and Push-Pull

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Features

- Wide supply voltage range: VCC(A): 1.2 V to 5.5 V and VCC(B): 1.65 V to 5.5 V
- IOFF circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5 V
- Maximum data rates: Push-pull: 40 Mbps ， Open-drain: 2 Mbps
- No power-supply sequencing required – VCCA or VCCB can be ramped first
- package: TSSOP-14

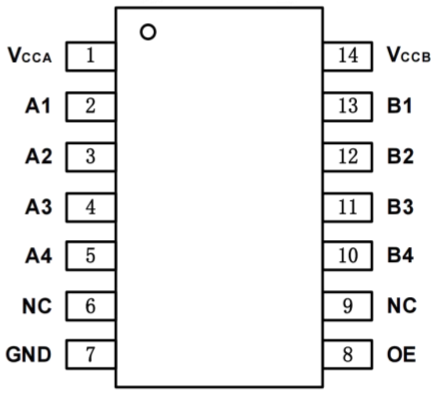
General Description

The is a 4-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 4-bit input-output ports (An and Bn), one output enable (OE) and two supply pins (VCC(A) and VCC(B)). VCC(A) can be supplied at any voltage between 1.2 V and 5.5 V and VCC(B) can be supplied at any voltage between 1.65 V and 5.5 V, making the device suitable for translating between any of the voltage nodes (1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins An and OE are referenced to VCC(A) and pins Bn are referenced to VCC(B). A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using IOFF. The IOFF circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

Applications

- tablet
- smartphone
- Desktop computer
- Handheld Terminal

Pinout (top view)



Pin Configurations

Number	Name	Function	Number	Name	Function
1	VCCA	Supply voltage A	8	OE	Output enable
2	A1	Data IO referenced to VCCA	9	NC	Not connection
3	A2	Data IO referenced to VCCA	10	B4	Data IO referenced to VCCB
4	A3	Data IO referenced to VCCA	11	B3	Data IO referenced to VCCB
5	A4	Data IO referenced to VCCA	12	B2	Data IO referenced to VCCB
6	NC	Not connection	13	B1	Data IO referenced to VCCB
7	GND	Ground	14	VCCB	Supply voltage B

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	Supply voltage A		-0.5	6.5	V
$V_{CC(B)}$	Supply voltage B		-0.5	6.5	V
V_I	Input voltage	OE [1]	-0.5	6.5	V
		An, Bn; Power-down or 3-state mode [1]	-0.5	6.5	V
		An, Bn; Active mode [1] [2] [3]	-0.5	V_{CCI}+0.5	V
V_O	Output voltage	An, Bn; Power-down or 3-state mode [1]	-0.5	6.5	V
		An, Bn; Active mode [1] [3] [4]	-0.5	V_{CCO}+0.5	V
I_{IK}	Input clamping current	V_I < 0 V	-50	--	mA
I_{OK}	Output clamping current	V_O < 0 V	-50	--	mA
I_O	Output current	V_O=0VtoV$_{CCO}$ [2]	--	±50	mA
I_{CC}	Supply current	$I_{CC(A)}$ or $I_{CC(B)}$	--	100	mA
I_{GND}	Ground current		-100	--	mA
P_{tot}	Total power dissipation	T_{amb} = -40 °C to + 125 °C	--	250	mW
T_{stg}	Storage temperature		-65	150	°C

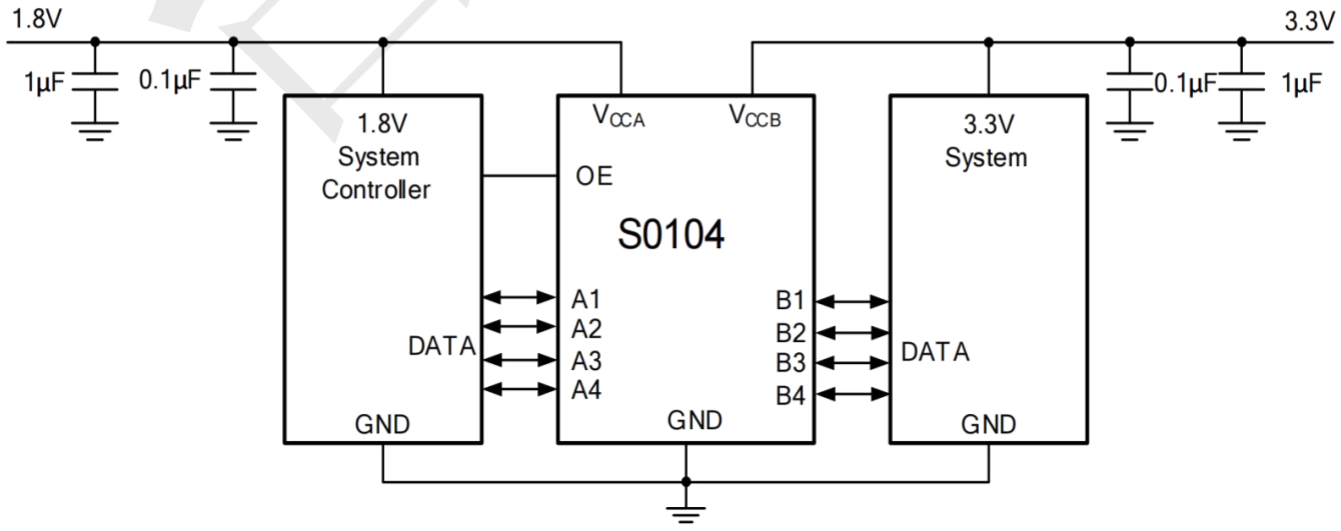
[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCI} is the supply voltage associated with the input.

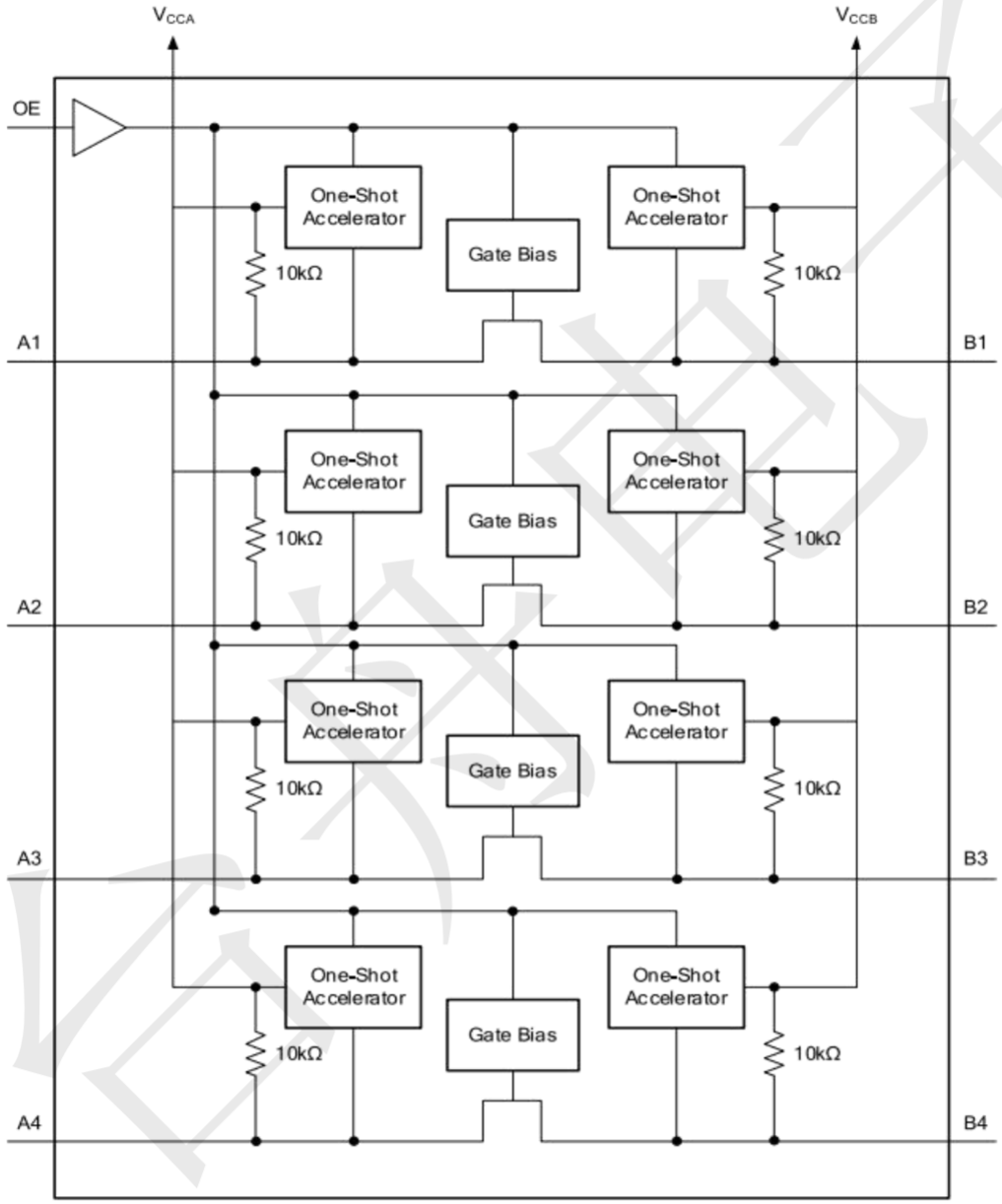
[3] V_{CCI} + 0.5 V or V_{CCO} + 0.5 V should not exceed 6.5 V.

[4] V_{CCO} is the supply voltage associated with the output.

Typical working circuit



Functional Block Diagram



Functional description

VCCA	VCCB	OE	Status
1.2V ~ 5.5V	1.65V ~ 5.5V	L	Both Ax and Bx are High Z
1.2V ~ 5.5V	1.65V ~ 5.5V	H	Ax input (output) and Bx output(input)

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

DC Electrical Characteristics

(Ta=25°C, V_{VCCA} =1.2V~1.8V, V_{VCCB} =1.62V~3.6V, unless otherwise specified)

$V_{CC(A)}$	$V_{CC(B)}$								Unit
	1.8 V		2.5 V		3.3 V		5.0 V		
	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	
1.3 V	0.03	0.001	0.08	0.01	0.15	0.07	0.26	0.35	μA
1.5 V	0.03	0.001	0.08	0.004	0.16	0.05	0.30	0.30	μA
1.8 V	0.03	0.001	0.08	0.001	0.16	0.03	0.33	0.25	μA
2.5 V	--	--	0.07	0.001	0.16	0.001	0.40	0.13	μA
3.3 V	--	--	--	--	0.16	0.001	0.42	0.05	μA
5.0 V	--	--	--	--	--	--	0.43	0.01	μA

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V). All typical values are measured at Tamb = 25℃.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IH}	HIGH-level input voltage	A port						
		$V_{CC(A)}$ = 1.3 V to 1.95 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	$V_{CC(A)}$ - 0.2	--	$V_{CC(A)}$	$V_{CC(A)}$ - 0.2	$V_{CC(A)}$	V
		$V_{CC(A)}$ = 2.3 V to 5.5 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	$V_{CC(A)}$ - 0.4	--	$V_{CC(A)}$	$V_{CC(A)}$ - 0.4	$V_{CC(A)}$	V
		B port						
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	$V_{CC(B)}$ - 0.4	--	$V_{CC(B)}$	$V_{CC(B)}$ - 0.4	$V_{CC(B)}$	V
		OE input						
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	$0.65V_{CC(A)}$	--	$V_{CC(A)}$	$0.65V_{CC(A)}$	$V_{CC(A)}$	V
V_{IL}	LOW-level input voltage	A or B port						
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	0	--	0.15	0	0.15	V
		OE input						
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	0	--	$0.35V_{CC(A)}$	0	$0.35V_{CC(A)}$	V

DC Electrical Characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V). All typical values are measured at Tamb = 25℃.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
V_{OH}	HIGH-level output voltage	A port; I_O = -20 μA; $V_I \geq V_{CC(B)}$ - 0.4 V						
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	0.67V_{C} C(A)	--	--	0.67V_{C} C(A)	--	V
		B port; I_O = -20 μA; $V_I \geq V_{CC(A)}$ - 0.2 V						
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	0.67V_{C} C(B)	--	--	0.67V_{C} C(B)	--	V
V_{OL}	LOW-level output voltage	A or B port; IO = 1 mA; VI ≤ 0.15 V						
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	--	--	0.4	--	0.4	V
I_{OZ}	OFF-state output current	A or B port; $V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65V to 5.5 V	--	--	±4	--	±20	μA
I_I	input leakage current	OE input; $V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65V to 5.5 V	--	--	±4	--	±20	μA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 5.5 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0 V to 5.5 V	--	--	±4	--	±20	μA
		B port; V_I or V_O = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0 V to 5.5 V	--	--	±4	--	±20	μA

DC Electrical Characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V). All typical values are measured at Tamb = 25℃.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
I_{CC}	supply current	OE = 0 V or $V_{CC(A)}$; An, Bn open						
		$I_{CC(A)}$						
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	--	--	12	--	54	μA
		$V_{CC(A)}$ = 5.5 V; $V_{CC(B)}$ = 0 V	--	--	3.7	--	19	μA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V	--	--	-1	--	-1	μA
		$I_{CC(B)}$						
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	--	--	11	--	53	μA
		$V_{CC(A)}$ = 5.5 V; $V_{CC(B)}$ = 0 V	--	--	-1	--	-1	μA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V	--	--	3.7	--	19	μA
		$I_{CC(A)}$ + $I_{CC(B)}$						
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	--	--	21	--	105	μA
C_I	input capacitance	OE input; $V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V	--	4	--	--	--	pF
$C_{I/O}$	input/output capacitance	A port; $V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V						
		enabled	--	7	--	--	--	pF
		disabled	--	3.1	--	--	--	pF
		B port; $V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V						
		enabled	--	7	--	--	--	pF
		disabled	--	3.1	--	--	--	pF

AC Electrical Characteristics

(Ta=25°C, V_{CCA} =1.2V~1.8V, V_{CCB} =1.62V~3.6V, unless otherwise specified)

Symbol	Parameter	Conditions	1.8±0.15 V	2.5 V ± 0.2 V	3.3 V ± 0.3 V	5.0 V ± 0.5 V	Unit
			Typ	Typ	Typ	Typ	
$V_{CC(A)}$ = 1.3 V; T_{amb} = 25℃							
t_{PHL}	HIGH to LOW propagation delay	A to B	4.9	6.5	7.8	9.5	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	8.6	6.9	6.2	6.0	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	4.5	5.6	6.5	8.7	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	5.8	5.1	4.9	4.8	ns
t_{en}	enable time	OE to A, B ; see Fig. 5 [1]	82	82	82	82	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]	190	190	190	190	ns
		OE to B see Fig.6 [1]	174	137	182	131	ns
t_{TLH}	LOW to HIGH output transition time	A port	7.4	6.7	6.7	6.5	ns
		B port	10.2	8.2	6.6	6.5	ns
t_{THL}	HIGH to LOW output transition time	A port	7.3	7.3	7.6	7.6	ns
		B port	9.3	12.8	11.2	17.1	ns
$t_{sk(O)}$	output skew time	between channels [2]	0.7	0.7	0.7	0.7	ns
t_W	pulse width	data inputs	25	25	25	25	ns
f_{data}	data rate		40	40	40	40	Mbps

AC characteristics for temperature range -40 °C to +85 °C

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.5 V ± 0.1V											
t_{PHL}	HIGH to LOW propagation delay	A to B	--	6.0	--	7.0	--	8.6	--	10.5	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	--	12.6	--	10.0	--	8.5	--	8.0	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	--	5.1	--	5.5	--	5.9	--	6.5	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	--	8.5	--	8.0	--	5.8	--	5.5	ns
t_{en}	enable time	OE to A, B ; see Fig. 5 [1]	--	120	--	120	--	120	--	120	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]	--	230	--	230	--	230	--	230	ns
		OE to B see Fig.6 [1]	--	200	--	150	--	180	--	115	ns
t_{TLH}	LOW to HIGH output transition time	A port	2.5	10.6	2.1	9.5	1.9	9.1	1.9	8.9	ns
		B port	4.1	15.2	3.2	10.6	2.8	8.7	0.4	7.5	ns
t_{THL}	HIGH to LOW output transition	A port	3.0	9.7	3.1	10.8	3.1	10.1	3.1	10.2	ns
		B port	3.0	11.7	3.6	15.7	4.2	14.2	5.5	21.4	ns

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
	time										
$t_{sk(O)}$	output skew time	between channels [2]	--	--	--	0.7	--	0.7	--	0.7	ns
t_W	pulse width	data inputs	--	--	25	--	25	--	25	--	ns
f_{data}	data rate		--	--	--	40	--	40	--	40	Mbps
$V_{CC(A)}$ = 1.8 V ± 0.15 V											
t_{PHL}	HIGH to LOW propagation delay	A to B	--	4.5	--	5.0	--	5.5	--	7.5	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	--	11.3	--	8.4	--	6.4	--	6.1	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	--	3.5	--	4.1	--	4.5	--	5.5	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	--	6.5	--	6.0	--	5.0	--	4.6	ns
t_{en}	enable time	OE to A, B ; see Fig. 5 [1]	--	100	--	100	--	100	--	100	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]	--	200	--	200	--	200	--	200	ns
		OE to B see Fig.6 [1]	--	200	--	150	--	180	--	115	ns
t_{TLH}	LOW to HIGH output transition time	A port	2.3	8.7	1.8	7.6	1.6	7.4	1.5	7.1	ns
		B port	3.9	14.2	3.1	9.8	2.7	7.7	2.3	6.8	ns

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{THL}	HIGH to LOW output transition time	A port	2.7	9.2	2.7	9.3	2.7	9.7	2.9	9.8	ns
		B port	2.6	9.6	2.9	12.0	3.3	9.8	4.3	15.0	ns
$t_{sk(O)}$	output skew time	between channels [2]	--	--	--	0.7	--	0.7	--	0.7	ns
t_W	pulse width	data inputs	--	--	25	--	25	--	25	--	ns
f_{data}	data rate		--	--	--	40	--	40	--	40	Mbps
$V_{CC(A)}$ = 2.5 V ± 0.2 V											
t_{PHL}	HIGH to LOW propagation delay	A to B	--	--	--	2.5	--	2.7	--	3.8	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	--	--	--	5.7	--	5.0	--	5.2	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	--	--	--	2.8	--	3.5	--	4.2	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	--	--	--	1.8	--	1.6	--	1.5	ns
t_{en}	enable time	OE to A, B ; see Fig. 5 [1]	--	--	--	80	--	80	--	80	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]	--	--	--	150	--	150	--	150	ns
		OE to B see Fig.6 [1]	--	--	--	150	--	180	--	115	ns
t_{TLH}	LOW to	A port	--	--	1.7	6.3	1.4	5.9	1.3	5.7	ns

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
	HIGH output transition time	B port	--	--	2.7	9.1	2.4	7.1	2.1	6.0-	ns
t_{THL}	HIGH to LOW output transition time	A port	--	--	2.4	9.9	2.5	10.1	2.5	10.3	ns
		B port	--	--	2.3	9.8	2.5	7.4	3.0	10.5	ns
$t_{sk(O)}$	output skew time	between channels [2]	--	--	--	0.7	--	0.7	--	0.7	ns
t_W	pulse width	data inputs	--	--	25	--	25	--	25	--	ns
f_{data}	data rate		--	--	--	40	--	40	--	40	Mbps
$V_{CC(A)}$ = 3.3 V ± 0.3 V											
t_{PHL}	HIGH to LOW propagation delay	A to B	--	--	--	--	--	1.9	--	2.7	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	--	--	--	--	--	3.0	--	3.5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	--	--	--	--	--	3.0	--	3.5	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	--	--	--	--	--	1.9	--	1.7	ns
t_{en}	enable time	OE to A, B ; see Fig. 5 [1]	--	--	--	--	--	70	--	70	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]	--	--	--	--	--	180	--	180	ns

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
		OE to B see Fig.6 [1]	--	--	--	--	--	180	--	115	ns
t_{TLH}	LOW to HIGH output transition time	A port	--	--	--	--	1.4	4.7	1.2	4.3	ns
		B port	--	--	--	--	2.2	6.6	2	5.8	ns
t_{THL}	HIGH to LOW output transition time	A port	--	--	--	--	2.3	7.3	2.3	7.9	ns
		B port	--	--	--	--	2.3	6.9	2.5	9.6	ns
$t_{sk(O)}$	output skew time	between channels [2]	--	--	--	--	--	0.7	--	0.7	ns
t_W	pulse width	data inputs	25	--	25	--	25	--	25	--	ns
f_{data}	data rate		--	40	--	40	--	40	--	40	Mbps
$V_{CC(A)}$ = 5.5 V ± 0.5 V											
t_{PHL}	HIGH to LOW propagation delay	A to B	--	--	--	--	--	--	--	1.8	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	--	--	--	--	--	--	--	1.5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	--	--	--	--	--	--	--	2.5	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	--	--	--	--	--	--	--	2.3	ns
t_{en}	enable time	OE to A, B ; see Fig. 5	--	--	--	--	--	--	--	60	ns

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
		[1]									
t_{dis}	disable time	OE to A; see Fig.6 [1]	--	--	--	--	--	--	--	115	ns
		OE to B see Fig.6 [1]	--	--	--	--	--	--	--	115	ns
t_{TLH}	LOW to HIGH output transition time	A port	--	--	--	--	--	--	1.4	6.0	ns
		B port	--	--	--	--	--	--	1.8	5.8	ns
t_{THL}	HIGH to LOW output transition time	A port	--	--	--	--	--	--	2.2	9.4	ns
		B port	--	--	--	--	--	--	2.2	9.2	ns
$t_{sk(O)}$	output skew time	between channels [2]	--	--	--	--	--	0.7	--	0.7	ns
t_W	pulse width	data inputs	25	--	25	--	25	--	25	--	ns
f_{data}	data rate		--	40	--	40	--	40	--	40	Mbps

[1] t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[2] Skew between any two outputs of the same package switching in the same direction.

AC characteristics for temperature range -40 °C to +125 °C

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.5 V ± 0.1V											
t_{PHL}	HIGH to LOW propagation delay	A to B	--	6.0	--	7.0	--	8.6	--	10.5	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	--	12.6	--	10.5	--	9.2	--	8.5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	--	5.1	--	5.5	--	5.9	--	6.5	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	--	8.5	--	8.0	--	5.8	--	5.5	ns
t_{en}	enable time	OE to A, B ; see Fig. 5 [1]	--	120	--	120	--	120	--	120	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]	--	230	--	230	--	230	--	230	ns
		OE to B see Fig.6 [1]	--	200	--	150	--	180	--	115	ns
t_{TLH}	LOW to HIGH output transition time	A port	2.5	10.8	2.1	9.6	1.9	9.3	1.9	9.9	ns
		B port	4.1	15.3	3.2	10.9	2.8	8.9	0.4	7.7	ns
t_{THL}	HIGH to LOW output transition	A port	3.0	9.7	3.1	10.8	3.1	10.1	3.1	10.2	ns
		B port	3.0	11.7	3.6	15.7	4.2	14.2	5.5	21.4	ns

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
	time										
$t_{sk(O)}$	output skew time	between channels [2]	--	--	--	0.8	--	0.8	--	0.8	ns
t_W	pulse width	data inputs	--	--	25	--	25	--	25	--	ns
f_{data}	data rate		--	--	--	40	--	40	--	40	Mbps
$V_{CC(A)}$ = 1.8 V ± 0.15 V											
t_{PHL}	HIGH to LOW propagation delay	A to B	--	4.5	--	5.0	--	5.5	--	7.5	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	--	11.3	--	9.0	--	7.1	--	6.7	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	--	3.5	--	4.1	--	4.5	--	5.5	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	--	6.5	--	6.0	--	5.0	--	4.6	ns
t_{en}	enable time	OE to A, B ; see Fig. 5 [1]	--	100	--	100	--	100	--	100	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]	--	200	--	200	--	200	--	200	ns
		OE to B see Fig.6 [1]	--	200	--	150	--	180	--	115	ns
t_{TLH}	LOW to HIGH output transition time	A port	2.3	8.9	1.8	7.8	1.6	7.6	1.5	7.3	ns
		B port	3.9	14.3	3.1	10.1	2.7	7.9	2.3	7.4	ns
t_{THL}	HIGH to	A port	2.7	9.2	2.7	9.3	2.7	9.7	2.9	9.8	ns

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
	LOW output transition time	B port	2.6	9.6	2.9	12.0	3.3	9.8	4.3	15.0	ns
$t_{sk(O)}$	output skew time	between channels [2]	--	--	--	0.8	--	0.8	--	0.8	ns
t_W	pulse width	data inputs	--	--	25	--	25	--	25	--	ns
f_{data}	data rate		--	--	--	40	--	40	--	40	Mbps
$V_{CC(A)}$ = 2.5 V ± 0.2 V											
t_{PHL}	HIGH to LOW propagation delay	A to B	--	--	--	2.7	--	2.9	--	4.1	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	--	--	--	5.7	--	5.5	--	5.8	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	--	--	--	2.8	--	4.0	--	5.3	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	--	--	--	1.8	--	1.6	--	1.7	ns
t_{en}	enable time	OE to A, B ; see Fig. 5 [1]	--	--	--	80	--	80	--	80	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]	--	--	--	150	--	150	--	150	ns
		OE to B see Fig.6 [1]	--	--	--	150	--	180	--	115	ns
t_{TLH}	LOW to HIGH output	A port	--	--	1.7	6.5	1.4	6.1	1.3	5.8	ns
		B port	--	--	2.7	9.3	2.4	7.3	2.1	6.2	ns

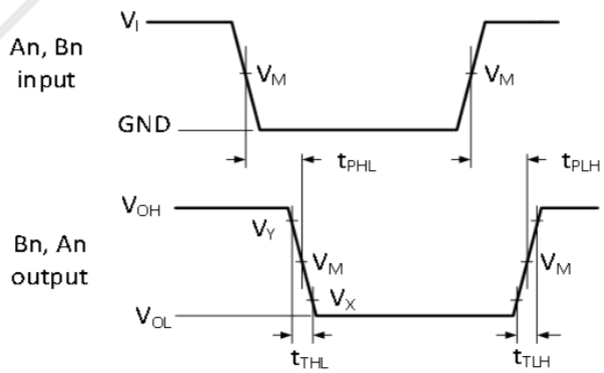
Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
	transition time										
t_{THL}	HIGH to LOW output transition time	A port	--	--	2.4	9.9	2.5	10.1	2.5	10.3	ns
		B port	--	--	2.3	9.8	2.5	7.4	3.0	10.5	ns
$t_{sk(O)}$	output skew time	between channels [2]	--	--	--	0.8	--	0.8	--	0.8	ns
t_W	pulse width	data inputs	--	--	25	--	25	--	25	--	ns
f_{data}	data rate		--	--	--	40	--	40	--	40	Mbps
$V_{CC(A)}$ = 3.3 V ± 0.3 V											
t_{PHL}	HIGH to LOW propagation delay	A to B	--	--	--	--	--	2.1	--	3.0	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	--	--	--	--	--	3.0	--	4.0	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	--	--	--	--	--	3.5	--	4.0	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	--	--	--	--	--	1.9	--	1.7	ns
t_{en}	enable time	OE to A, B ; see Fig. 5 [1]	--	--	--	--	--	70	--	70	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]	--	--	--	--	--	180	--	180	ns
		OE to B see Fig.6 [1]	--	--	--	--	--	180	--	115	ns

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{TLH}	LOW to HIGH output transition time	A port	--	--	--	--	1.4	4.8	1.2	4.4	ns
		B port	--	--	--	--	2.2	6.9	2	6.1	ns
t_{THL}	HIGH to LOW output transition time	A port	--	--	--	--	2.3	7.3	2.3	7.9	ns
		B port	--	--	--	--	2.3	6.9	2.5	9.6	ns
$t_{sk(O)}$	output skew time	between channels [2]	--	--	--	--	--	0.8	--	0.8	ns
t_W	pulse width	data inputs	25	--	25	--	25	--	25	--	ns
f_{data}	data rate		--	40	--	40	--	40	--	40	Mbps
$V_{CC(A)}$ = 5.5 V ± 0.5 V											
t_{PHL}	HIGH to LOW propagation delay	A to B	--	--	--	--	--	--	--	1.9	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	--	--	--	--	--	--	--	1.8	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	--	--	--	--	--	--	--	3.0	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	--	--	--	--	--	--	--	2.3	ns
t_{en}	enable time	OE to A, B ; see Fig. 5 [1]	--	--	--	--	--	--	--	60	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]	--	--	--	--	--	--	--	115	ns

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
		OE to B see Fig.6 [1]	--	--	--	--	--	--	--	115	ns
t_{TLH}	LOW to HIGH output transition time	A port	--	--	--	--	--	--	1.4	6.5	ns
		B port	--	--	--	--	--	--	1.8	6.2	ns
t_{THL}	HIGH to LOW output transition time	A port	--	--	--	--	--	--	2.2	9.5	ns
		B port	--	--	--	--	--	--	2.2	9.3	ns
$t_{sk(O)}$	output skew time	between channels [2]	--	--	--	--	--	--	--	0.8	ns
t_W	pulse width	data inputs	25		25		25		25		ns
f_{data}	data rate		--	40	--	40	--	40	--	40	Mbps

[1] t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[2] Skew between any two outputs of the same package switching in the same direction.

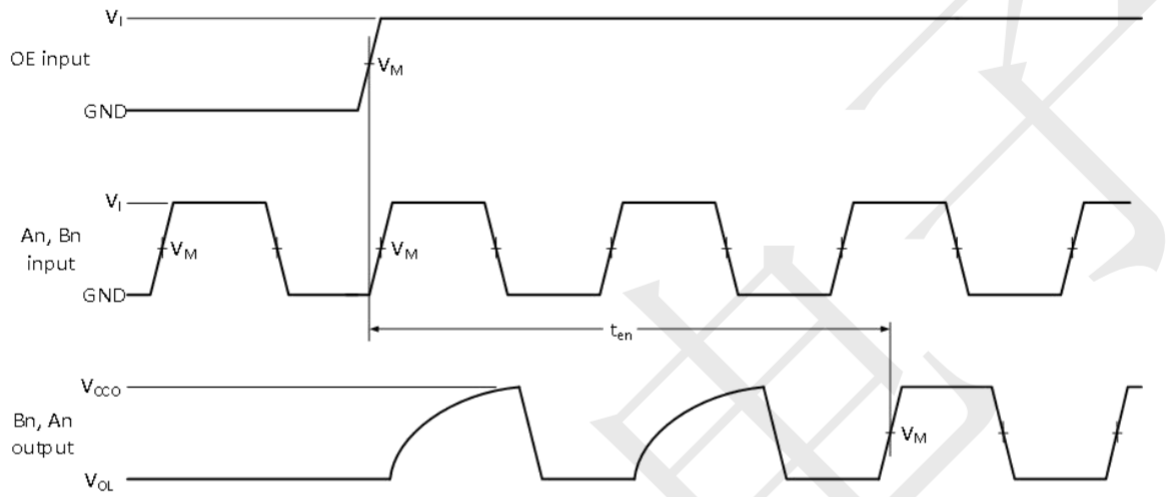
Waveforms and test circuit



Measurement points are given in Table 12.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

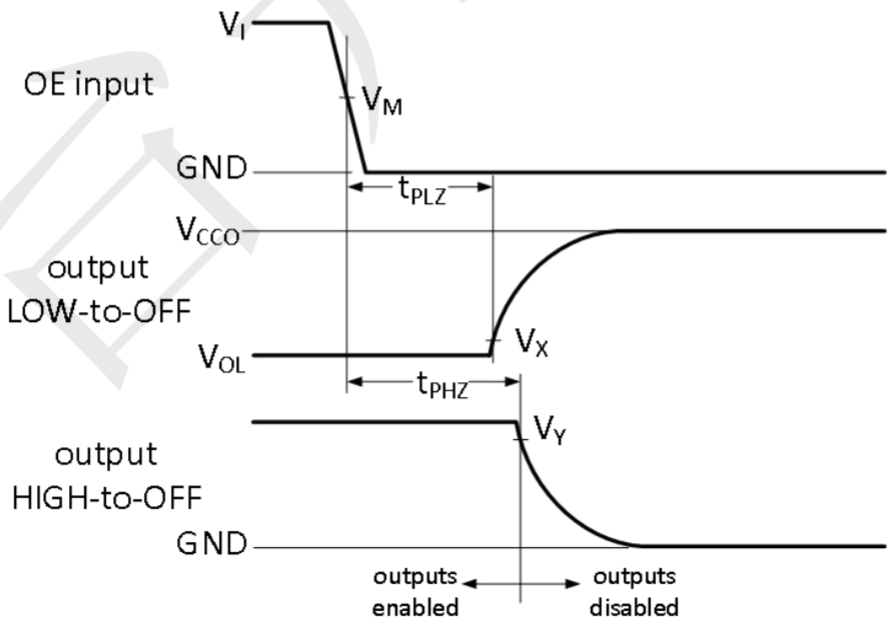
Fig. 1. The data input (An, Bn) to data output (Bn, An) propagation delay times

Waveforms and test circuit



(1) The enable time (ten) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. See also Section 11.6
Measurement points are given in Table 11.
V_{OL} is a typical output voltage level that occur with the output load.
V_{CCO} is the supply voltage associated with the output.

Fig. 2. Enable times



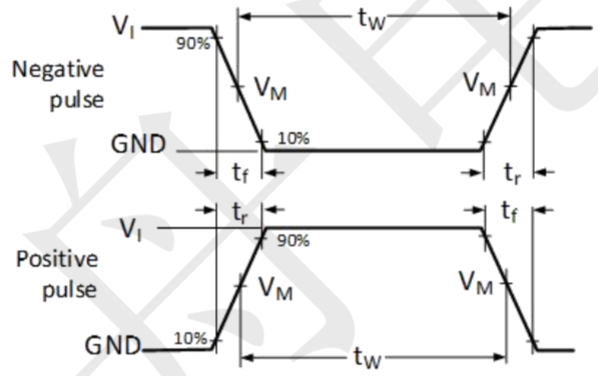
Measurement points are given in Table 11.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.
V_{CCO} is the supply voltage associated with the output.

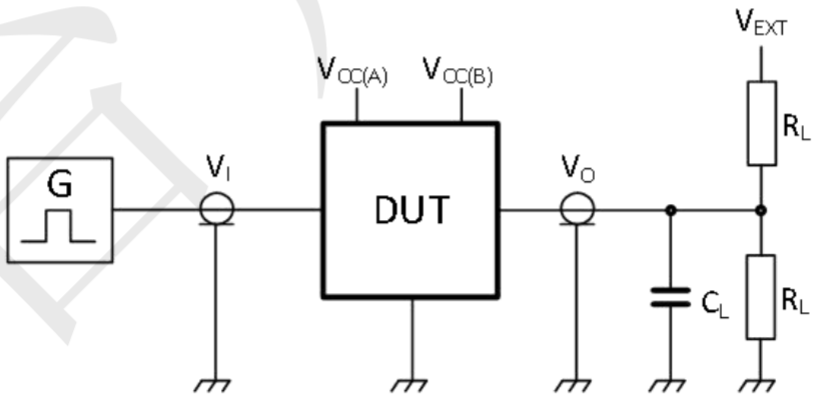
Fig. 3. Disable times

Measurement points

Supply Voltage	Input	Output		
V_{CCO}	V_M	V_M	V_X	V_Y
1.8 V ± 0.15 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.5 V ± 0.2 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
3.3 V ± 0.3 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V
5.0 V ± 0.5 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V

[1] V_{CCI} is the supply voltage associated with the input.
[2] V_{CCO} is the supply voltage associated with the output.





Test data is given in Table 12.
All input pulses are supplied by generators having the following characteristics:
PRR ⩽ 10 MHz; Z_O = 50 Ω; dV/dt ⩾ 1.0 V/ns.
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
V_{EXT} = External voltage for measuring switching times.

Fig. 4. Test circuit for measuring switching times

Test data

Supply voltage		Input		Load		V_{EXT}		
$V_{CC(A)}$	$V_{CC(B)}$	V_I [1]	$\Delta t/\Delta V$	C_L	R_L [2]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.3 V to 5.5 V	1.65 V to 5.5 V	V_{CCI}	≤2.5 ns/V	15 pF	50 kΩ, 1MΩ	open	open	$2V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the input.

[2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R_L = 1 MΩ. For measuring enable and disable times, R_L = 50 kΩ.

[3] V_{CCO} is the supply voltage associated with the output.

Application information

Voltage level-translation applications. The S0104 can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device is primarily targeted at I^2C or 1-wire which use open-drain drivers, it may also be used in applications where push-pull drivers are connected to the ports.

Architecture

The architecture of the S0104 is shown in Fig. 1. The device does not require an extra input signal to control the direction of data flow from A to B or B to A.

The S0104 is a "switch" type voltage translator, it employs two key circuits to enable voltage translation:

1. A pass-gate transistor (N-channel) that ties the ports together.
2. An output edge-rate accelerator that detects and accelerates rising edges on the I/O pins.

The gate bias voltage of the pass gate transistor (T3) is set at approximately one threshold voltage above the V_{CC} level of the low-voltage side. During a LOW-to-HIGH transition the output one-shot accelerates the output transition by switching on the PMOS transistors (T1, T2) bypassing the 10 kΩ pull-up resistors and increasing current drive capability. The one-shot is activated once the input transition reaches approximately $0.5V_{CCI}$; it is de-activated approximately 50 ns after the output reaches $0.5V_{CCO}$. During the acceleration time the driver output resistance is between approximately 50 Ω and 70 Ω.

To avoid signal contention and minimize dynamic I_{CC}, the user should wait for the one-shot circuit to turn-off before applying a signal in the opposite direction. Pull-up resistors are included in the device for DC current sourcing capability.

Input driver requirements

As the S0104 is a switch type translator, properties of the input driver directly affect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system; the max data rate, HIGH-to-LOW output transition time (t_{THL}) and propagation delay (t_{PHL}) are dependent upon the output impedance and edge-rate of the external driver. The limits provided for these parameters in the datasheet assume a driver with output impedance below 50 Ω is used.

Output load considerations

The maximum lumped capacitive load that can be driven is dependent upon the one-shot pulse duration. In cases with very heavy capacitive loading there is a risk that the output will not reach the positive rail within the one-shot pulse duration. To avoid excessive capacitive loading and to ensure correct triggering of the one-shot it's recommended to use short trace lengths and low capacitance connectors on B0104 PCB layouts. To ensure low impedance termination and avoid output signal oscillations and one-shot re-triggering, the length of the PCB trace should be such that the around trip delay of any reflection is within the one-shot pulse duration.

Power up

During operation $V_{CC(A)}$ must never be higher than $V_{CC(B)}$, however during power-up $V_{CC(A)} \geq V_{CC(B)}$ does not damage the device, so any power supply can be ramped up first. There is no special power-up sequencing required. The B0104 includes circuitry that disables all output ports when either $V_{CC(A)}$ or $V_{CC(B)}$ is switched off.

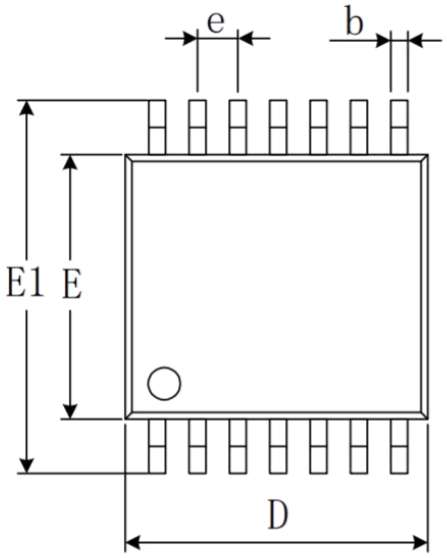
Enable and disable

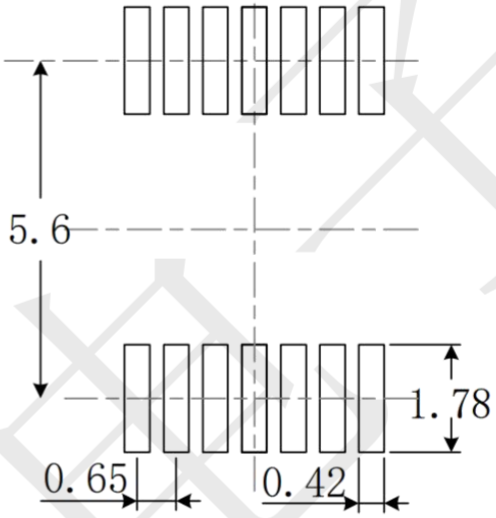
An output enable input (OE) is used to disable the device. Setting OE to LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (tdis with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor, the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Pull-up or pull-down resistors on I/O lines

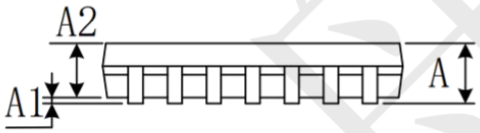
Each A port I/O has an internal 10 kΩ pull-up resistor to $V_{CC(A)}$, and each B port I/O has an internal 10 kΩ pull-up resistor to $V_{CC(B)}$. If a smaller value of pull-up resistor is required, an external resistor must be added parallel to the internal 10 kΩ, this will affect the V_{OL} level. When OE goes LOW the internal pull-ups of the S0104 are disabled.

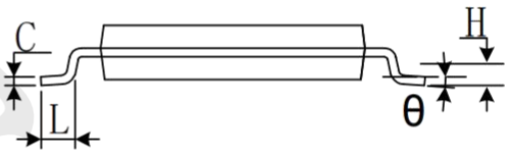
Package information TSSOP -14





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.860	5.100	0.191	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.250(TYP)		0.010(TYP)	
θ	1°	7°	1°	7°