PXAE183708NB

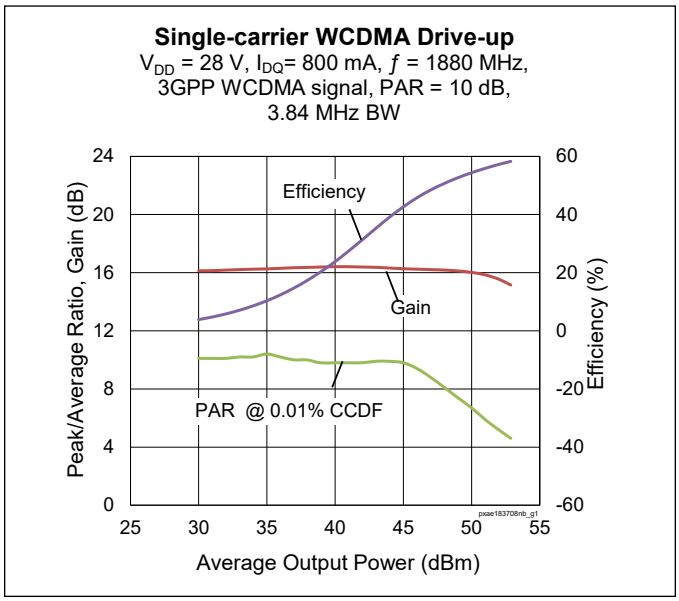
Thermally-Enhanced High Power RF LDMOS FET
320 W, 48 V, 1805 – 1880 MHz



Package Type: PG-HB2SOF-8-1

Description

The PXAE183708NB is a 320-watt LDMOS FET intended for use in multi-standard cellular power amplifier applications in the 1805 to 1880 MHz frequency band. Features include input and output matching, high gain and thermally-enhanced package with earless flange. Manufactured with an advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



Features

- Broadband internal input and output matching
- Asymmetrical Doherty design
  - Main: P_{3dB} = 160 W Typ
  - Peak: P_{3dB} = 315 W Typ
- Typical Pulsed CW performance, 1880 MHz, 28 V, Doherty configuration, 10 µs pulse width, 10% duty cycle, Class AB (main), Class C (peak)
  - Output power at P_{1dB} = 320 W
  - Output power at P_{3dB} = 430 W
  - Drain efficiency = 60%
  - Gain = 13.5 dB
- Capable of handling 10:1 VSWR @ 28 V, 54 W (1C WCDMA) output power
- Human Body Model Class 2 (per ANSI/ESDA/JEDEC JS-001)
- Integrated ESD protection
- Low thermal resistance
- Pb-free and RoHS compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in the Doherty production test circuit)

V_{DD} = 28 V, I_{DQ} = 800 mA, P_{OUT} = 54 W avg, $V_{GS(PEAK)}$ = 1.5 V, ƒ = 1880 MHz, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Gain	G_{ps}	15.3	16	—	dB
Drain Efficiency	ηD	48	50.5	—	%
Adjacent Channel Power Ratio	ACPR	—	–29.5	–25	dBc
Output PAR @ 0.01% CCDF	OPAR	6.8	7.7	—	dB

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RoHS compliant

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Rev. 04, 2022-12-20

DC Characteristics

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-source Breakdown Voltage	$V_{BR(DSS)}$	65	—	—	V	V_{GS} = 0 V, I_{DS} = 10 mA
Drain Leakage Current (main)	I_{DSS}	—	—	1	µA	V_{DS} = 28 V, V_{GS} = 0 V
(peak)		—	—	10		V_{DS} = 60 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	1	µA	V_{GS} = 10 V, V_{DS} = 0 V
On-State Resistance (main)	$R_{DS(on)}$	—	0.08	—	W	V_{GS} = 10 V, V_{DS} = 0.1 V
(peak)		—	0.04	—		
Operating Gate Voltage (main)	V_{GS}	2.7	2.9	3.3	V	V_{DS} = 28 V, I_{DQ} = 800 mA
(peak)		—	1.5	—		V_{DS} = 28 V, I_{DQ} = 0 mA

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	65	V
Gate-source Voltage	V_{GS}	–6 to +10	
Operating Voltage	V_{DD}	0 to +32	
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	

1. Operation above the maximum values listed here may cause permanent damage. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For reliable continuous operation, the device should be operated within the operating voltage range (V_{DD}) specified above.
2. Product's qualification were performed at 225 °C. Operation at T_J (275 °C) reduces median time to failure.

Thermal Characteristics

Parameter	Symbol	Value	Unit	Conditions
Thermal Resistance (main)	$R_{\theta JC}$	0.63	°C/W	T_{CASE} = 70°C, 54 W CW
Thermal Resistance (peak)		0.20		T_{CASE} = 70°C, 316 W CW

Moisture Sensivity Level

Level	Test Signal	Package Temperature	Unit
3	IPC/JEDEC J-STD-020	260	°C

Ordering Information

Type and Version	Order Code	Package Description	Shipping
PXAE183708NB V1 R2	PXAE183708NB-V1-R2	PG-HB2SOF-8-1	Tape & Reel, 250 pcs

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Typical Performance (data taken in test fixture)

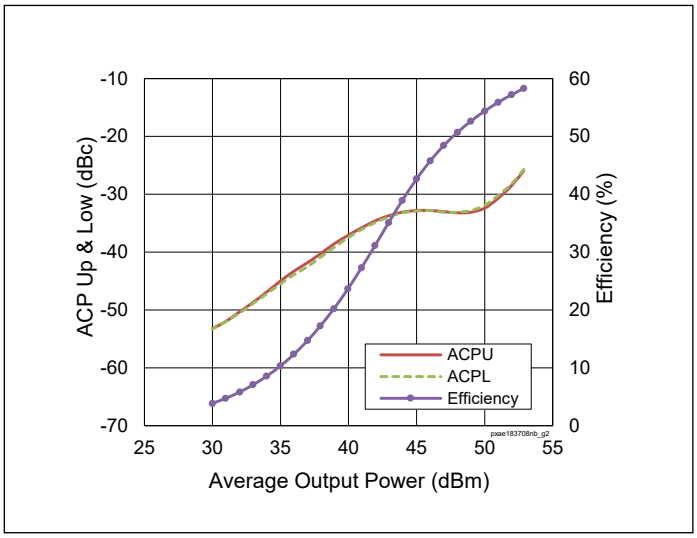


Figure 1. Single-carrier WCDMA Drive-up
V_{DD} = 28 V, $I_{DQ(MAIN)}$ = 800 mA, f = 1880 MHz,
3GPP WCDMA signal, PAR = 10 dB,
BW = 3.84 MHz

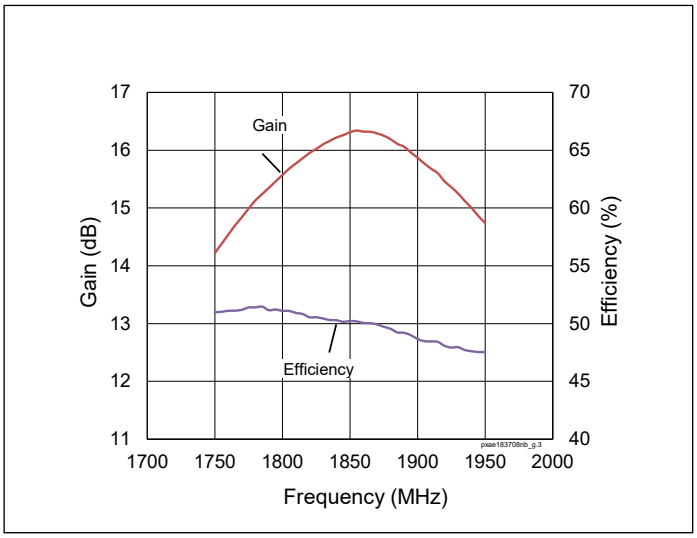


Figure 2. Single-carrier WCDMA Broadband
V_{DD} = 28 V, I_{DQ} = 800 mA, P_{OUT} = 47.3 dBm,
3GPP WCDMA signal, PAR = 10 dB

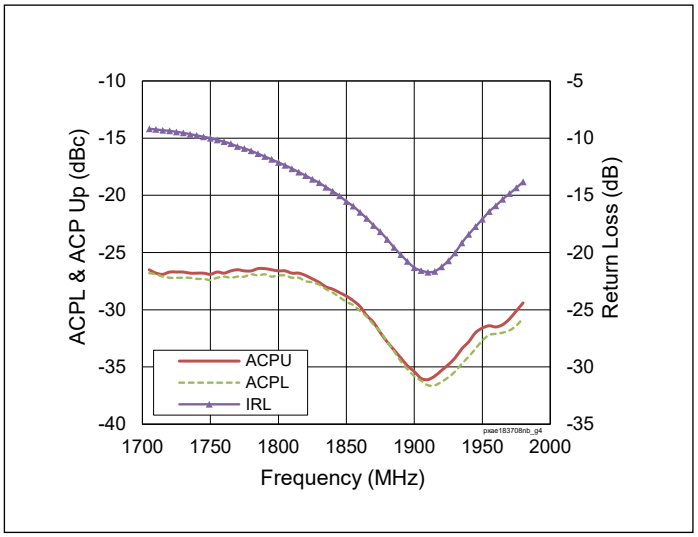


Figure 3. Single-carrier WCDMA Broadband
V_{DD} = 28 V, I_{DQ}= 800 mA, P_{OUT} = 47.3 dBm,
3GPP WCDMA signal, PAR = 10 dB

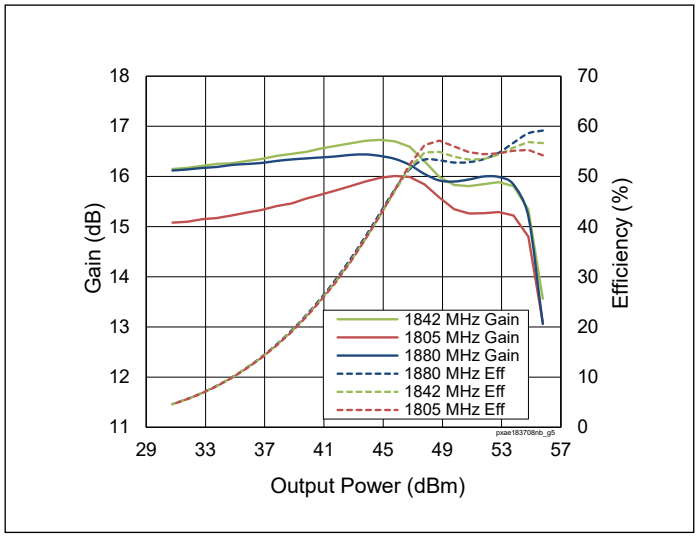


Figure 4. CW Performance
V_{DD} = 28 V, I_{DQ} = 800 mA

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Typical Performance (cont.)

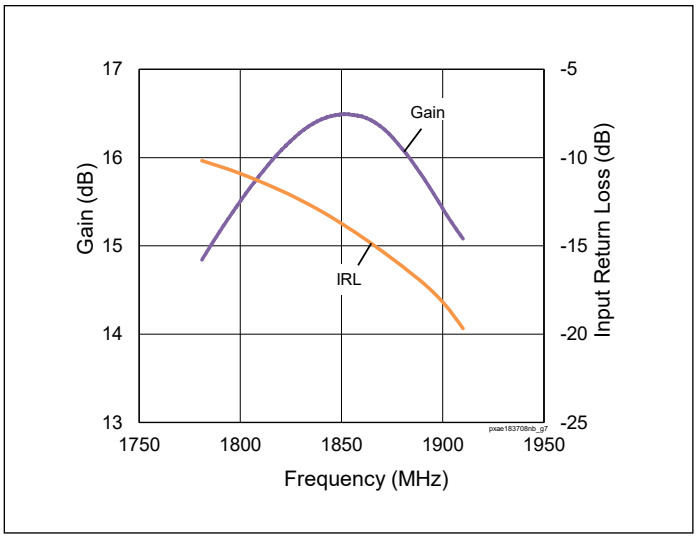


Figure 5. Small Signal CW Gain & Input Return Loss
V_{DD} = 28 V, I_{DQ} = 800 mA

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Load Pull Performance

Main side load pull performance – pulsed CW signal: 10 µsec, 10% duty cycle, 28 V, I_{DQ} = 850 mA, class AB

		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Z_s [Ω]	Z_l [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]	Z_l [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]
1805	4.4-j10.8	1.2 - j2.5	19.4	52.30	171	57.6	2.4 - j1.3	21.9	50.10	103	68.4
1842.5	7.4-j13.2	1.2 - j2.7	19.2	52.30	170	56.7	2.1 - j1.5	21.7	50.50	112	67.9
1880	16.8-j14.6	1.2 - j2.9	19.3	52.20	165	55.9	2.1 - j1.7	21.7	50.30	106	65.8

		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Z_s [Ω]	Z_l [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]	Z_l [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]
1805	4.4 - j10.8	1.2 - j2.6	17.3	53.20	209	60.5	2.1 - j1.9	19.3	51.90	155	71.0
1842.5	7.4 - j13.2	1.2 - j2.9	17.2	53.10	204	58.9	2.0 - j1.7	19.5	51.60	144	70.6
1880	16.8 - j14.6	1.3 - j3.0	17.4	53.00	200	59.4	2.0 - j1.9	19.4	51.60	143	69.0

Peak side load pull performance – pulsed CW signal: 10 µsec, 10% duty cycle, 28 V, $V_{GS(PEAK)}$ = 2.4 V, class B

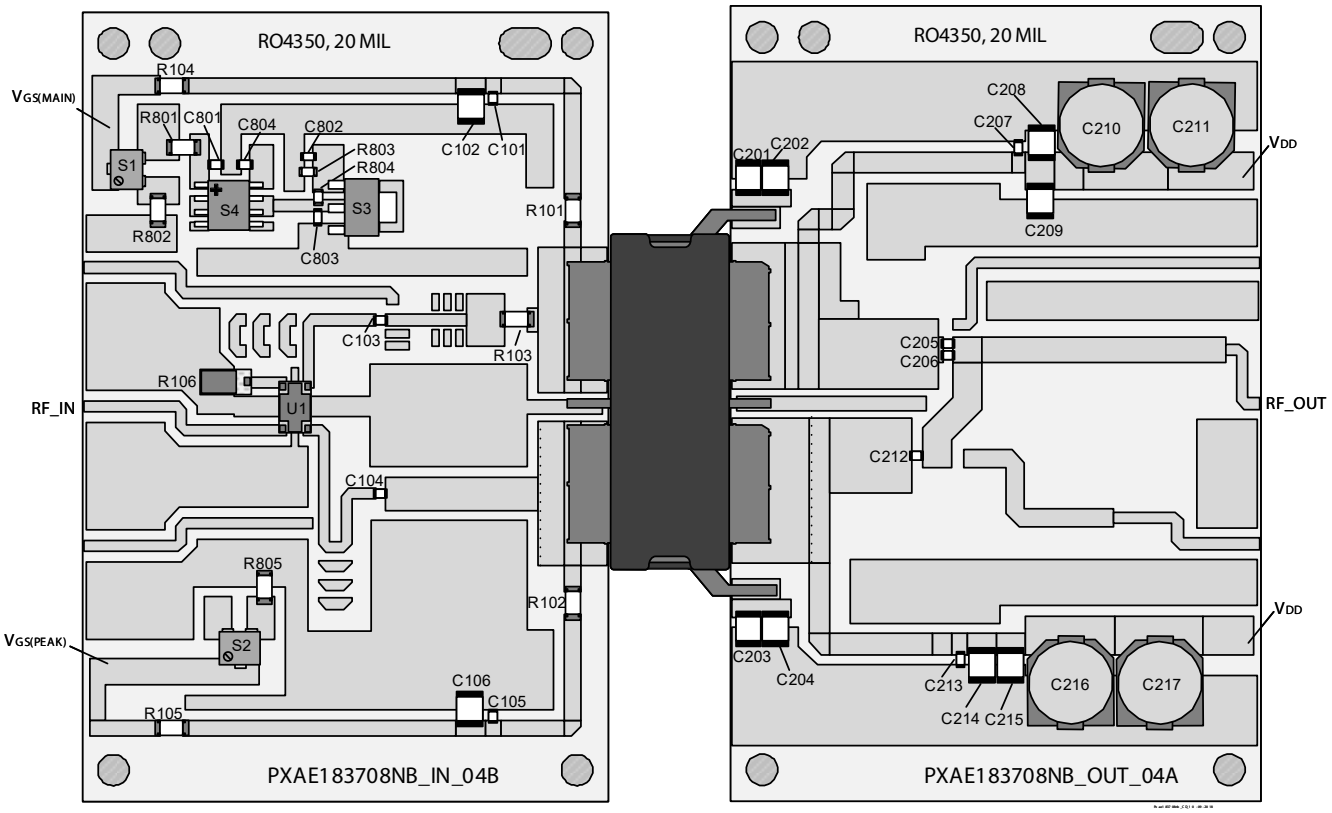
		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Z_s [Ω]	Z_l [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]	Z_l [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]
1805	2.9 - j6.7	2.0 - j4.5	17.4	54.90	306	56.0	2.2 - j1.7	18.9	52.20	164	69.1
1842.5	5.4 - j7.1	2.4 - j4.8	17.6	54.80	305	54.4	2.1 - j2.1	19.2	52.60	181	69.0
1880	8.4 - j4.2	2.4 - j4.9	17.9	54.80	300	55.4	2.1 - j2.2	19.3	52.20	166	68.3

		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Z_s [Ω]	Z_l [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]	Z_l [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]
1805	2.9 - j6.7	2.4 - j4.6	15.3	55.70	369	59.1	2.6 - j2.1	16.7	53.70	234	68.8
1842.5	5.4 - j7.1	2.5 - j4.8	15.6	55.60	366	57.7	2.6 - j2.6	16.9	54.20	260	68.3
1880	8.4 - j4.2	2.9 - 5.1	15.7	55.50	357	57.5	2.5 - j2.7	17.1	53.90	245	68.4

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Reference Circuit, 1805 – 1880 MHz

Test Circuit Part Number	LTA/PXAE183708NB-V1
PCB Information	Rogers 4350, 0.508 mm [0.020”] thick, 2 oz. copper, ε_r = 3.66



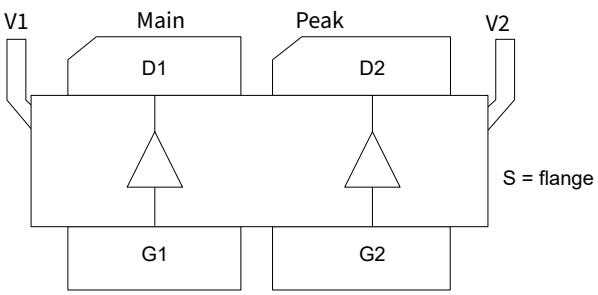
Reference circuit assembly diagram (not to scale)

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Components Information

Component	Description	Manufacturer	P/N
Input			
C101, C105	Capacitor, 33 pF	ATC	ATC800A330JT250XT
C102, C106	Capacitor, 10 µF, 50 V	Taiyo Yuden	UMK325C7106MM-T
C103, C104	Capacitor, 22 pF	ATC	ATC800A220JT250XT
R101, R102	Resistor, 5.1 ohms	Panasonic Electronic Components	ERJ-8GEYJ5R1V
R103, R104, R105	Resistor, 10 ohms	Panasonic Electronic Components	ERJ-8GEYJ100V
R106	Resistor, 50 ohms	Richardson	C16A50Z4
C801,C802, C803, C804	Capacitor, 1000 pF	Murata Electronics North America	GRM188R71H102KA01J
R801	Resistor, 1K ohms	Panasonic Electronic Components	ERJ-8GEYJ102V
R802	Resistor, 51 ohms	Panasonic Electronic Components	ERJ-8GEYJ510V
R803	Resistor, 1.3K ohms	Panasonic Electronic Components	ERJ-3GEYJ132V
R804	Resistor, 1.2K ohms	Panasonic Electronic Components	ERJ-3GEYJ122V
R805	Resistor, 10 ohms	Panasonic Electronic Components	ERJ-8GEYJ100V
S1, S2	Potentiometer, 2K ohms	Bourns Inc.	3224W-1-202E
S3	Voltage Regulator	Texas Instruments	LM78L05ACM
S4	Transistor	Diodes Incorporated	BCP5616TA
U1	Hybrid coupler	Anaren	X3C20F1-02S
Output			
C201, C202, C203, C204, C208, C209, C214, C215	Capacitor, 10 µF, 100 V	TDK Corporation	C5750X7S2A106M230KB
C205, C206	Capacitor, 2.4 pF	ATC	ATC800A2R4CT250XT
C207, C212, C213	Capacitor, 33 pF	ATC	ATC800A330JT250XT
C210, C211, C216, C217	Capacitor, 220 µF	Panasonic Electronic Components	EEE-FP1V221AP

Pinout Diagram (top view)



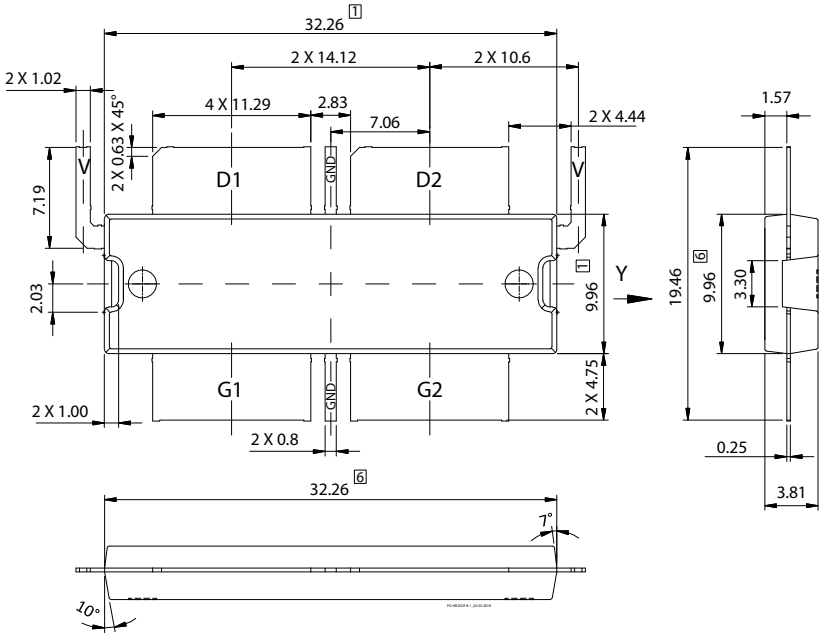
Pin	Description
D1	Drain Device 1 (Main)
D2	Drain Device 2 (Peak)
G1	Gate Device 1(Main)
G2	Gate Device 2 (Peak)
GND	Ground
V1, V2	Drain video decoupling, no DC bias

Lead connections for PXAE183708NB

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Package Outline Specifications – Package PG-HB2SOF-8-1

Top and Side View



Bottom View

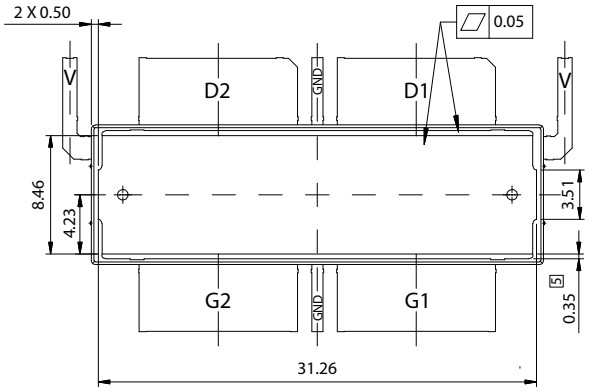


Diagram Notes–unless otherwise specified:

1. Mold/Dam Bar/Metal protusion of 0.30mm max per side not included.
2. Fillets and radii: all radii are 0.3 mm max unless specified otherwise
3. Interpret dimensions and tolerances per ISO 8015
4. Dimensions are mm
5. Exposed metal surface are tin plated, may not be covered by mold compound
6. Does not include mold/dam bar/metal protusion.
7. All tolerances ± 0.1mm unless specified otherwise
9. All metal surfaces pre-plated, except area of cut
9. Lead thickness: 0.25 mm
10. Pins: D1, D2 – drain; G1, G2 – gate; GND – ground; V – Drain video decoupling, no DC bias

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