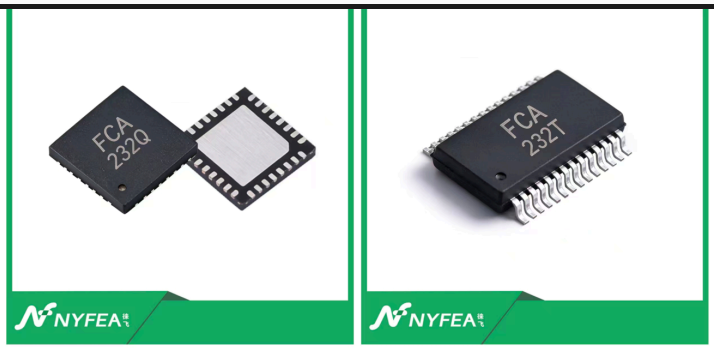
USB UART IC

FCA232Q/FCA232T USB UART IC

USB to Serial UART Interface IC · Datasheet



The FCA232Q (QFN-32) and FCA232T (28-Pin SSOP) are USB to serial UART interface ICs. Both package variants share the same silicon and offer the following advanced features:

- Single chip USB to asynchronous serial data transfer interface.
- Entire USB protocol handled on the chip. No USB specific firmware programming required.
- Fully integrated 1024-bit EEPROM storing device descriptors and CBUS I/O configuration.
- Fully integrated USB termination resistors.
- Fully integrated clock generation with no external crystal required plus optional clock output selection enabling a glue-less interface to external MCU or FPGA.
- Data transfer rates from 300 baud to 3 Mbaud (RS422, RS485, RS232) at TTL levels.
- 128 bytes receive buffer, and 256 bytes transmit buffer utilising buffer smoothing technology to allow for high data throughput.
- NYFEA's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases.
- Unique USB NYFEA-ID™ feature.
- Configurable CBUS I/O pins.
- Transmit and receive LED drive signals.
- UART interface support for 7 or 8 data bits, 1 or 2 stop bits and odd / even / mark / space / no parity.
- FIFO receives and transmits buffers for high data throughput.
- Synchronous and asynchronous bit bang interface options with RD# and WR# strobes.
- Device supplied pre-programmed with unique USB serial number.
- Supports bus powered, self-powered and high-power bus powered USB configurations.
- Integrated +3.3V level converter for USB I/O.
- Integrated level converter on UART and CBUS for interfacing to between +1.8V and +5V logic.
- True 5V/3.3V/2.8V/1.8V CMOS drive output and TTL input.
- Configurable I/O pin output drive strength.
- Integrated power-on-reset circuit.
- Fully integrated AVCC supply filtering – no external filtering required.
- UART signal inversion option.
- +3.3V to +5.25V Single Supply Operation.
- Low operating and USB suspend current.
- Low USB bandwidth consumption.
- UHCI/OHCI/EHCI host controller compatible.
- USB 2.0 Full Speed compatible.
- -40°C to 85°C extended operating temperature range.
- Available in compact Pb-free RoHS compliant QFN-32 and 28-Pin SSOP packages.

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1 Typical Applications

- USB to RS232/RS422/RS485 Converters
- Upgrading Legacy Peripherals to USB
- Cellular and Cordless Phone USB data transfer cables and interfaces
- Interfacing MCU/PLD/FPGA based designs to USB
- USB Audio and Low Bandwidth Video data transfer
- PDA to USB data transfer
- USB Smart Card Readers
- USB Instrumentation
- USB Industrial Control
- USB MP3 Player Interface
- USB FLASH Card Reader and Writers
- Set Top Box PC - USB interface
- USB Digital Camera Interface
- USB Hardware Modems
- USB Wireless Modems
- USB Bar Code Readers
- USB Software and Hardware Encryption Dongles

1.1 Driver Support

Royalty free VIRTUAL COM PORT (VCP) DRIVERS for...	**Royalty free D2XX Direct Drivers (USB Drivers + DLL S/W Interface)**
Windows 11, 64-bit	Windows 11, 64-bit
Windows 10 32,64-bit	Windows 10 32,64-bit
Windows 8/8.1 32,64-bit	Windows 8/8.1 32,64-bit
Windows 7 32,64-bit	Windows 7 32,64-bit
Windows Server 2008 and Server 2012 R2	Server 2008 and Server 2012 R2
Mac OS	Mac OS
Linux 2.4 and greater	Linux 2.4 and greater
Android(J2xx)	—

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All of the drivers listed above can be downloaded free of charge from the NYFEA website. Third-party drivers for additional operating systems are also offered – see the NYFEA website for further details.

1.2 Part Numbers

Table 1.1 – FCA232Q / FCA232T Part Numbers

Part Number	**Package**	**Number of Pins**	**Description**
FCA232Q	QFN-32	32	USB 2.0 Full Speed to serial UART interface IC
FCA232T-xxxx	28 Pin SSOP	28	USB 2.0 Full Speed to serial UART interface IC

Note: The packing code represented by xxxx denotes the following options:

- Reel: Taped and Reel, (SSOP is 2,000pcs per reel).
- Tube: Tube packing, 47pcs per tube (SSOP only).

For example, FCA232T-Reel indicates 2,000 pieces supplied in taped and reel packing.

1.3 USB Compliant

The FCA232Q/FCA232T fully conforms to the USB 2.0 specification and has been assigned USB-IF Test-ID (TID) 6654.

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2 FCA232Q/FCA232T Block Diagram

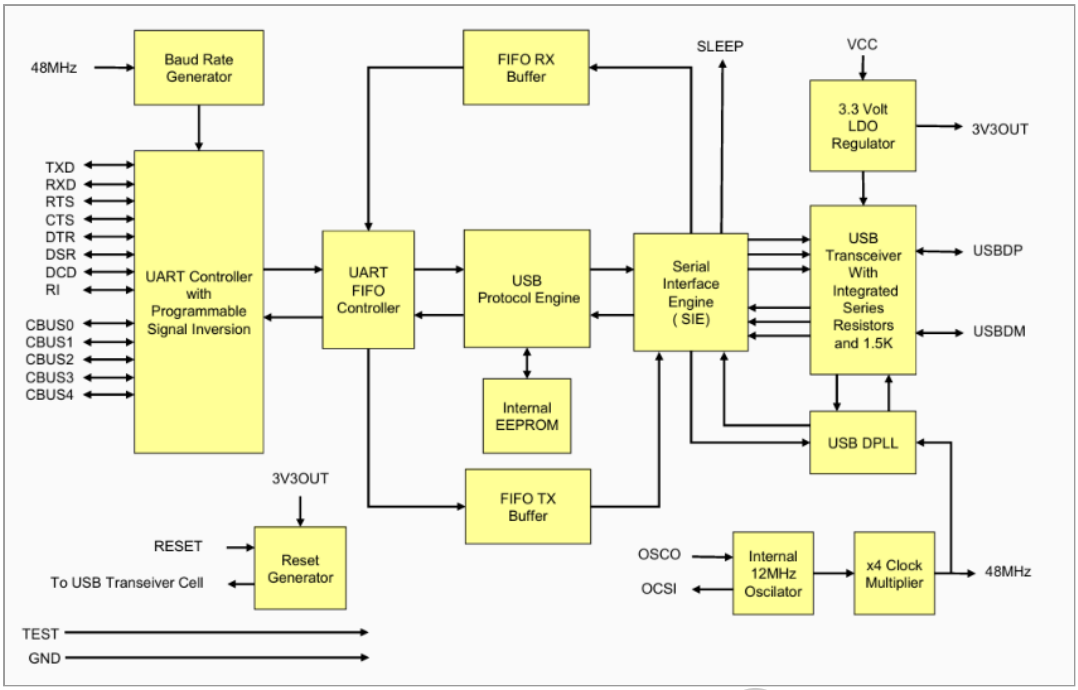


Figure 2.1 – FCA232Q/FCA232T Block Diagram

A description of each functional block can be found in Section 4.

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3 Device Pin Out and Signal Description

3.1 Package Pin Outs

The FCA232Q is supplied in a QFN-32 package and the FCA232T in a 28-LD SSOP package. Figure 3.1 and Figure 3.2 show the pin outs and schematic symbols for the two package variants.

QFN-32 Package

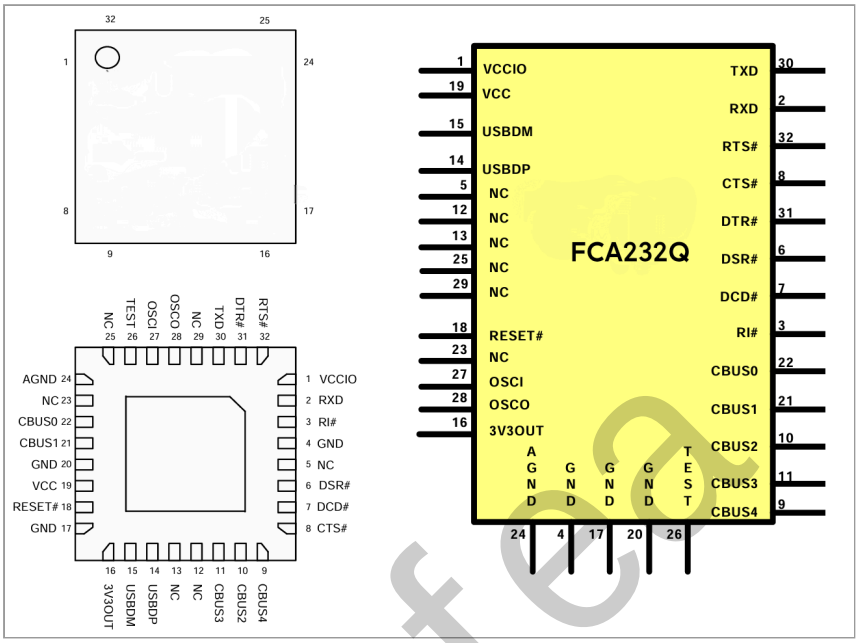


Figure 3.1 – QFN-32 Package Pin Out and Schematic Symbol

28-LD SSOP Package

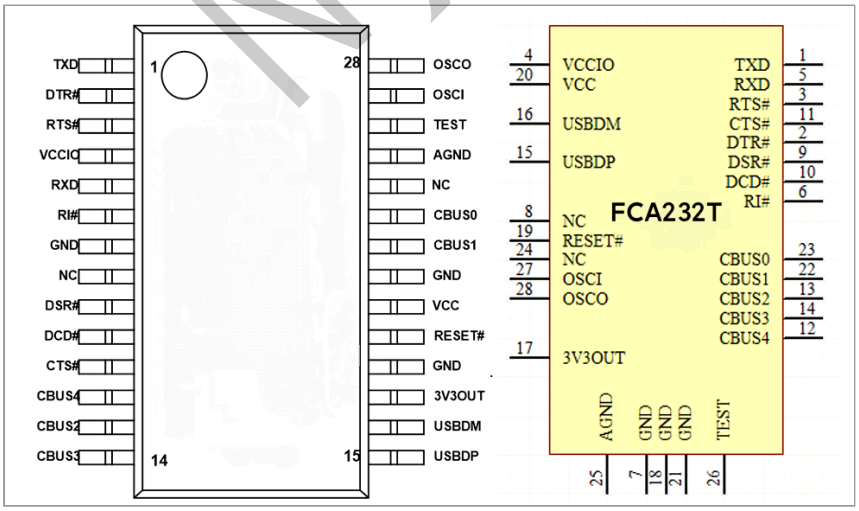


Figure 3.2 – SSOP Package Pin Out and Schematic Symbol

3.2 Signal Descriptions

> **Note:** Throughout this document, active-low signals are identified by appending "#" to the signal name.

Table 3.1 – QFN-32 Package Signal Descriptions

Pin No.	Name	Type	Description
1	TXD	O	Transmit asynchronous data output.
2	DTR#	O	Data Terminal Ready control output / handshake signal.
3	RTS#	O	Request To Send control output / handshake signal.
4	VCCIO	PWR	+1.8 V to +5.25 V supply to the UART interface and CBUS group. Connects the UART / CBUS level converter reference.
5	RXD	I	Receive asynchronous data input.
6	RI#	I	Ring Indicator control input. When remote wake-up is enabled, taking RI# low wakes the host from suspend.
7	GND	PWR	Device ground supply pin.
8	NC	NC	No internal connection. Leave unconnected.
9	DSR#	I	Data Set Ready control input / handshake signal.
10	DCD#	I	Data Carrier Detect control input.
11	CTS#	I	Clear To Send control input / handshake signal.
12	CBUS4	I/O	Configurable CBUS I/O pin. Function is defined by the EEPROM.
13	CBUS2	I/O	Configurable CBUS I/O pin. Function is defined by the EEPROM.
14	CBUS3	I/O	Configurable CBUS I/O pin. Function is defined by the EEPROM.
15	USBDP	I/O	USB data signal plus (D+).
16	USBDM	I/O	USB data signal minus (D–).
17	3V3OUT	O	+3.3 V output from the integrated LDO regulator. Decouple to ground with a 100 nF capacitor.
18	GND	PWR	Device ground supply pin.
19	RESET#	I	Active-low reset input. Pull high (or leave floating) for normal operation.
20	VCC	PWR	+3.3 V to +5.25 V supply to the device core. Decouple to ground with a 100 nF capacitor.
21	GND	PWR	Device ground supply pin.
22	CBUS1	I/O	Configurable CBUS I/O pin. Function is defined by the EEPROM.
23	CBUS0	I/O	Configurable CBUS I/O pin. Function is defined by the EEPROM.
24	AGND	PWR	Analogue ground for the internal clock and USB analogue circuitry.
25	TEST	I	Puts the device into IC test mode. Must be tied to GND for normal operation.
26	OSCI	I	Input pin for an optional external oscillator / clock source.

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Pin No.	Name	Type	Description
27	OSCO	O	Output pin for the optional clock output signal.
28	NC	NC	No internal connection. Leave unconnected.
29	GND	PWR	Device ground supply pin.
30	NC	NC	No internal connection. Leave unconnected.
31	NC	NC	No internal connection. Leave unconnected.
32	NC	NC	No internal connection. Leave unconnected.

SSOP Package Pin Out Description

Table 3.2 – USB Interface Group

Pin No.	Name	Type	Description
15	USBDP	I/O	USB Data Signal Plus, incorporating internal series resistor and 1.5kΩ pull up resistor to 3.3V.
16	USBDM	I/O	USB Data Signal Minus, incorporating internal series resistor.

Table 3.3 – Power and Ground Group

Pin No.	Name	Type	Description
4	VCCIO	PWR	+1.8V to +5.25V supply to the UART Interface and CBUS group pins (1...3, 5, 6, 9...14, 22, 23). In USB bus powered designs connect this pin to 3V3OUT pin to drive out at +3.3V levels or connect to VCC to drive out at 5V CMOS level. This pin can also be supplied with an external +1.8V to +2.8V supply to drive outputs at lower levels. It should be noted that in this case this supply should originate from the same source as the supply to VCC. This means that in bus powered designs a regulator which is supplied by the +5V on the USB bus should be used.
7, 18, 21	GND	PWR	Device ground supply pins
17	3V3OUT	Output	+3.3V output from integrated LDO regulator. This pin should be decoupled to ground using a 100nF capacitor. The main usage of this pin is to provide the internal +3.3V supply to the USB transceiver cell and the internal 1.5kΩ pull up resistor on USBDP. Up to 50mA can be drawn from this pin to power external logic if required. This pin can also be used to supply the VCCIO pin.
20	VCC	PWR	+3.3V to +5.25V supply to the device core.
25	AGND	PWR	Device analogue ground supply for internal clock multiplier

Table 3.4 – Miscellaneous Signal Group

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Pin No.	Name	Type	Description
8, 24	NC	NC	No internal connection
19	RESET#	Input	Active low reset pin. This can be used by an external device to reset the FCA232Q/FCA232T. If not required can be left unconnected or pulled up to VCC.
26	TEST	Input	Puts the device into IC test mode. Must be tied to GND for normal operation, otherwise the device will appear to fail.
27	OSCI	Input	Input 12MHz Oscillator Cell. Optional – Can be left unconnected for normal operation. (See Note 1)
28	OSCO	Output	Output from 12MHZ Oscillator Cell. Optional – Can be left unconnected for normal operation if internal Oscillator is used. (See Note 1)

Table 3.5 – UART Interface and CBUS Group (see note 2)

Pin No.	Name	Type	Description
1	TXD	Output	Transmit Asynchronous Data Output.
2	DTR#	Output	Data Terminal Ready Control Output / Handshake Signal.
3	RTS#	Output	Request to Send Control Output / Handshake Signal.
5	RXD	Input	Receiving Asynchronous Data Input.
6	RI#	Input	Ring Indicator Control Input. When remote wake up is enabled in the internal EEPROM taking RI# low (20ms active low pulse) can be used to resume the PC USB host controller from suspend.
9	DSR#	Input	Data Set Ready Control Input / Handshake Signal.
10	DCD#	Input	Data Carrier Detect Control Input.
11	CTS#	Input	Clear To Send Control Input / Handshake Signal.
12	CBUS4	I/O	Configurable CBUS output only Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is SLEEP#. See CBUS Signal Options, Table 3.6.
13	CBUS2	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is TXDEN. See CBUS Signal Options, Table 3.6.
14	CBUS3	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is PWREN#. See CBUS Signal Options, Table 3.6. PWREN# should be used with a 10kΩ resistor pull up.
22	CBUS1	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is RXLED#. See CBUS Signal Options, Table 3.6.
23	CBUS0	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is TXLED#. See CBUS Signal Options, Table 3.6.

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Notes:

1. Refer to Section 7.6 for information on operating the FCA232Q/FCA232T with an external crystal, ceramic resonator, or oscillator.
2. In input mode, each input pin is pulled to VCCIO through an internal 200kΩ resistor. Setting an option in the internal EEPROM allows these pins to be programmed to gently pull low during USB suspend (PWREN# = "1").

3.3 CBUS Signal Options

The options below can be assigned to the CBUS I/O pins. They are programmed into the internal EEPROM using the FT_PROG utility, which is available for download from the NYFEA Utilities page. Section 8 describes the factory default configuration.

Table 3.6 – CBUS Configuration Control

CBUS Signal Option	Available On CBUS Pin	Description
TXDEN	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Enable transmit data for RS485
PWREN#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Output is low after the device has been configured by USB, then high during USB suspending mode. This output can be used to control power to external logic P-Channel logic level MOSFET switch. Enable the interface pull-down option when using the PWREN# in this way. *
TXLED#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Transmit data LED drive: Data from USB Host to FCA232Q/FCA232T. Pulses low when transmitting data via USB. See Section 7.5 for more details.
RXLED#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Receive data LED drive: Data from FCA232Q/FCA232T to USB Host. Pulses low when receiving data via USB. See Section 7.5 for more details.
TX&RXLED#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	LED drive – pulses low when transmitting or receiving data via USB. See Section 7.5 for more details.
SLEEP#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Goes low during USB suspend mode. Typically used to power down an external TTL to RS232 level converter IC in USB to RS232 converter designs.
CLK48	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	48MHz ±0.7% Clock output. **
CLK24	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	24 MHz Clock output. **

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CBUS Signal Option	Available On CBUS Pin	Description
CLK12	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	12 MHz Clock output. **
CLK6	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	6 MHz ±0.7% Clock output. **
CBitBangI/O	CBUS0, CBUS1, CBUS2, CBUS3	CBUS bit bang mode option. Allows up to 4 of the CBUS pins to be used as general purpose I/O. Configured individually for CBUS0, CBUS1, CBUS2 and CBUS3 in the internal EEPROM. A separate application note, AN232R-01, available from NYFEA website describes in more detail how to use CBUS bit bang mode.
BitBangWRn	CBUS0, CBUS1	Synchronous and asynchronous bit bang mode WR# strobe output.
BitBangRDn	CBUS0, CBUS1, CBUS2, CBUS3	Synchronous and asynchronous bit bang mode RD# strobe output.

* PWREN# requires a 10kΩ pull-up resistor.

** The clock outputs are also suspended while the device is in USB suspend mode.

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4 Function Description

The FCA232Q/FCA232T is a USB-to-serial UART bridge that streamlines USB-to-serial designs and lowers the external component count by integrating an EEPROM, USB termination resistors, and a clock circuit that needs no external crystal. It is engineered to work efficiently with a USB host controller while consuming as little of the available USB bandwidth as possible.

4.1 Key Features

Functional Integration. The device integrates the EEPROM, USB termination resistors, clock generation, AVCC filtering, power-on reset (POR), and an LDO regulator.

Configurable CBUS I/O Pin Options. The integrated EEPROM enables configuration of the Control Bus (CBUS) functions, signal inversion, and drive strength. Five CBUS I/O pins are configurable, with the following options –

1. TXDEN - transmit enable for RS485 designs.
2. PWREN# - Power control for high power, bus powered designs.
3. TXLED# - for pulsing an LED upon transmission of data.
4. RXLED# - for pulsing an LED upon receiving data.
5. TX&RXLED# - which will pulse an LED upon transmission OR reception of data.
6. SLEEP# - indicates that the device going into USB suspend mode.
7. CLK48 / CLK24 / CLK12 / CLK6 - 48MHz, 24MHz, 12MHz, and 6MHz clock output signal options.
8. BitBangWRn / BitBangRDn - Synchronous and asynchronous bit bang mode WR# / RD# strobe outputs.

The CBUS pins can also be set individually as GPIO pins, much like asynchronous bit bang mode. This mode can be used at the same time as the UART interface, giving up to four general-purpose I/O pins during normal operation. Application note AN232R-01, available from the NYFEA website, covers this feature.

Any of the above output options can be assigned to the CBUS lines by setting bits in the internal EEPROM. The device ships with the most common pin definitions already programmed – see Section 8 for details.

Asynchronous Bit Bang Mode with RD# and WR# Strobes. The FCA232Q/FCA232T supports the bit-bang mode of NYFEA's earlier chip generation. In bit-bang mode, the eight UART lines switch from their regular interface function to an 8-bit general-purpose I/O port. Data packets written to the device are output to the interface in sequence, paced by an internal timer (equivalent to the baud rate pre-scaler). In the FCA232Q/FCA232T this mode is enhanced by exposing the internal RD# and WR# strobe signals, which can clock external logic in step with accesses to the bit-bang I/O bus. This option is described more fully in application note AN232R-01, available from the NYFEA website.

Synchronous Bit Bang Mode. The FCA232Q/FCA232T also supports synchronous bit bang mode. Unlike asynchronous bit bang mode, the interface pins are read only when the device is written to. Because the returned data is synchronous with the output data, the controlling program can more easily measure the response to an output stimulus. Application note AN232R-01, available from the NYFEA website, describes this feature.

NYFEA-ID™. The FCA232Q/FCA232T also includes the NYFEA-ID™ security dongle feature. During manufacture, a unique number is permanently burnt into each device and cannot be reprogrammed. This number is readable only over USB and serves as the basis of a security dongle that can guard customer application software against copying, allowing the FCA232Q/FCA232T to be used in a dongle for software

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licensing. In addition, a renewable license scheme can be built around the NYFEA-ID™ number by encrypting it with other information; the encrypted value can be stored in the user area of the internal EEPROM and later decrypted and compared with the protected NYFEA-ID™ to verify that a license is valid. Web-based applications can maintain product licensing in this way. Application note AN232R-02, available from the NYFEA website, describes this feature.

The FCA232Q/FCA232T operates from a supply of +3.3V to +5V, drawing a nominal 15mA in normal operation and 70µA in USB suspend mode. This leaves generous margin for peripheral designs to satisfy the 2.5mA USB suspend current limit. A built-in level converter in the UART interface lets the FCA232Q/FCA232T connect to UART logic running at +1.8V, +2.8V, +3.3V, or +5V.

4.2 Functional Block Descriptions

The paragraphs below describe each function inside the FCA232Q/FCA232T. See the block diagram in Figure 2.1.

Internal EEPROM. The internal EEPROM stores the USB Vendor ID (VID), Product ID (PID), device serial number, product description string, and other USB configuration descriptors. It also configures the CBUS pin functions. The FCA232Q/FCA232T ships with the internal EEPROM pre-programmed as described in Section 8, and a user area is provided so system designers can store additional data. The EEPROM descriptors can be programmed in-circuit over USB with no extra voltage needed, using the NYFEA utility FT_PROG, downloadable from NYFEA Utilities on the NYFEA website.

+3.3V LDO Regulator. The +3.3V LDO regulator produces the +3.3V reference used to drive the USB transceiver output buffers. It needs an external decoupling capacitor on the 3V3OUT output pin, and it also powers the internal 1.5kΩ pull-up resistor on USBDP. Although the LDO is primarily intended to supply the USB transceiver and reset generator cells rather than external logic, it can provide up to 50mA to external circuitry needing a nominal +3.3V supply.

USB Transceiver. The USB Transceiver Cell supplies the USB 1.1 / USB 2.0 full-speed physical interface to the USB cable. Its output drivers deliver +3.3V slew-rate-controlled signalling, while a differential input receiver and two single-ended input receivers detect USB data, Single-Ended-0 (SE0), and USB reset conditions respectively. This block also contains the internal series termination resistors on the USB data lines and a 1.5kΩ pull-up resistor on USBDP.

USB DPLL. The USB DPLL cell locks onto the incoming NRZI USB data and produces recovered clock and data signals for the Serial Interface Engine (SIE).

Internal 12MHz Oscillator. The internal 12MHz oscillator cell produces a 12MHz reference clock that feeds the x4 clock multiplier. This same 12MHz clock also serves as the reference for the SIE, USB Protocol Engine, and UART FIFO controller blocks.

Clock Multiplier / Divider. The clock multiplier / divider takes the 12MHz input from the internal oscillator and derives the 48MHz, 24MHz, 12MHz, and 6MHz reference clocks. The 48MHz reference is used by the USB DPLL and the baud rate generator.

Serial Interface Engine (SIE). The SIE block converts USB data between parallel and serial forms. As required by the USB 2.0 specification, it performs bit stuffing/un-stuffing and CRC5/CRC16 generation, and it also verifies the CRC on the USB data stream.

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USB Protocol Engine. The USB Protocol Engine manages the data flow from the device's USB control endpoint. It handles the low-level USB protocol requests from the host controller as well as the commands that set the UART's functional parameters, in line with USB 2.0 specification chapter 9.

FIFO RX Buffer (128 bytes). Data sent from the USB host controller to the UART through the USB data OUT endpoint is held in the FIFO RX (receive) buffer. Under the control of the UART FIFO controller, data is moved from this buffer to the UART transmit register (Rx is relative to the USB interface).

FIFO TX Buffer (256 bytes). Data from the UART receive register is held in the TX buffer. The USB host controller retrieves this data by issuing a USB request on the device data IN endpoint (Tx is relative to the USB interface).

UART FIFO Controller. The UART FIFO controller supervises data movement between the FIFO RX/TX buffers and the UART transmit/receive registers.

UART Controller with Programmable Signal Inversion and High Drive. Working with the UART FIFO controller, the UART controller moves data between the FIFO RX/TX buffers and the UART transmit/receive registers. It carries out asynchronous 7- or 8-bit parallel-to-serial and serial-to-parallel conversion of the data on the RS232 (or RS422/RS485) interface.

UART mode supports the control signals RTS, CTS, DSR, DTR, DCD, and RI. The UART controller also offers a transmitter-enable signal option (TXDEN) for interfacing to RS485 transceivers, along with RTS/CTS, DSR/DTR, and XON/XOFF handshaking. Handshaking is handled in hardware for fast response times. The UART interface additionally supports RS232 BREAK setting and detection.

Each UART signal can also be individually inverted and assigned a configurable high drive strength. Both features are set through the EEPROM.

Baud Rate Generator. The baud rate generator supplies a 16x clock to the UART controller from the 48MHz reference clock. It comprises a 14-bit pre-scaler plus 3 register bits for fine tuning, enabling division by a whole number plus a fraction (a "sub-integer"). This sets the UART baud rate, which is programmable from 183 baud to 3 Mbaud.

The FCA232Q/FCA232T supports every standard baud rate as well as non-standard rates between 183 baud and 3 Mbaud. Achievable non-standard rates are given by –

$$\text{Baud Rate} = 3000000 / (n + x)$$

Here 'n' is any integer from 2 to 16,384 (= 2^{14}), and 'x' is a sub-integer chosen from 0, 0.125, 0.25, 0.375, 0.5, 0.625, 0.75, or 0.875. When n = 1, x = 0, meaning baud rate divisors between 1 and 2 are not possible.

This yields achievable baud rates from 183.1 baud up to 3,000,000 baud. To use a non-standard rate, simply pass the desired value to the driver; the NYFEA driver works out the needed divisor and applies it. See application note AN_120 on the NYFEA website for more details.

RESET Generator. The integrated reset generator cell reliably resets the device's internal circuitry at power-up. The RESET# input lets an external device reset the FCA232Q/FCA232T; if unused, RESET# may be tied to VCC or left unconnected.

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5 Devices Characteristics and Ratings

5.1 Absolute Maximum Ratings

The absolute maximum ratings for the FCA232Q/FCA232T are listed below. These limits follow the Absolute Maximum Rating System (IEC 60134), and operating beyond them may result in permanent damage to the device.

Table 5.1 – Absolute Maximum Ratings

Parameter	Value	Units
Storage Temperature	-65 to 150	°C
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 (IPC/JEDEC J-STD-033A MSL Level 3 Compliant) *	Hours
Ambient Temperature (Power Applied)	-40 to 85	°C
VCC Supply Voltage	-0.5 to +6.00	V
DC Input Voltage – USBDP and USBDM	-0.5 to +3.8	V
DC Input Voltage – High Impedance Bidirectional	-0.5 to + (VCC +0.5)	V
DC Input Voltage – All Other Inputs	-0.5 to + (VCC +0.5)	V
DC Output Current – Outputs	24	mA
DC Output Current – Low Impedance Bidirectional	24	mA
Power Dissipation (VCC = 5.25V)	500	mW

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

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5.2 DC Characteristics

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Table 5.2 – Operating Voltage and Current

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCC1	VCC Operating Supply Voltage	3.3	—	5.25	V	Normal Operation
VCC2	VCCIO Operating Supply Voltage	1.8	—	5.25	V	—
Icc1	Operating Supply Current	—	15	—	mA	Normal Operation
Icc2	Operating Supply Current	50	70	100	µA	USB Suspend
3V3	3.3v regulator output	3.0	3.3	3.6	V	—

Table 5.3 – UART and CBUS I/O Pin Characteristics (VCCIO = +5.0V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 2mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 2mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.4 – UART and CBUS I/O Pin Characteristics (VCCIO = +3.3V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.2	2.7	3.2	V	I source = 1mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.5 – UART and CBUS I/O Pin Characteristics (VCCIO = +2.8V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.1	2.6	2.8	V	I source = 1mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.6 – UART and CBUS I/O Pin Characteristics (VCCIO = +1.8V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	1.32	1.62	1.8	V	I source = 0.2mA
Vol	Output Voltage Low	0.06	0.1	0.18	V	I sink = 0.5mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.7 – UART and CBUS I/O Pin Characteristics (VCCIO = +5.0V, High Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 6mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 6mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

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Table 5.8 – UART and CBUS I/O Pin Characteristics (VCCIO = +3.3V, High Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.2	2.8	3.2	V	I source = 3mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.9 – UART and CBUS I/O Pin Characteristics (VCCIO = +2.8V, High Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.1	2.6	2.8	V	I source = 3mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.10 – UART and CBUS I/O Pin Characteristics (VCCIO = +1.8V, High Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	1.35	1.67	1.8	V	I source = 0.4mA
Vol	Output Voltage Low	0.12	0.18	0.35	V	I sink = 3mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

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** Only input pins have an internal 200KΩ pull-up resistor to VCCIO

Table 5.11 – RESET# and TEST Pin Characteristics

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Vin	Input Switching Threshold	1.3	1.6	1.9	V	—
VHys	Input Switching Hysteresis	50	55	60	mV	—

Table 5.12 – USB I/O Pin (USBDP, USBDM) Characteristics

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
UVoh	I/O Pins Static Output (High)	2.8	—	3.6	V	RI = 1.5kΩ to 3V3OUT (D+) RI = 15KΩ to GND (D-)
UVol	I/O Pins Static Output (Low)	0	—	0.3	V	RI = 1.5kΩ to 3V3OUT (D+) RI = 15kΩ to GND (D-)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
UVse	Single Ended Rx Threshold	0.8	—	2.0	V	—
UCom	Differential Common Mode	0.8	—	2.5	V	—
UVDif	Differential Input Sensitivity	—	—	0.2	V	—
UDrvZ	Driver Output Impedance	26	29	44	Ohms	—

5.3 EEPROM Reliability Characteristics

The internal 1024-bit EEPROM offers the reliability characteristics listed below:

Table 5.13 – EEPROM Characteristics

Parameter	Value	Units
Data Retention	10	Years
Write	10,000	Cycles
Read	Unlimited	Cycles

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5.4 Internal Clock Characteristics

The internal clock oscillator is characterised as follows:

Table 5.14 – Internal Clock Characteristics

Parameter	Minimum	Typical	Maximum	Unit
Frequency of Operation (see Note 1)	11.98	12.00	12.02	MHz
Clock Period	83.19	83.33	83.47	ns
Duty Cycle	45	50	55	%

Note 1: Equivalent to +/-1667ppm

Table 5.15 – OSCI, OSCO Pin Characteristics – see Note 1

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	—	1.57	—	V	I source = 0.2mA
Vol	Output Voltage Low	—	0.25	—	V	I sink = 0.2mA
Vin	Input Switching Threshold	—	0.8	—	V	—

Note: As supplied, the FCA232Q/FCA232T is configured to use its internal clock oscillator; the figures above apply only when an external oscillator or crystal is employed.

5.5 Thermal Characteristics

The QFN-32 and SSOP-28 package variants exhibit the thermal characteristics listed below:

Table 5.16 – QFN-32 Package Thermal Characteristics

Parameter	Value	Unit
Junction-to-ambient thermal resistance (θJA)	40	°C/W
Maximum junction temperature	125	°C

Table 5.17 – SSOP-28 Package Thermal Characteristics

Parameter	Value	Units	Remark
Theta JA (ΘJA)	81.36	°C/W	Estimated value for reference only
Theta JC (ΘJC)	49.58	°C/W	Estimated value for reference only

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6 USB Power Configurations

The sections below describe several possible USB power configurations for the FCA232Q/FCA232T. Pin numbers have been omitted from the diagrams for clarity; see Section 3 for the pin-out and signal descriptions.

6.1 USB Bus Powered Configuration

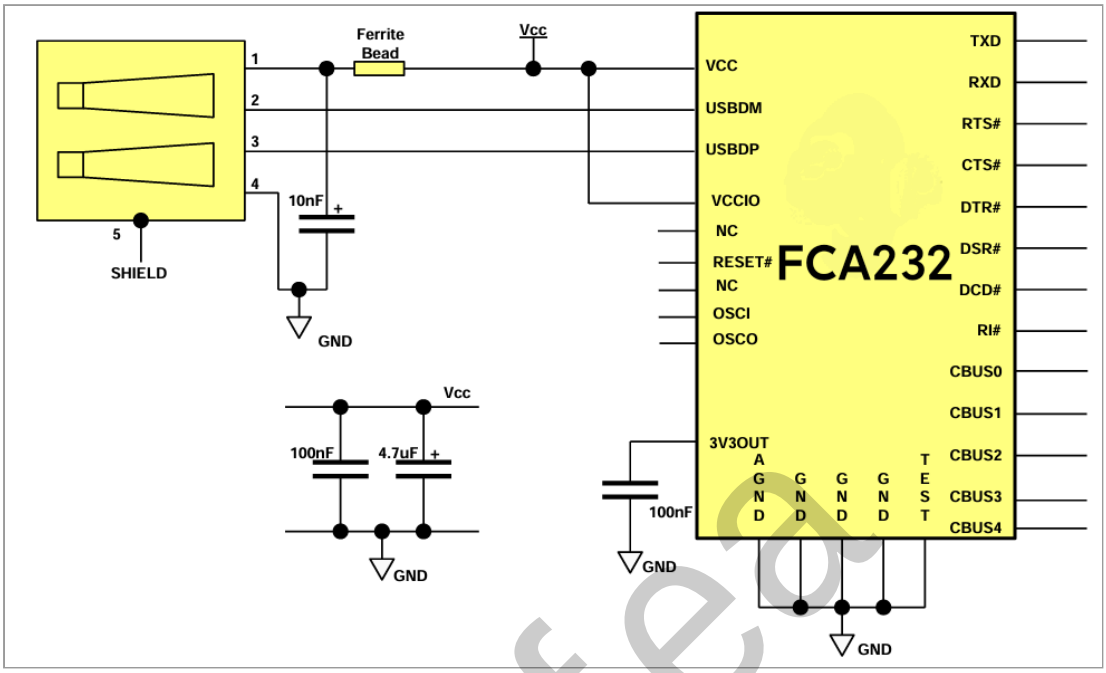


Figure 6.1 – Bus Powered Configuration

Figure 6.1 shows the FCA232Q/FCA232T in a typical USB bus-powered configuration. A bus-powered device draws its supply from the USB bus. The basic rules that apply to USB bus-powered devices are as follows:

i. On plug-in to USB, the device should draw no more current than 100mA.
ii. In USB Suspend mode the device should draw no more than 2.5mA.
iii. A bus powered high power USB device (one that draws more than 100mA) should use one of the CBUS pins configured as PWREN# and use it to keep the current below 100mA on plug-in and 2.5mA on USB suspend.
iv. A device that consumes more than 100mA cannot be plugged into a USB bus powered hub.
v. No device can draw more than 500mA from the USB bus.

The power descriptors in the FCA232Q/FCA232T's internal EEPROM should be programmed to reflect the current the device actually draws.

A ferrite bead is placed in series with the USB power supply to suppress EMI noise from the FCA232Q/FCA232T and surrounding circuitry that might otherwise be radiated along the USB cable to the host. The required bead value depends on the total current drawn by the application. A suitable range of ferrite beads is available from Laird (www.laird.com); for example, Laird part # MI0805K400R-10.

> **Note:** If PWREN# is used (available through the CBUS), the pin should be pulled up to VCCIO with a 10kΩ resistor.

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6.2 Self Powered Configuration

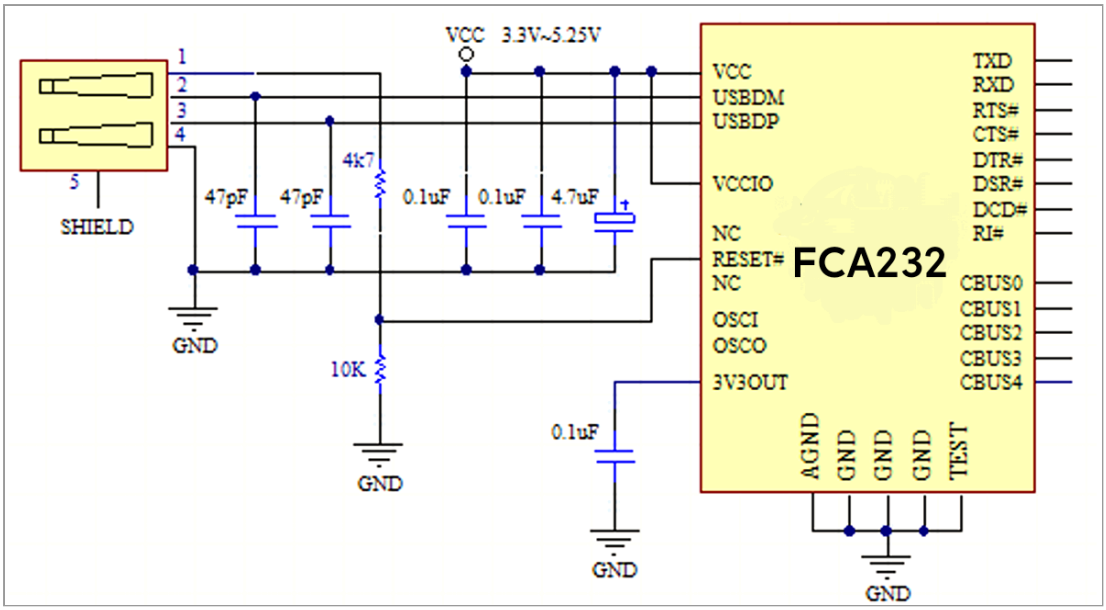


Figure 6.2 – Self-Powered Configuration

Figure 6.2 shows the FCA232Q/FCA232T in a typical USB self-powered configuration. A self-powered device is supplied from its own VCC source rather than drawing current from the USB bus. The basic rules that apply to USB self-powered devices are as follows:

i. A self-powered device should not force current down the USB bus when the USB host or hub controller is powered down.
ii. A self-powered device can use as much current as it needs during normal operation and USB suspend as it has its own power supply.
iii. A self-powered device can be used with any USB host, a bus powered USB hub or a self-powered USB hub.

The power descriptor in the FCA232Q/FCA232T's internal EEPROM should be set to zero (self-powered).

To satisfy the first requirement above, the USB bus power (pin 1) is used to drive the RESET# pin of the FCA232Q/FCA232T. When the USB host or hub is powered up, an internal 1.5kΩ resistor on USBDP is pulled up to +3.3V (produced by the 4K7 and 10k resistor network), causing the device to be recognised as a full-speed device. When the host or hub is powered off, RESET# goes low and the FCA232Q/FCA232T is held in reset; because RESET# is low, the internal 1.5kΩ resistor is no longer pulled up to any supply, so no current flows through the USBDP pull-up resistor. Failing to implement this can cause some host or hub controllers to power up erratically.

Figure 6.2 shows a self-powered design supplied from +3.3V to +5.25V.

Note:

1. When the FCA232Q/FCA232T is in reset, the UART interface I/O pins are tri-stated. Input pins have internal 200kΩ pull-up resistors to VCCIO, so they will gently pull high unless driven by some external logic.
2. Any design which interfaces to +3.3 V or +1.8V would be having a +3.3V or +1.8V supply to VCCIO.

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6.3 USB Bus Powered with Power Switching Configuration

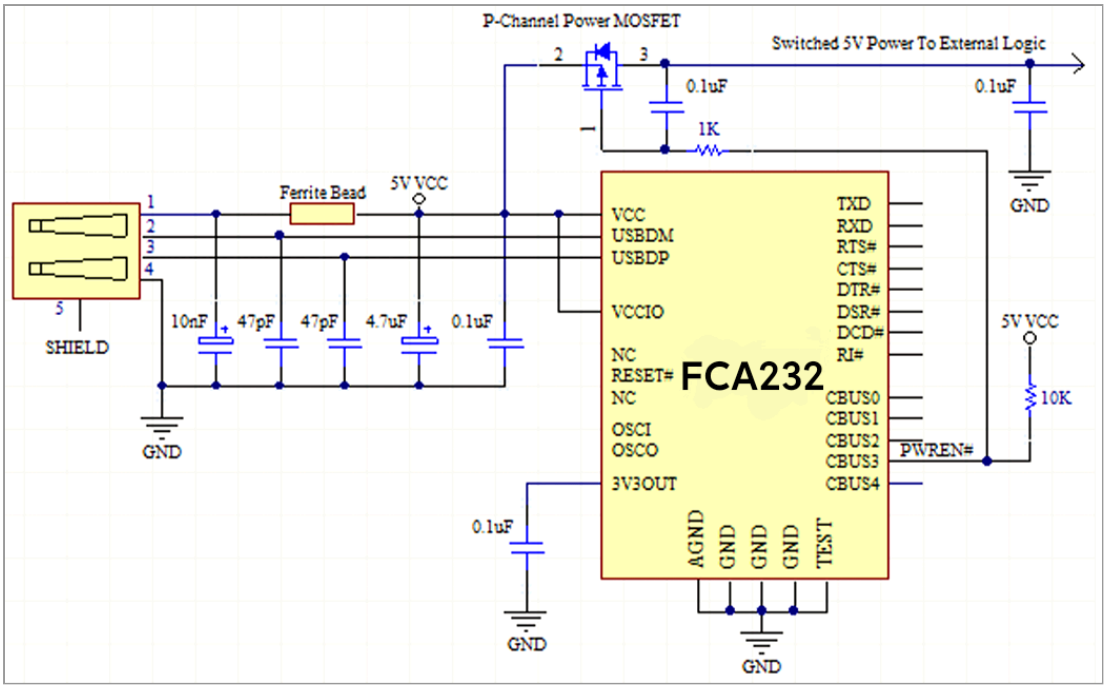


Figure 6.3 – Bus Powered with Power Switching Configuration

USB bus-powered applications must draw less than 2.5mA in total during USB suspend mode, a limit that also covers external logic. Some external logic can enter a low-current state by monitoring PWREN#. For logic that cannot power itself down in this manner, the FCA232Q/FCA232T offers a simple yet effective way to remove power during suspend.

Figure 6.3 shows how a discrete P-channel MOSFET can control the power supplied to external logic. A suitable part is the International Rectifier (www.irf.com) IRLML6402 or an equivalent. A "soft start" circuit, made up of a 1kΩ series resistor and a 0.1µF capacitor, is recommended to limit the inrush current when the MOSFET switches on; without it, the transient surge could reset the FCA232Q/FCA232T or the USB host/hub controller. The example soft start circuit in Figure 6.3 provides a slew rate of roughly 12.5V/ms, so the external logic supply ramps from GND to +5V in about 400 microseconds.

As an alternative to the MOSFET, a dedicated power-switch IC with built-in "soft-start" can be used. A suitable choice for this application is the Micrel (www.micrel.com) MIC2025-2BM or an equivalent.

For designs using power switching, note the following:

i. The external logic to which the power is being switched should have its own reset circuitry to automatically reset the logic when power is re-applied when moving out of suspend mode.
ii. Set the Pull-down on Suspend option in the internal FCA232Q/FCA232T EEPROM.
iii. One of the CBUS Pins should be configured as PWREN# in the internal FCA232Q/FCA232T EEPROM and used to switch the power supply to the external circuitry. This should be pulled high through a 10 kΩ resistor.
iv. For USB high-power bus powered applications (one that consumes greater than 100mA, and up to 500mA of current from the USB bus), the power consumption of the application must be set in the Max Power field in the internal FCA232Q/FCA232T EEPROM. A high-power bus powered application uses the descriptor in the internal FCA232Q/FCA232T EEPROM to inform the system of its power requirements.

v. PWREN# gets its VCC from VCCIO. For designs using 3V3 logic, ensure VCCIO is not powered down using the external logic. In this case use the +3V3OUT.

6.4 USB Bus Powered with Selectable External Logic Supply

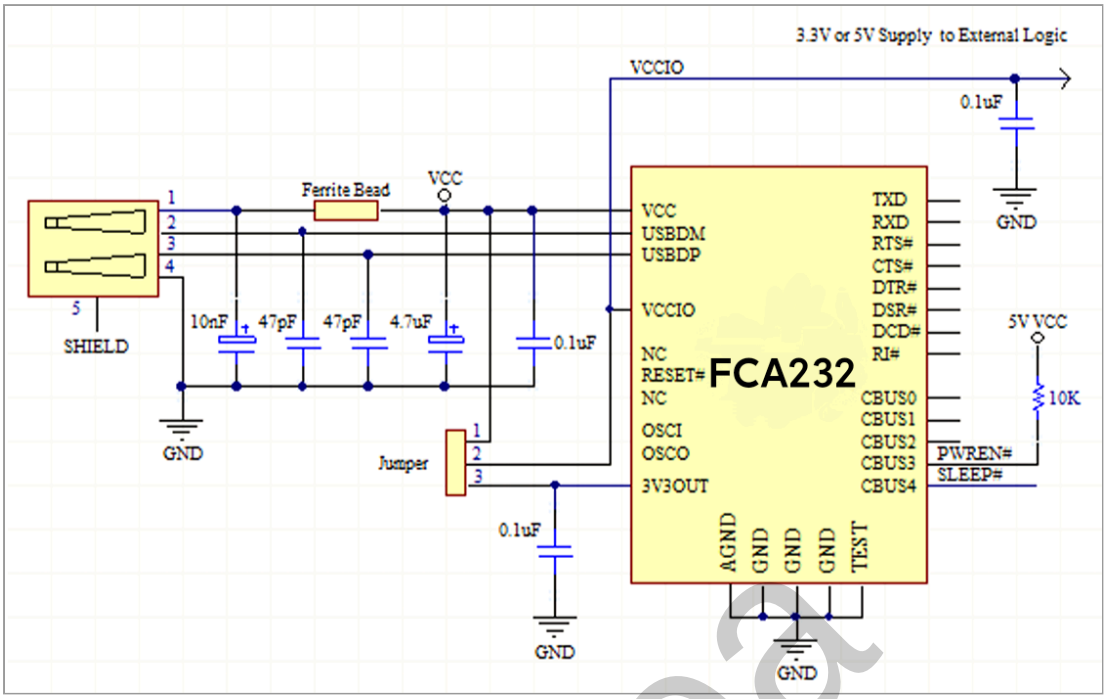


Figure 6.4 – USB Bus Powered with +3.3V or +5V External Logic Power Supply

Figure 6.4 shows a USB bus-powered application with a selectable external logic supply. A jumper switch selects between +3.3V and +5V, allowing the FCA232Q/FCA232T to interface with +3.3V or +5V logic. The VCCIO pin is fed either with +5V from the USB bus (jumper pins 1 and 2 connected) or with +3.3V from the FCA232Q/FCA232T's 3V3OUT pin (jumper pins 2 and 3 connected). This same VCCIO supply also powers the external logic.

For bus-powered applications, note the following:

i. To comply with the 2.5mA current supply limit during USB suspend mode, PWREN# or SLEEP# signals should be used to power down external logic in this mode. If this is not possible, use the configuration shown in Section 6.3.
ii. The maximum current sourced from the USB bus during normal operation should not exceed 100mA, otherwise a bus powered design with power switching (Section 6.3) should be used.

Another configuration option uses a discrete low-dropout (LDO) regulator powered by the 5V USB bus to deliver between +1.8V and +2.8V to the VCCIO pin and the external logic. In this case VCC is fed with the +5V USB supply, while VCCIO is taken from the LDO output, so the FCA232Q/FCA232T I/O pins drive out at between +1.8V and +2.8V logic levels.

When choosing a regulator for a USB bus-powered application, consider the following:

i. The regulator must be capable of sustaining its output voltage with an input voltage of +4.35V. A Low Drop Out (LDO) regulator should be selected.
ii. The quiescent current of the regulator must be low enough to meet the total current requirement of <= 2.5mA during USB suspend mode.

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A suitable range of LDO regulators that meets these requirements is the MicroChip/Telecom (www.microchip.com) TC55 series. These devices can source up to 250mA and draw a quiescent current of under 1μA.

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7 Application Examples

The sections below describe possible applications of the FCA232Q/FCA232T. Pin numbers have been omitted from the diagrams for clarity.

7.1 USB to RS232 Converter

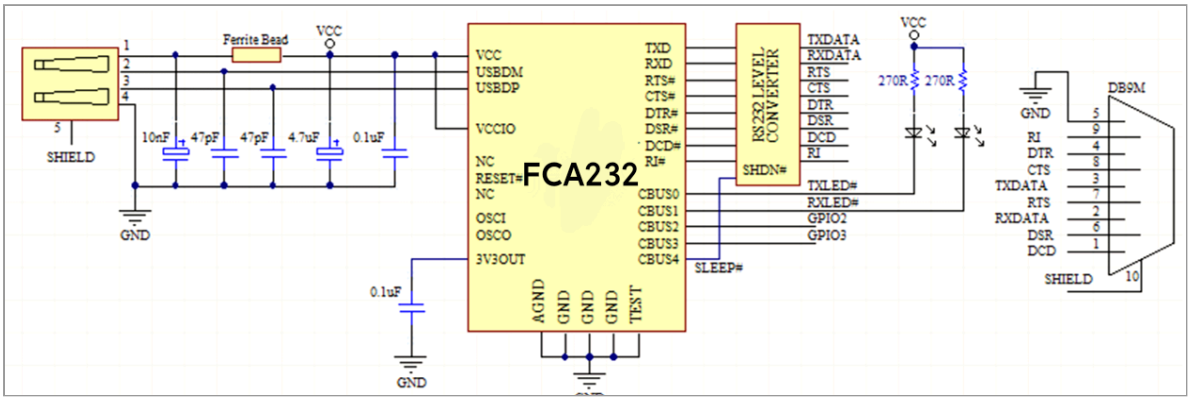


Figure 7.1 – Application Example showing USB to RS232 Converter

Figure 7.1 shows an example of using the FCA232Q/FCA232T as a USB-to-RS232 converter. In this application, a TTL-to-RS232 level converter IC sits on the FCA232Q/FCA232T's serial UART interface to translate the FCA232Q/FCA232T's TTL levels to RS232 levels. This level shifting can be done with the popular "213" series of TTL-to-RS232 converters, which typically contain 4 transmitters and 5 receivers in a 28-LD SSOP package and include an on-board voltage converter that turns the +5V (nominal) VCC into the +/-9 volts RS232 requires. A handy feature of these devices is the SHDN# pin, which can power the device down to a low quiescent current during USB suspend mode.

A suitable level-shifting device is the Sipex SP213EHCA, which supports RS232 communication at up to 500k baud. If a lower baud rate is acceptable, several pin-compatible alternatives exist, such as the Sipex SP213ECA, the Maxim MAX213CAI, and the Analogue Devices ADM213E, all rated for communication up to 115.2k baud. Where a higher rate is needed, the Maxim MAX3245CAI can handle RS232 up to 1Mbaud. Note that the MAX3245 is not pin-compatible with the 213 series, and its SHDN pin is active high, so it should be connected to PWREN# rather than SLEEP#.

In the example shown, CBUS0 and CBUS1 are configured as TXLED# and RXLED# and are used to drive two LEDs.

7.2 USB to RS485 Converter

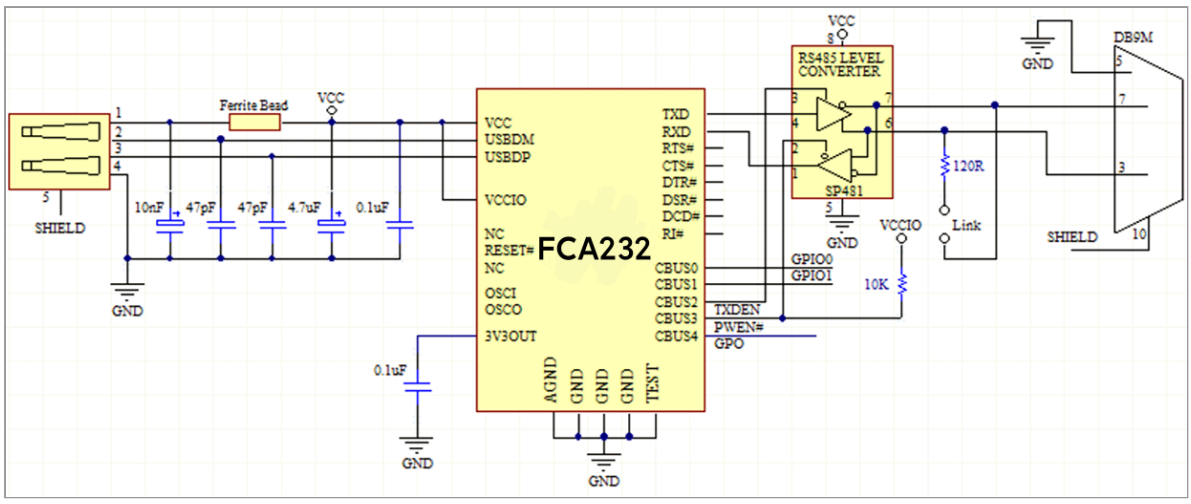


Figure 7.2 – Application Example Showing USB to RS485 Converter

Figure 7.2 shows an example of using the FCA232Q/FCA232T as a USB-to-RS485 converter. Here, a TTL-to-RS485 level converter IC on the FCA232Q/FCA232T's serial UART interface translates the FCA232Q/FCA232T's TTL levels to RS485 levels.

This example uses the Sipex SP481, with equivalent devices available from Maxim and Analogue Devices. The SP481 is an RS485 device in a compact 8-pin SOP package and has separate enables for its transmitter and receiver. In RS485, the transmitter is enabled only while a character is being sent from the UART; the TXDEN CBUS option on the FCA232Q/FCA232T exists precisely for this purpose, so the transmitter enable is wired to CBUS2 configured as TXDEN. Likewise, CBUS3 is configured as PWREN# and controls the SP481's receiver enable. Since the receiver enable is active low, it is tied to PWREN# to disable the receiver during USB suspend mode.

CBUS2 = TXDEN and CBUS3 = PWREN# are the factory-default configurations for these FCA232Q/FCA232T pins.

RS485 is a multi-drop network in which many devices can communicate over a two-wire cable. The cable must be terminated at each end, and a link providing the 120Ω termination allows this when the SP481 is physically located at either end of the cable.

In this example, data transmitted by the FCA232Q/FCA232T also appears on the SP481's receive path. This is a normal characteristic of RS485 and normally requires application software to strip the transmitted data from the received stream. With the FCA232Q/FCA232T, however, this can be done entirely in hardware by modifying Figure 7.2: logically OR the FCA232Q/FCA232T's TXDEN with the SP481 receiver output and connect the OR gate output to the FCA232Q/FCA232T's RXD.

Note that TXDEN is asserted one bit period before the start bit and de-asserted at the same time as the stop bit; this behaviour is not configurable.

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7.3 USB to RS422 Converter

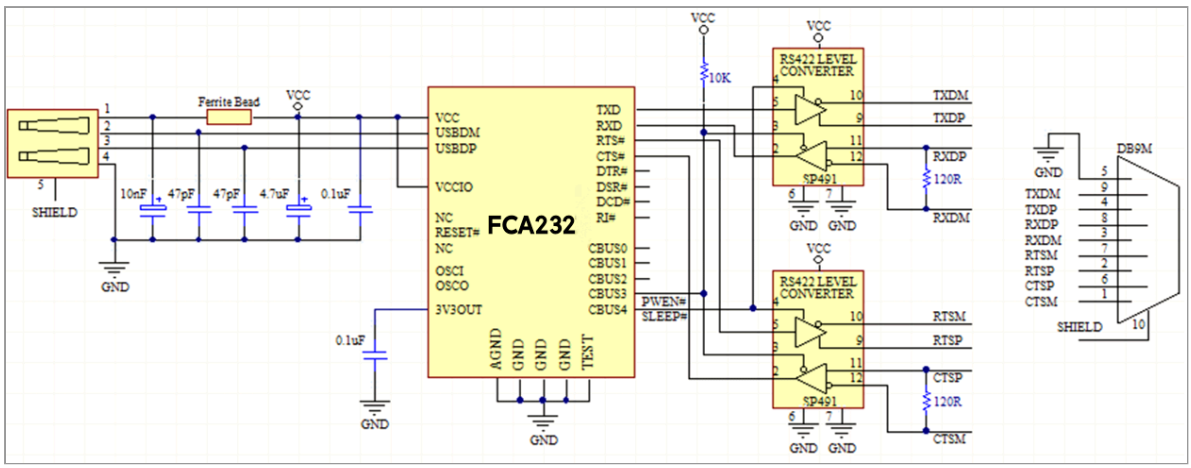


Figure 7.3 – USB to RS422 Converter Configuration

Figure 7.3 shows an example of using the FCA232Q/FCA232T as a USB-to-RS422 converter. Here, two TTL-to-RS422 level converters on the FCA232Q/FCA232T's serial UART interface translate the FCA232Q/FCA232T's TTL levels to RS422 levels. Many suitable converters are available; this example uses Sipex SP491 devices, which have enables on both transmitter and receiver. Because the SP491 transmitter enable is active high, it connects to a CBUS pin configured as SLEEP#, while the active-low receiver enable connects to a CBUS pin configured as PWREN#. This keeps the SP491 active whenever its transmitters and receivers are enabled, and disables them when the device enters USB suspend mode. For a similar USB bus-powered design, a P-channel logic-level MOSFET (controlled by PWREN#) may be needed in the VCC line of the SP491 devices to meet the 2.5mA USB standby current limit.

The SP491 is rated for data rates up to 5 Mbaud, but in this example the FCA232Q/FCA232T limits the maximum rate to 3 Mbaud.

7.4 USB to MCU UART Interface

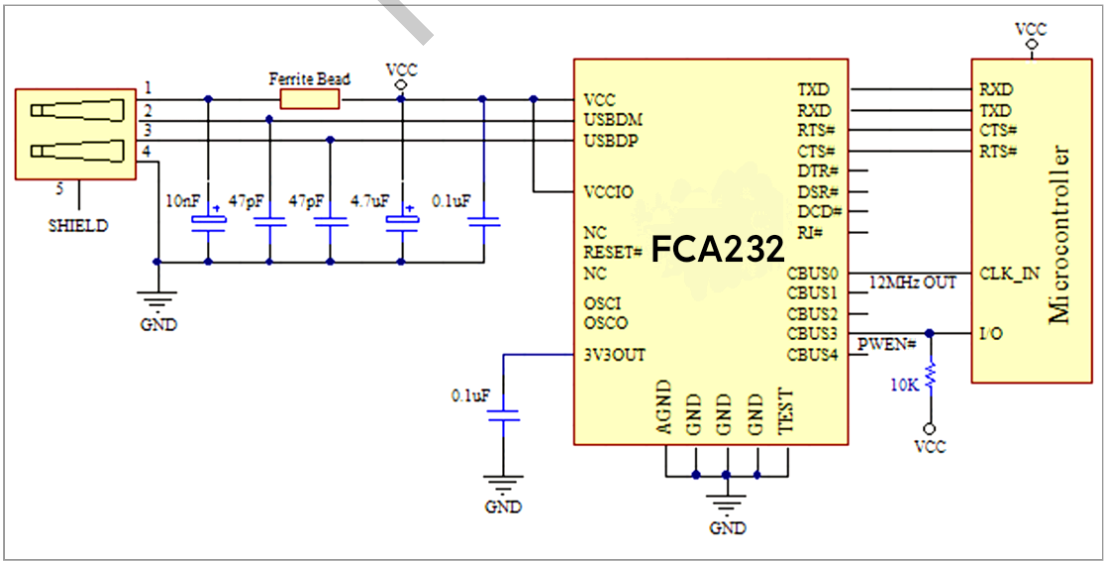


Figure 7.4 – USB to MCU UART Interface

Figure 7.4 shows an example of using the FCA232Q/FCA232T as a USB-to-microcontroller (MCU) UART interface. Here the FCA232Q/FCA232T uses TXD and RXD for data transmission and reception, and RTS#/CTS#

for hardware handshaking. In this example CBUS0 is configured as a 12MHz output to clock the MCU (the clock stops during suspend mode).

Optionally, RI# can be connected to another I/O pin on the MCU to wake the USB host controller from suspend. If the MCU handles power management, a CBUS pin can be configured as PWREN# and connected to an MCU I/O pin as well.

7.5 LED Interface

Any CBUS I/O pin can be configured to drive an LED. The FCA232Q/FCA232T provides three CBUS options for driving LEDs: TXLED#, RXLED#, and TX&RXLED#. See Section 3.3 for the configuration options.

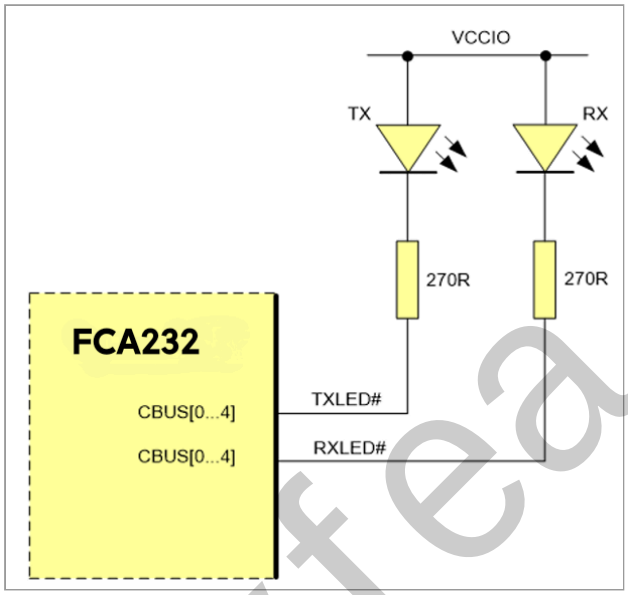


Figure 7.5 – Dual LED Configuration

Figure 7.5 shows an example of using the FCA232Q/FCA232T to drive LEDs. In this application one CBUS pin signals data transmission (TXLED#) and another signals data reception (RXLED#). While data is being sent or received, the corresponding pin drives from tristate to low to light the LED. A digital one-shot ensures that even brief bursts of data transfer remain visible to the user.

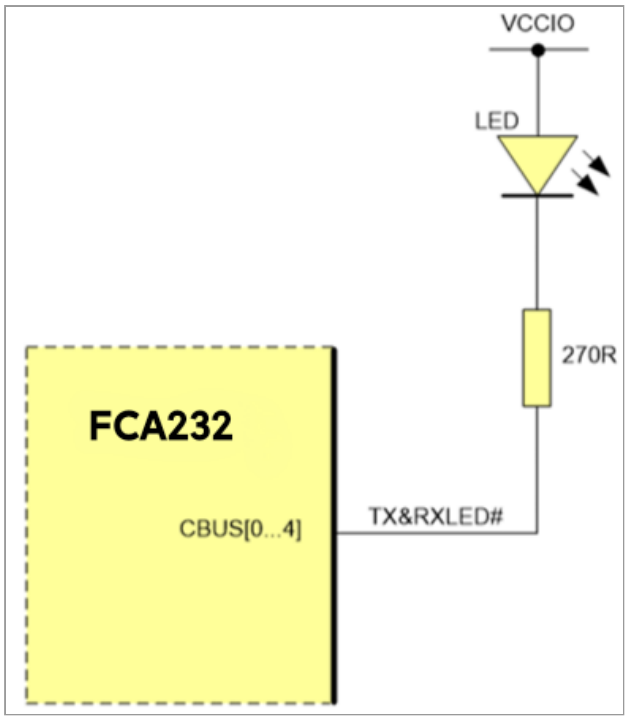


Figure 7.6 – Single LED Configuration

7.6 Using the External Oscillator

By default, the FCA232Q/FCA232T is configured to use its internal oscillator, which operates normally over a VCC range from 5.25V down to 3.3V. Alternatively, the device can be configured to use an external oscillator over the same VCC range. The external oscillator may be either a crystal or a clock source; if an external clock source is used instead of an external crystal or the internal oscillator, the external clock input level must be adjusted to stay below 1.98V. Please refer to TN_183.

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8 Internal EEPROM Configuration

This section describes how the internal EEPROM is configured on the FCA232Q/FCA232T.

Table 8.1 – Default Internal EEPROM Configuration

Parameter	Value	Notes
USB Vendor ID (VID)	0403h	NYFEA default VID (hex)
USB Product ID (PID)	6001h	NYFEA default PID (hex)
Serial Number Enabled?	Yes	—
Serial Number	See Note	A unique serial number is generated and programmed into the EEPROM during device final test.
Pull down I/O Pins in USB Suspend	Disabled	Enabling this option will make the device pull down on the UART interface lines when in USB suspend mode (PWREN# is high).
Manufacturer Name	NYFEA	—
Product Description	FCA232Q USB UART / FCA232T USB UART	Product description string for the QFN-32 and SSOP-28 variants respectively.
Max Bus Power Current	90mA	—
Power Source	Bus Powered	—
Device Type	FCA232Q / FCA232T	Device type string for the QFN-32 and SSOP-28 variants respectively.
USB Version	0200	Returns USB 2.0 device description to the host. Note: The device is a USB 2.0 Full Speed device (12Mb/s) as opposed to a USB 2.0 High Speed device (480Mb/s).
Remote Wake Up	Enabled	Taking RI# low will wake up the USB host controller from suspend in approximately 20 ms.
High Current I/Os	Disabled	Enables the high drive level on the UART and CBUS I/O pins.
Load VCP Driver	Enabled	Makes the device load the VCP driver interface for the device.
CBUS0	TXLED#	Default configuration of CBUS0 – Transmit LED drive.
CBUS1	RXLED#	Default configuration of CBUS1 – Receive LED drive.
CBUS2	TXDEN	Default configuration of CBUS2 – Transmit data enable for RS485.
CBUS3	PWREN#	Default configuration of CBUS3 – Power enable. Low after USB enumeration, high during USB suspend mode.
CBUS4	SLEEP#	Default configuration of CBUS4 – Low during USB suspend mode.
Invert TXD	Disabled	Signal on this pin becomes TXD# if enable.

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Parameter	Value	Notes
Invert RXD	Disabled	Signal on this pin becomes RXD# if enable.
Invert RTS#	Disabled	Signal on this pin becomes RTS if enable.
Invert CTS#	Disabled	Signal on this pin becomes CTS if enable.
Invert DTR#	Disabled	Signal on this pin becomes DTR if enable.
Invert DSR#	Disabled	Signal on this pin becomes DSR if enable.
Invert DCD#	Disabled	Signal on this pin becomes DCD if enable.
Invert RI#	Disabled	Signal on this pin becomes RI if enable.

The FCA232Q/FCA232T's internal EEPROM can be programmed over USB using NYFEA's FT_PROG utility, which can be downloaded from NYFEA Utilities on the NYFEA website. Version 2.8a or later is required for the FCA232Q/FCA232T. Users without their own USB Vendor ID who would like a unique Product ID for their design can apply to NYFEA for a free block of unique PIDs; contact NYFEA support for this service.

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9 Package Parameters

The FCA232Q is supplied in a QFN-32 package and the FCA232T in a 28-LD SSOP package. Package dimensions and soldering information for both variants are provided below.

9.1 QFN-32 Package Dimensions

The FCA232Q is supplied in a 5 mm × 5 mm, 32-pin QFN package with a 0.5 mm pin pitch. Figure 9.1 shows the package dimensions.

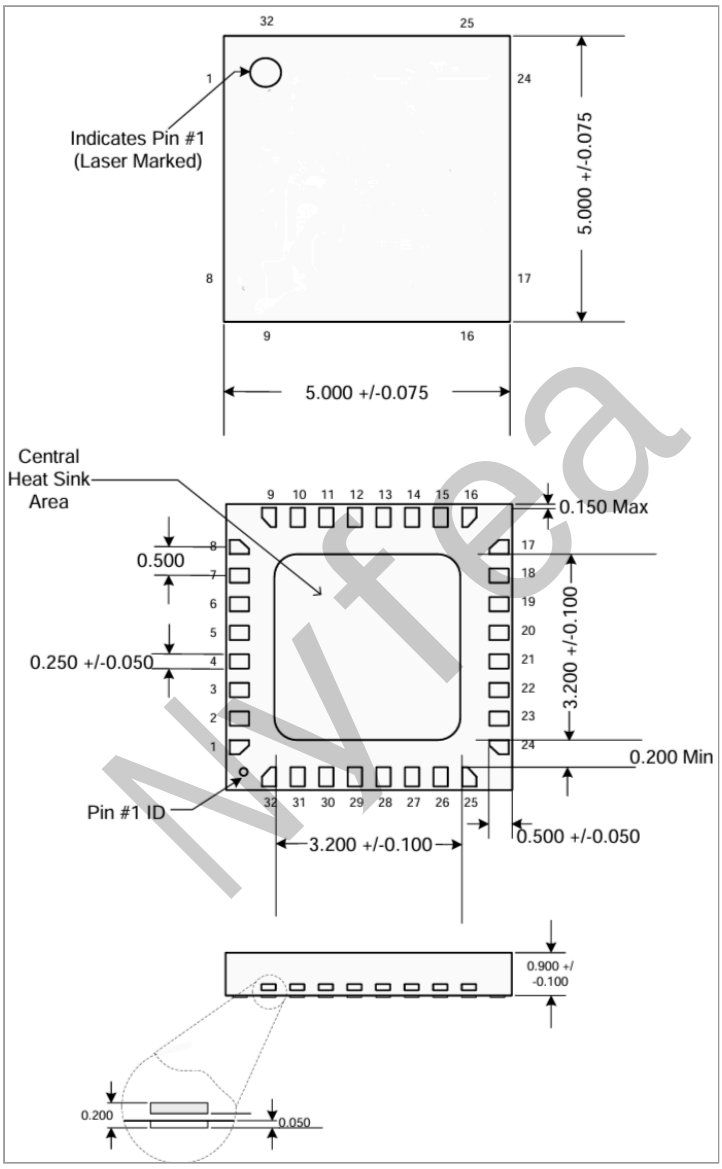


Figure 9.1 – QFN-32 Package Dimensions

9.2 QFN-32 Package Typical Pad Layout

Figure 9.2 shows the recommended PCB pad layout for the QFN-32 package.

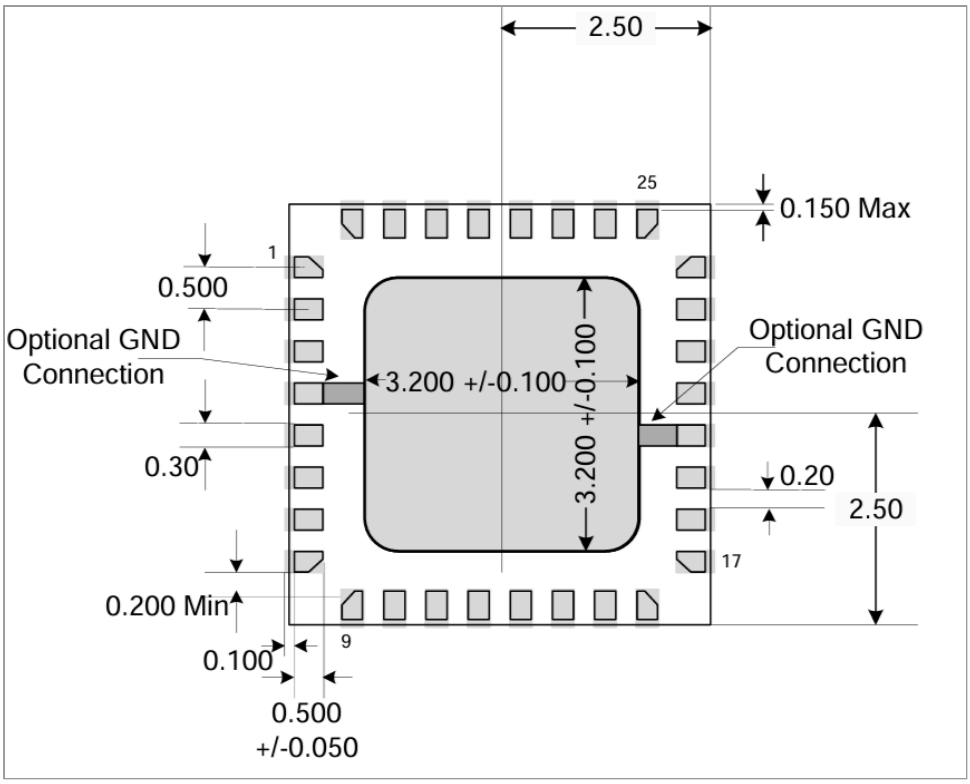


Figure 9.2 – Typical Pad Layout for QFN-32 Package

9.3 QFN-32 Package Typical Solder Paste Diagram

Figure 9.3 shows the recommended solder paste stencil aperture pattern for the QFN-32 package.

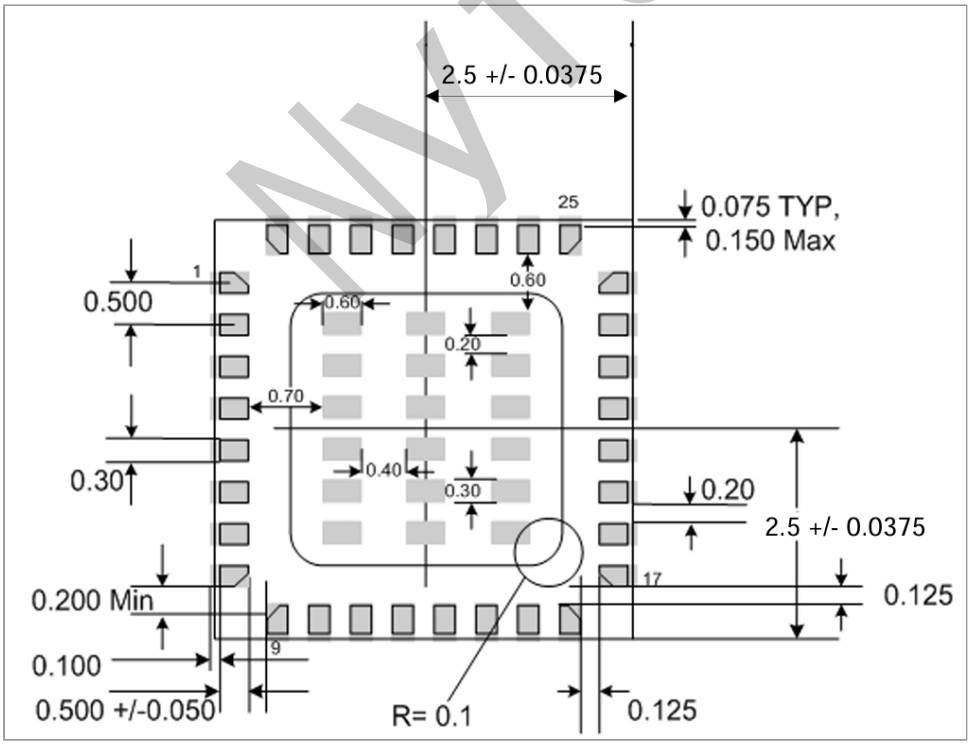
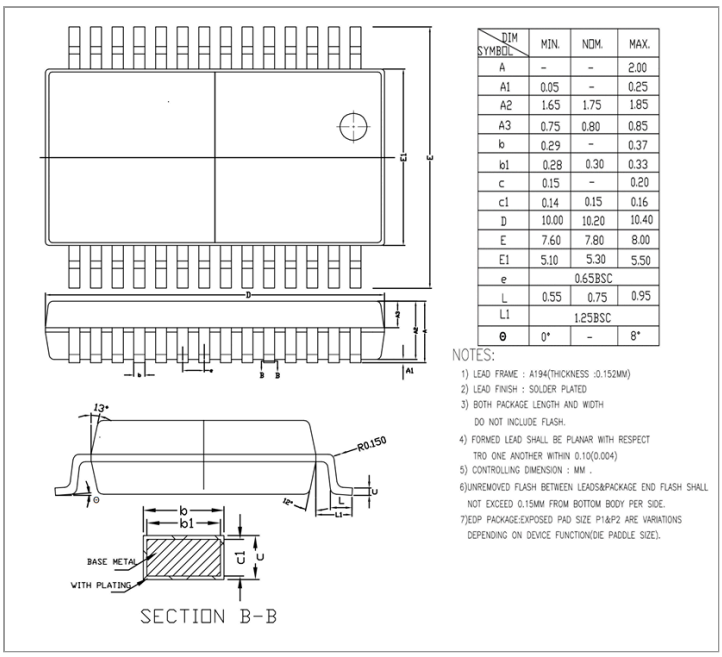


Figure 9.3 – Typical Solder Paste Diagram for QFN-32 Package

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9.4 SSOP-28 Package Dimensions



DIM SYMBOL	MIN.	NOM.	MAX.
A	–	–	2.00
A1	0.05	–	0.25
A2	1.65	1.75	1.85
A3	0.75	0.80	0.85
b	0.29	–	0.37
b1	0.28	0.30	0.33
c	0.15	–	0.20
c1	0.14	0.15	0.16
D	10.00	10.20	10.40
E	7.60	7.80	8.00
E1	5.10	5.30	5.50
e	0.65BSC		
L	0.55	0.75	0.95
L1	1.25BSC		
θ	0°	–	8°

Figure 9.4 – SSOP-28 Package Dimensions

The FCA232T is supplied in a RoHS-compliant 28-pin SSOP package that is lead (Pb) free and uses a 'green' mould compound. The package is fully compliant with European Union directive 2002/95/EC. It has a nominal 5.30mm x 10.20mm body (7.80mm x 10.20mm including pins) with pins on a 0.65mm pitch. The mechanical drawing above shows the SSOP-28 package; all dimensions are in millimetres.

The date code format is YYWW-B, where WW is the 2-digit week number, YY is the 2-digit year, and B is a single letter denoting the device revision (e.g., A, B, or C). The XXXXXXXXXXXX code is the manufacturing lot code. This applies only to devices manufactured after April 2009.

9.5 Solder Reflow Profile

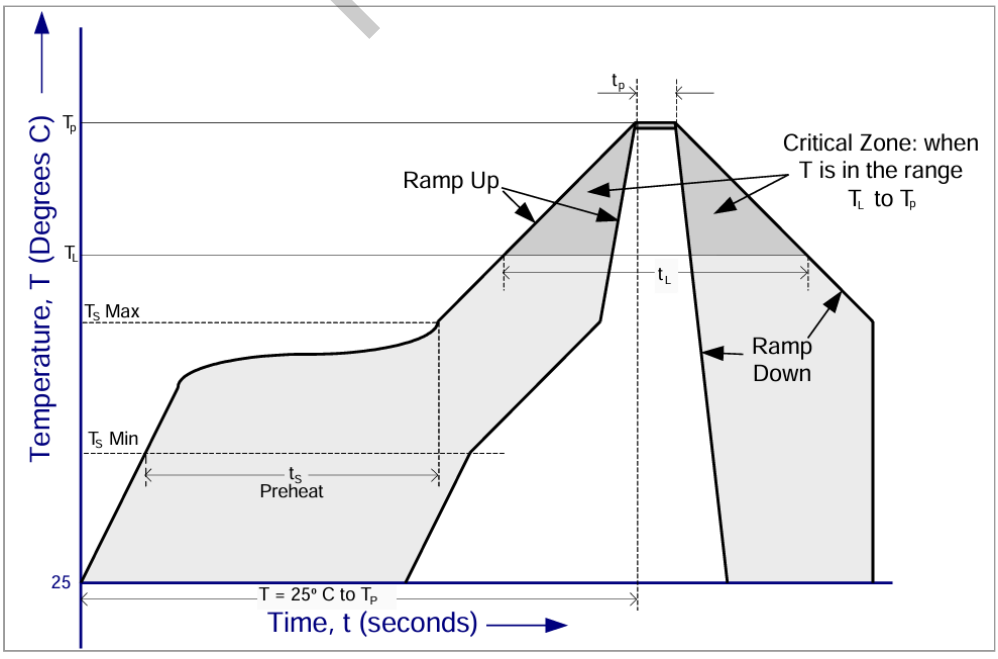


Figure 9.5 – Solder Reflow Profile

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The FCA232Q/FCA232T is supplied in Pb-free QFN-32 and 28-LD SSOP packages. The recommended solder reflow profile is shown in Figure 9.5.

The recommended reflow profile values are listed in Table 9.1. Values are given for both a fully Pb-free solder process (the FCA232Q/FCA232T used with Pb-free solder) and a non-Pb-free process (the FCA232Q/FCA232T used with non-Pb-free solder).

Table 9.1 – Reflow Profile Parameter Values

Profile Feature	Pb Free Solder Process	Non-Pb Free Solder Process
Average Ramp Up Rate (Ts to Tp)	3°C / second Max.	3°C / Second Max.
Preheat - Temperature Min (Ts Min.)	150°C	100°C
Preheat - Temperature Max (Ts Max.)	200°C	150°C
Preheat - Time (ts Min to ts Max)	60 to 120 seconds	60 to 120 seconds
Time Maintained Above Critical Temperature TL: - Temperature (TL)	217°C	183°C
Time Maintained Above Critical Temperature TL: - Time (tL)	60 to 150 seconds	60 to 150 seconds
Peak Temperature (Tp)	260°C	240°C
Time within 5°C of actual Peak Temperature (tp)	20 to 40 seconds	20 to 40 seconds
Ramp Down Rate	6°C / second Max.	6°C / second Max.
Time for T = 25°C to Peak Temperature, Tp	8 minutes Max.	6 minutes Max.

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10 Alternative Parts

The NYFEA range offers several alternatives for different interface and package requirements. Table 10.1 summarises the key alternatives to the FCA232Q/FCA232T.

Table 10.1 – Alternative NYFEA USB UART / FIFO Devices

Part	Interface	Package	Key Difference
FCA232Q	UART	QFN-32	Equivalent single-channel USB UART in QFN-32
FCA232T	UART	SSOP-28	Single-channel USB UART in SSOP-28

For new designs, refer to the latest NYFEA product selector and datasheets for device availability, package options and recommended replacements.

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