1.General Description

The EM74LVC4245 is an octal dual supply translating transceiver featuring 3-state bus compatible outputs in both send and receive directions. It is designed to interface between a 3 V and 5 V bus in a mixed 3 V and 5 V supply environment. The device features an output enable input ($\overline{OE}$) and a send/receive input (DIR) for direction control. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state, effectively isolating the buses. In suspend mode, when either supply is zero, there is no current path between supplies. $V_{CCA} \geq V_{CCB}$, except in suspend mode. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

2.Features and Benefits

- 5 V tolerant inputs/outputs, for interfacing with 5 V logic
- Wide supply voltage range
  - 5 V bus ($V_{CC(A)}$): 1.5 V to 5.5 V
  - 3 V bus ($V_{CC(B)}$): 1.5 V to 3.6 V
- CMOS low-power consumption
- TTL interface capability at 3.3 V
- Latch-up performance exceeds 250 mA
- Overvoltage tolerant control inputs to 5.5 V
- High-impedance when $V_{CC(A)}$ or $V_{CC(B)}$ = 0 V
- Complies with JEDEC standard no. JESD8B/JESD36
- I_{OFF} circuitry provides partial Power-down mode operation
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2500 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options

3.Ordering Information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Quantity
EM74LVC4245PW	LVC4245☐ XYYWW	TSSOP-24L	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	3000

MARKING INFORMATION

NOTE: LVC4245☐ = Serial number and Internal code; XYYWW = Vendor Code and Date Code.

4.Function Diagram

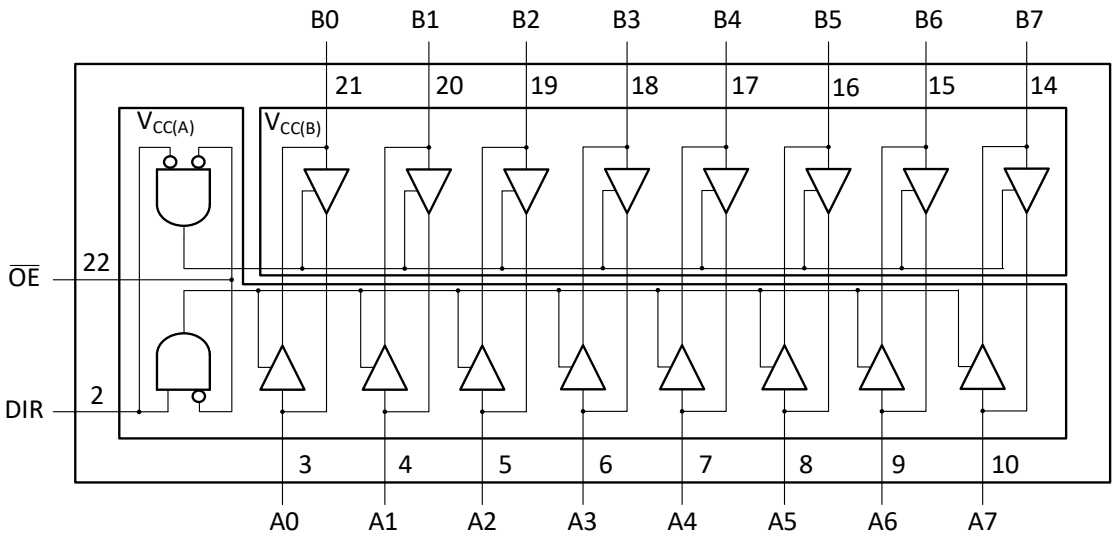


Fig. 1. Logic symbol

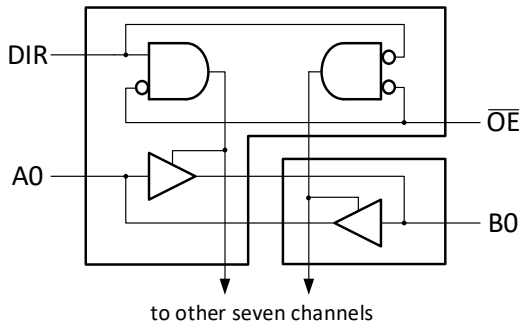


Fig. 2. Logic diagram (one channel)

5.Pinning Information

5.1. Pinning

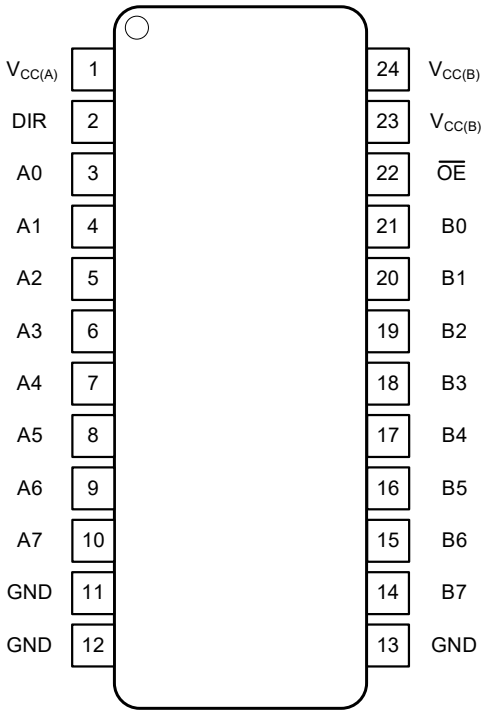


Fig. 3. Top view pin configuration TSSOP

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{CC(A)}$	1	Supply voltage A (An inputs/outputs, $\overline{OE}$ and DIR inputs are referenced to $V_{CC(A)}$)
DIR	2	Direction control
A0, A1, A2, A3, A4, A5, A6, A7	3, 4, 5, 6, 7, 8, 9, 10	Data input or output
GND [1]	11, 12, 13	Ground (0 V)
B0, B1, B2, B3, B4, B5, B6, B7	21, 20, 19, 18, 17, 16, 15, 14	Data input or output
$\overline{OE}$	22	Output enable input (active LOW)
$V_{CC(B)}$	23, 24	Supply voltage B (Bn inputs/outputs are referenced to $V_{CC(B)}$)

[1] All GND pins must be connected to ground (0V).

6.Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Input/output	
$\overline{OE}$	DIR	An	Bn
L	L	A = B	input
L	H	input	B = A
H	X	Z	Z

7.Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 4. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	6.5	V
$V_{CC(B)}$	supply voltage B		-0.5	6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50		mA
V_I	input voltage	[1]	-0.5	6.5	V
I_{OK}	output clamping current	$V_O < 0$ V	-50		mA
V_O	output voltage	Active mode [1][2][3]	-0.5	V_{CCO} + 0.5	V
		Suspend or 3-state mode [1]	-0.5	6.5	V
I_O	output current	V_O = 0 V to V_{CCO} [2]		±50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$; per V_{CC} pin		100	mA
I_{GND}	ground current	per GND pin	-100		mA
P_{tot}	total power dissipation			500	mW
T_{stg}	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] V_{CCO} + 0.5 V should not exceed 6.5 V.

8. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.5	5.5	V
$V_{CC(B)}$	supply voltage B		1.5	3.6	V
V_I	input voltage	for control inputs	0	5.5	V
V_O	output voltage	Active mode	0	V_{CCO}	V
		Suspend or 3-state mode	0	5.5	V
T_{amb}	ambient temperature		-40	125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC(B)}$ = 2.7 V to 3.0 V		20	ns/V
		$V_{CC(B)}$ = 3.0 V to 3.6 V		10	ns/V
		$V_{CC(A)}$ = 3.0 V to 4.5 V		10	ns/V
		$V_{CC(A)}$ = 4.5 V to 5.5 V		5	ns/V

9.Static Characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V). Typical values measured at T_{amb} = 25°C (unless otherwise noted).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC(B)}$ = 2.7 V to 3.6 V	2.0			2.0		V
		$V_{CC(A)}$ = 4.5 V to 5.5 V	2.0			2.0		V
V_{IL}	LOW-level input voltage	$V_{CC(B)}$ = 2.7 V to 3.0 V			0.5		0.5	V
		$V_{CC(B)}$ = 3.3 V to 3.6 V			0.7		0.7	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V			0.8		0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH}						
		I_O = -100 µA; $V_{CC(B)}$ = 2.7 V to 3.6 V	$V_{CC(B)}$ - 0.1			$V_{CC(B)}$ - 0.1		V
		I_O = -12 mA; $V_{CC(B)}$ = 2.7 V	2.2			2.1		V
		I_O = -20 mA; $V_{CC(B)}$ = 3.0 V	2.4			2.3		V
		I_O = -100 µA; $V_{CC(A)}$ = 4.5 V to 5.5 V	$V_{CC(A)}$ - 0.1			$V_{CC(A)}$ - 0.1		V
		I_O = -32 mA; V_{CC} = 4.5 V	3.8			3.7		V
V_{OL}	LOW-level output voltage	V_I = V_{IL}						
		I_O = 100 µA; $V_{CC(B)}$ = 2.7 V to 3.6 V			0.1		0.1	V
		I_O = 12 mA; $V_{CC(B)}$ = 2.7 V			0.4		0.6	V
		I_O = 20 mA; $V_{CC(B)}$ = 3.0 V			0.55		0.55	V
		I_O = 100 µA; $V_{CC(A)}$ = 4.5 V to 5.5 V			0.1		0.1	V
		I_O = 32 mA; $V_{CC(A)}$ = 4.5 V			0.55		0.6	V
I_I	input leakage current	V_I = 5.5 V or GND			±2		±10	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL} [1]						
		$V_{CC(B)}$ = 3.6 V; V_O = $V_{CC(B)}$ or GND			±2		±10	µA
		$V_{CC(A)}$ = 5.5 V; V_O = $V_{CC(A)}$ or GND			±2		±10	µA

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
I_{CC}	supply current	I_O = 0 A						
		$V_{CC(B)}$ = 3.6 V; other inputs at $V_{CC(B)}$ or GND			10		20	µA
		$V_{CC(A)}$ = 5.5 V; other inputs at $V_{CC(A)}$ or GND			10		20	µA
ΔI_{CC}	additional supply current	per input; I_O = 0 A						
		$V_{CC(B)}$ = 2.7 V to 3.6 V; V_I = $V_{CC(B)}$ - 0.6 V; other inputs at $V_{CC(B)}$ or GND			50		75	µA
		$V_{CC(A)}$ = 4.5 V to 5.5 V; V_I = $V_{CC(A)}$ - 0.6 V; other inputs at $V_{CC(A)}$ or GND			50		75	µA

[1] For transceivers, the parameter IOZ includes the input leakage current.

10. Dynamic Characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $V_{CC(A)}$ = 4.5 V to 5.5 V;$V_{CC(B)}$ = 2.7 V to 3.6 V; $t_r = t_f \leq 2.5$ ns. For test circuit see Fig. 6.

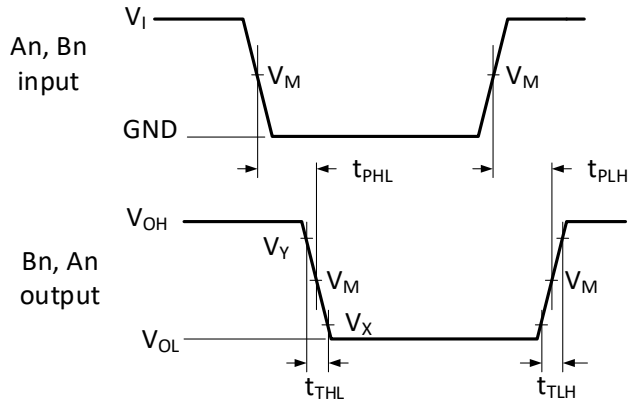
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
t_{PHL}	HIGH to LOW propagation delay	An to Bn; see Fig. 4	1.0	3.3	6.3	1.0	8.0	ns
		Bn to An; see Fig. 4	1.0	3.3	6.3	1.0	8.0	ns
t_{PLH}	LOW to HIGH propagation delay	An to Bn; see Fig. 4	1.0	3.3	6.7	1.0	8.5	ns
		Bn to An; see Fig. 4	1.0	3.0	5.0	1.0	6.5	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{OE}$ to An; see Fig. 5	1.0	4.5	9.0	1.0	11.5	ns
		$\overline{OE}$ to Bn; see Fig. 5	1.0	4.4	8.7	1.0	11.0	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{OE}$ to An; see Fig. 5	1.0	4.5	8.1	1.0	10.5	ns
		$\overline{OE}$ to Bn; see Fig. 5	1.0	4.3	8.7	1.0	11.0	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{OE}$ to An; see Fig. 5	1.0	2.9	7.0	1.0	9.0	ns
		$\overline{OE}$ to Bn; see Fig. 5	1.0	3.9	7.7	1.0	10.0	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{OE}$ to An; see Fig. 5	1.0	2.8	5.8	1.0	7.5	ns
		$\overline{OE}$ to Bn; see Fig. 5	1.0	3.3	7.8	1.0	10.0	ns
$t_{sk(o)}$	output skew time				1.0		1.5	ns
C_{PD}	power dissipation capacitance	5 V bus: Bn to An; V_I = GND to $V_{CC(A)}$; $V_{CC(A)}$ = 5.0 V						
		outputs enabled		17				pF
		outputs disabled		5				pF
		3 V bus: An to Bn; V_I = GND to $V_{CC(B)}$; $V_{CC(B)}$ = 3.3 V						
		outputs enabled		17				pF
		outputs disabled		5				pF

[1] Typical values are measured at Tamb = 25 °C, $V_{CC(A)}$ = 5.0 V, and $V_{CC(B)}$ = 3.3 V respectively.

[2] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW). $P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}{}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz;
C_L = output load capacitance in pF; V_{CC} = supply voltage in Volts;
N = number of inputs switching; $\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = sum of the outputs

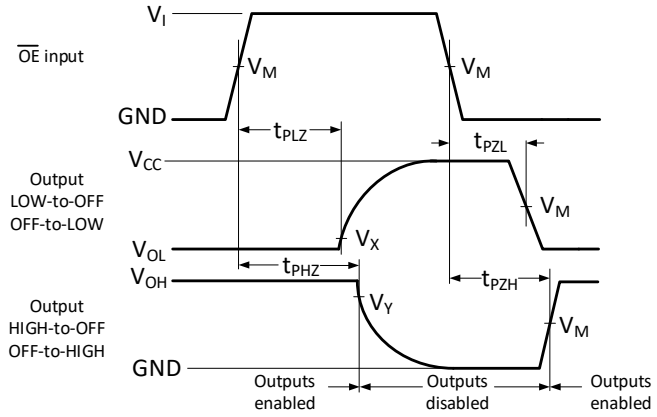
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. The input An, Bn to output Bn, An propagation delays



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

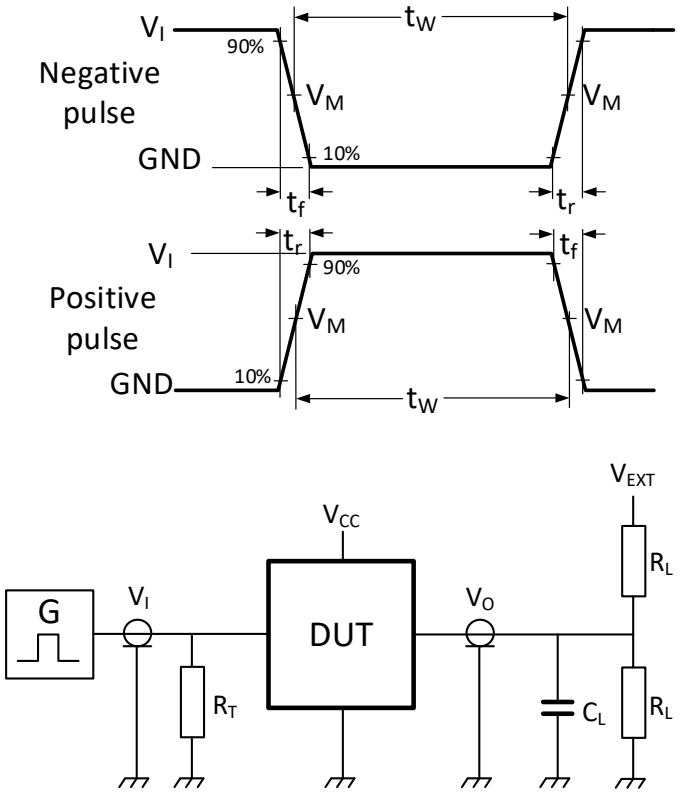
Fig. 5. 3-state enable and disable times

Table 8. Measurement points

Supply voltage		Input		Output		
$V_{CC(A)}$	$V_{CC(B)}$	V_M [1]	V_I [1]	V_M [2]	V_X	V_Y
≤ 2.7 V	≤ 2.7 V	0.5 V_{CCI}	V_{CCI}	0.5 V_{CCO}	V_{OL} + 0.1 V	V_{OH} - 0.1 V
-	2.7 V to 3.6 V	1.5 V	2.7 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
≥ 4.5 V	-	0.5 V_{CCI}	3.0 V	0.5 V_{CCO}	V_{OL} + 0.3 V	V_{OH} - 0.3 V

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.



Test data is given in Table 9.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
V_{EXT} = External voltage for measuring switching times.

Fig. 6. Test circuit for measuring switching times

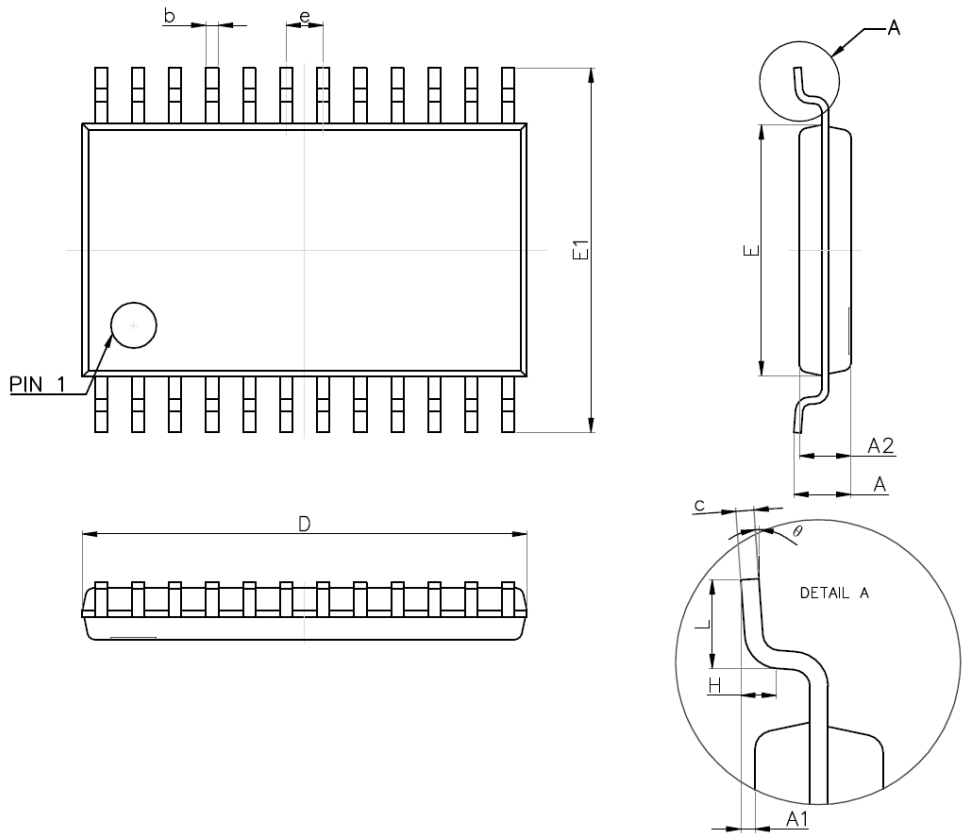
Table 9. Test data

Supply voltage		Input	Load		V_{EXT}		
$V_{CC(A)}$	$V_{CC(B)}$	V_I [1]	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ} [2]
< 2.7 V	< 2.7 V	V_{CCI}	50 pF	500 Ω	open	GND	$2V_{CCO}$
	2.7 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	$2V_{CCO}$
4.5 V to 5.5 V		3.0 V	50 pF	500 Ω	open	GND	$2V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the data input port.
[2] V_{CCO} is the supply voltage associated with the output port.

11. Package Outline

TSSOP-24L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	7.700	7.900	0.303	0.311
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.650(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.250(TYP)		0.010(TYP)	
θ	1°	7°	1°	7°

12. Tape and Reel Information

12.1. Carrier tape dimensions

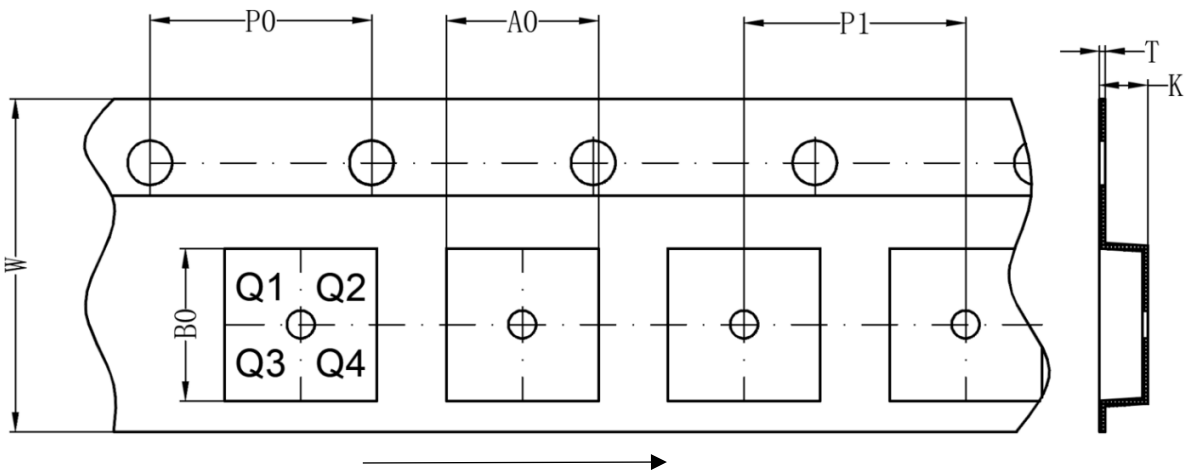


Table 10. Carrier tape dimensions

Package version	A0(mm)	B0(mm)	K0(mm)	T(mm)	P1(mm)	W(mm)	P0(mm)	PIN 1
TSSOP-24L	6.8	8.6	1.9	0.3	8	16	4	Q1

12.2. Reel and box dimensions

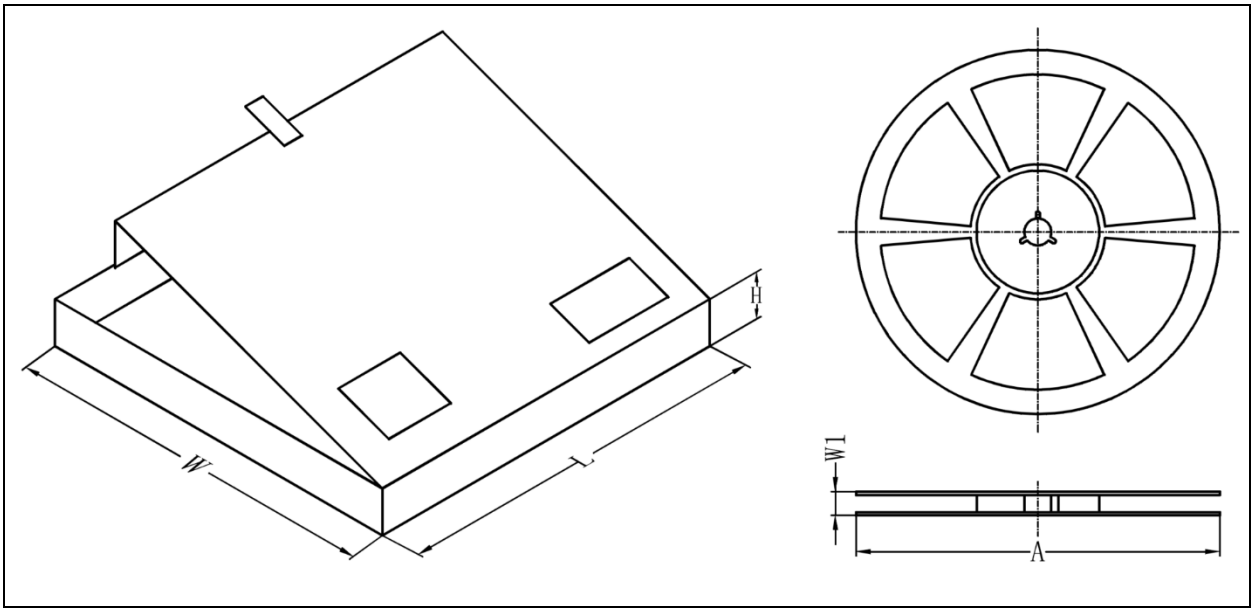


Table 11. Dimensions and quantities

Package version	Type NO. ending	Reel Dimension A (mm)	Reel Width W1 (mm)	SPQ (pcs) [1]	Reels per box	Outer box dimensions L×W×H(mm) [2]
TSSOP-24L	PW	330	22.4	3000	1	358x340x50

[1] Packing quantity dependent on specific product type. Please contact your local Energymath representative for ordering.

[2] Dimensions for reference only.

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model

14. Revision History

Table 13. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
EM74LVC4245 Rev. 1.3	Aug 15, 2025	Product datasheet		EM74LVC4245 Rev. 1.2
Modifications:	• Table 1 : ordering information updated. • Section 12: Added tape and reel information.			
EM74LVC4245 Rev. 1.2	Apr 20, 2025	Product datasheet		EM74LVC4245 Rev. 1.1
Modifications:	• Section 11: Updated the package outline.			
EM74LVC4245 Rev. 1.1	Apr 13, 2025	Product datasheet		EM74LVC4245 Rev. 1.0
Modifications:	• Updated the V_{OH} and V_{OL} spec. • Added the topside marking information.			
EM74LVC4245 Rev. 1.0	Feb 10, 2025	Product datasheet		