XHSC 小华半导体 XIAOHUA SEMICONDUCTOR

HC32F460 Series

32-bit ARM® Cortex®-M4 Microcontroller

Datasheet

Rev1.61 February 2026

Features

ARM Cortex-M4 32bit MCU+FPU, 250DMIPS, up to 512 KB Flash, 192 KB SRAM, USB FS (Device/Host), 14 Timers, 2 ADCs, 1 PGA, 3 CMPs, 20 communication ports

- **ARMv7-M architecture 32bit Cortex-M4 CPU, integrated FPU, MPU, DSP supporting SIMD instructions, and CoreSight standard debugging unit. The highest operating frequency is 200 MHz, and the Flash acceleration unit realizes 0-wait program execution, reaching the computing performance of 250DMIPS or 680Coremarks**
- **Built-in memory**
  - Up to 512KByte of Flash memory, supporting security protection and data encryption*1
  - Maximum 192KByte SRAM, including 32KByte 200 MHz single-cycle access high-speed RAM, 4KByte Retention RAM
- **Power, Clock, Reset Management**
  - System power supply (Vcc): 1.8-3.6 V
  - 6 independent clock sources: external high-speed oscillator (4-25 MHz), external low-speed oscillator (32.768 kHz), internal high-speed RC (16/20 MHz), internal medium-speed RC (8MHz), internal low-speed RC (32.768 kHz), internal WDT Dedicated RC (10 kHz)
  - 14 kinds of reset sources including POR, LVDR and PDR, each of which has an independent flag bit.
- **Low power operation**
  - Peripherals can be turned off or on independently
  - Three low power consumption modes: Sleep, Stop, Power down mode
  - Support switching between super high-speed mode, high speed mode and super low speed mode in Run mode and Sleep mode
  - Standby power consumption: typ.90uA@25°C in Stop mode, as low as 1.8μA@25°C in Power down mode
  - In Power down mode, support 16 ports to wake up, support ultra-low power RTC work, 4KByte SRAM to keep data
  - Fast wake-up in standby mode, the fastest wake-up in Stop mode is 2 μs, and the fastest wake-up in Power down mode is 20 μs
- **Peripheral operation support system significantly reduces CPU processing load**
  - 8-channel dual-host DMAC
  - DMAC for USBFS
  - Data Computing Unit (CRC)
  - Support mutual triggering of peripheral events (AOS)
- **High Performance Simulation**
  - 2 independent 12bit 2.5MSPS ADCs
  - 1 programmable gain amplifier (PGA)
  - 3 independent voltage comparators (CMP), supporting 2 internal reference voltages
  - 1 on-chip temperature sensor (OTS)
- **Timer**
  - 3 multifunctional 16bit PWM Timers (Timer6)
  - 3 16-bit motor PWM Timers (Timer4)
  - 6 16bit general-purpose Timers (TimerA)
  - 2 16bit basic Timer (Timer0)
- **Up to 83 GPIOs**
  - CPU single-cycle access, maximum 100MHz output
  - Up to 81 5V-tolerant IOs
- **Maximum 20 communication interfaces**
  - 3 I2C, support SMBus protocol
  - 4 USART, support ISO7816-3 protocol
  - 4 SPIs
  - 4 I2S, built-in audio PLL supports audio level sampling accuracy
  - 2 SDIO, support SD/MMC/eMMC format
  - 1 QSPI, support 200Mbps high-speed access (XIP)
  - 1 CAN, support ISO11898-1 standard protocol
  - 1 USB 2.0 FS, built-in PHY, support Device/Host
- **Data encryption function**
  - AES/HASH/TRNG
- **Encapsulation form:**

  LQFP100 (14×14 mm) VFBGA100 (7×7 mm)
  LQFP64 (10×10 mm) QFN60 (7×7 mm)
  QFN48 (5×5 mm) LQFP48 (7×7 mm)

*1: For the specific specifications of Flash security protection and data encryption, please consult the sales window.

Support Model

HC32F460PETB-LQFP100	HC32F460PEHB-VFBGA100
HC32F460KETA-LQFP64	HC32F460KEUA-QFN60TR
HC32F460JETA-LQFP48	HC32F460JEUA-QFN48TR
HC32F460PCTB-LQFP100	HC32F460KCTA-LQFP64
HC32F460JCTA-LQFP48	-

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1 Overview

The HC32F460 product family is a high-performance MCU based on ARM® Cortex®-M4 32-bit RISC CPU with a maximum operating frequency of 200 MHz. The Cortex-M4 core integrates a floating-point arithmetic unit (FPU) and a DSP to implement single-precision floating-point arithmetic operations, supports all ARM single-precision data processing instructions and data types, and supports the complete DSP instruction set. The kernel integrates the MPU unit and superimposes the DMAC dedicated MPU unit at the same time to ensure the safety of system operation.

The HC32F460 series integrates high-speed on-chip memory, including a maximum of 512 KB of Flash and a maximum of 192KB of SRAM. Integrated Flash access acceleration unit to achieve single cycle program execution of the CPU on Flash. The polled bus matrix supports multiple bus hosts to access memory and peripherals simultaneously, improving performance. The bus master includes CPU, DMA, USB dedicated DMA, etc. In addition to the bus matrix, it supports data transfer between peripherals, basic arithmetic operations and mutual triggering of events, which can significantly reduce the transaction processing load of the CPU.

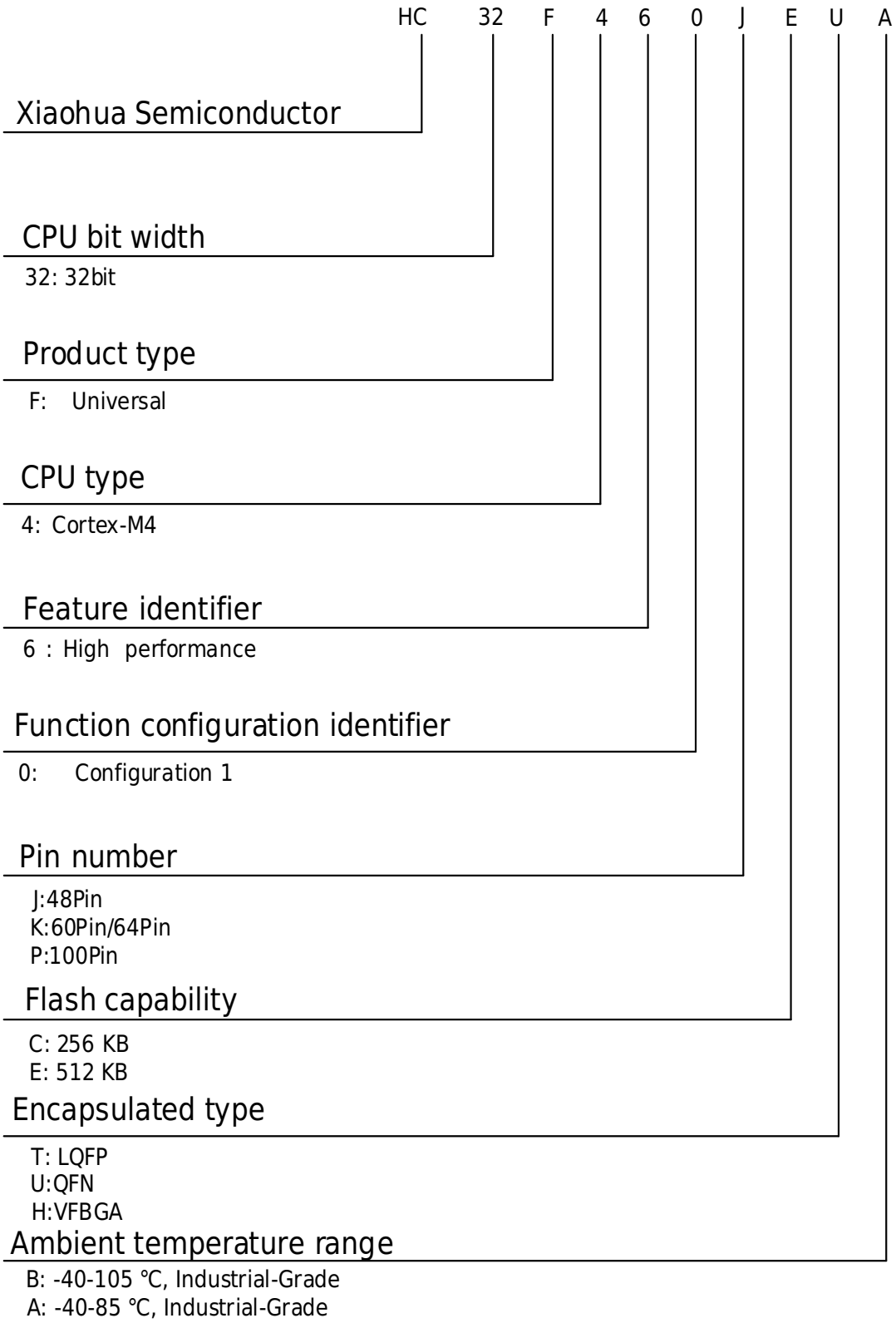
The HC32F460 series integrates rich peripheral functions. Including 2 independent 12bit 2.5MSPS ADCs, 1 adjustable gain PGA, 3 voltage comparators (CMP), 3 multifunctional 16bit PWM Timers (Timer6) supporting 6 complementary PWM outputs, 3 motor PWM Timers (Timer4) Support 18 complementary PWM outputs, 6 16bit general-purpose Timers (TimerA) support 3 3-phase quadrature encoding inputs and 48 Duty independent PWM outputs, 11 serial communication interfaces (I2C/UART/SPI), 1 QSPI interface, 1 channel CAN, 4 I2S supports audio PLLs, 2 SDIOs, 1 USB FS Controller with on-chip FS PHY supporting Device/Host.

The HC32F460 product family supports wide voltage range (1.8-3.6 V), wide temperature range (-40-105 °C) and low power mode. In Run mode and Sleep mode, you can switch between ultra-high-speed mode (≤200MHz), high-speed mode (≤168MHz) and ultra-low speed mode (≤8MHz). Supports fast wake-up in low power consumption mode, the fastest wake-up to STOP mode is 2μs, and the fastest wake-up to Power-down mode is 20μs.

Typical Application

The HC32F460 series provides 48pin, 64pin, 100pin LQFP packages, 48pin and 60pin QFN packages, 100pin VFBGA package, suitable for high-performance motor frequency conversion control, intelligent hardware, IoT connection modules and other fields.

1.1 Part Naming Rules



1.2 Part Function Comparison Table

Table 1-1 Model Function Comparison Table

Function		Product Model								
		HC32F460 PEHB	HC32F460 PETB	HC32F460 PCTB	HC32F460 KETA	HC32F460 KCTA	HC32F460 JETA	HC32F460 JCTA	HC32F460 JEUA	HC32F460 KEUA
Flash Memory (KB)		512	512	256	512	256	512	256	512	512
Pin number		100	100	100	64	64	48	48	48	60
Number of GPIOs		83	83	83	52	52	38	38	38	50
5 V Tolerant Number of GPIOs		81	81	81	50	50	36	36	36	48
Encapsulation		VFBGA	LQFP						QFN	
Temperature range		-40-105 ℃			-40-85 ℃					
Supply voltage range		1.8~3.6 V								
OTP(Byte)		960								
SRAM(KB)		192								
DMA		2unit * 4ch								
External port interrupt		EIRQ * 16vec + NMI * 1ch								
Communcation Interfaces (The minimum number of IOs required for each ch is in parentheses)	UART	4ch (2)								
	SPI	4ch (3)								
	I2C	3ch (2)								
	I2S	4ch (3)								
	CAN	1ch (2)								
	QSPI	1ch (6)								
	SDIO	2ch (3)								
	USB-FS	1ch (2)								
Timers	Timer0	2unit								
	TimerA	6unit								
	Timer4	3unit								
	Timer6	3unit								
	WDT	1ch								
	SWDT	1ch								
	RTC	1ch								

Function		Product Model								
		HC32F460 PEHB	HC32F460 PETB	HC32F460 PCTB	HC32F460 KETA	HC32F460 KCTA	HC32F460 JETA	HC32F460 JCTA	HC32F460 JEUA	HC32F460 KEUA
Analog	12bit ADC	2unit, 16ch					2unit, 10ch			2unit, 15ch
	PGA	1ch								
	CMP	3ch								
	OTS	✓								
AES128		✓								
HASH (SHA256)		✓								
TRNG		✓								
Frequency Monitoring Module (FCM)		✓								
Programmable voltage detection function (PVD)		✓								
Debug interface		SWD								
		JTAG								

1.3 Functional Block Diagram

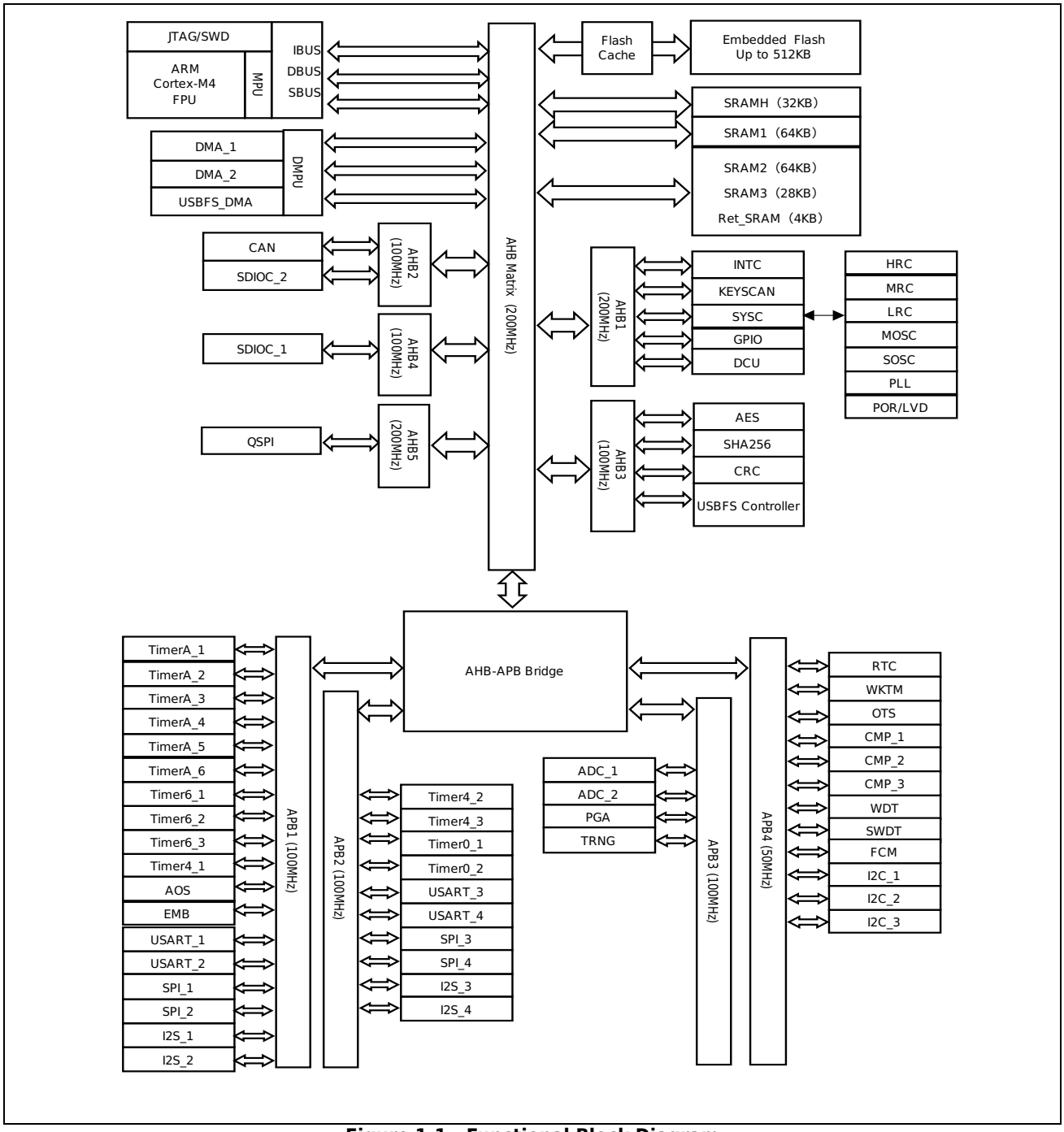


Figure 1-1 Functional Block Diagram

1.4 Feature Brief

1.4.1 CPU

The HC32F460 series integrates the latest generation of embedded ARM® Cortex®-M4 with FPU 32bit, which realizes fewer pins and lower power consumption while providing excellent computing performance and rapid interrupt response capability. The on-chip integrated storage capacity can give full play to the excellent instruction efficiency of ARM® Cortex®-M4 with FPU. The CPU supports DSP instructions, which can realize efficient signal processing operations and complex algorithms. The single-point precision FPU (Floating Point Unit) unit can avoid instruction saturation and speed up software development.

1.4.2 Bus Architecture (BUS)

The main system is composed of 32-bit multilayer AHB bus matrix, which can interconnect the following host bus and slave bus.

Host bus

- Cortex-M4F core CPU-I bus, CPU-D bus, CPU-S bus
- System DMA_1 bus, system DMA_2 bus
- USBFS_DMA bus

Slave bus

- Flash ICODE bus
- Flash DCODE bus
- Flash MCODE bus (bus for other hosts other than CPU to access Flash)
- SRAMH bus (SRAMH 32kB)
- SRAMA bus (SRAM1 64KB)
- SRAMB bus (SRAM2 64KB, SRAM3 28KB, Ret_SRAM 4KB)
- APB1 peripheral bus (AOS/EMB/Timers/SPI/USART/I2S)
- APB2 Peripheral Bus (Timers/SPI/USART/I2S)
- APB3 peripheral bus (ADC/PGA/TRNG)
- APB4 peripheral bus (FCM/WDT/CMP/OTS/RTC/WKTM/I2C)
- AHB1 peripheral bus (KEYSCAN/INTC/DCU/GPIO/SYSC)
- AHB2 peripheral bus (CAN/SDIOC)
- AHB3 peripheral bus (AES/HASH/CRC/USB FS)
- AHB4 peripheral bus (SDIOC)
- AHB5 peripheral bus (QSPI)

With the help of the bus matrix, high-efficiency concurrent access from the host bus to the slave bus can be realized.

1.4.3 Reset Control (RMU)

The chip is configured with 14 reset modes.

- Power-on Reset (POR)
- NRST pin reset (NRST)
- Brown-out Reset (BOR)
- Programmable Voltage Detect 1 Reset (PVD1R)
- Programmable Voltage Detect 2 Reset (PVD2R)
- Watchdog Reset (WDTR)
- Special watchdog reset (SWDTR)
- Power-down wake-up reset (PDRST)
- Software Reset (SRST)
- MPU Error Reset (MPUR)
- RAM Parity Reset (RAMPR)
- RAMECC reset (RAMECCR)
- Clock exception reset (CKFER)
- External High Speed Oscillator Abnormal Shock Reset (XTALER)

1.4.4 Clock Control (CMU)

The clock control unit provides a series of frequency clock functions, including: an external high-speed oscillator, an external low-speed oscillator, two PLL clocks, an internal high-speed oscillator, an internal medium-speed oscillator, an internal low-speed oscillator, A SWDT dedicated internal low-speed oscillator, clock prescaler, clock multiplexing and clock gating circuits.

The clock control unit also provides a clock frequency measurement function. The clock frequency measurement circuit (FCM) monitors and measures the measurement target clock using the measurement reference clock. An interrupt or reset occurs when the setting range is exceeded.

The AHB, APB and Cortex-M4 clocks all originate from the system clock. The system clock source has three timers:

1) External high-speed oscillator (XTAL)
2) External low-speed oscillator (XTAL32)
3) MPLL clock (MPLL)
4) Internal high-speed oscillator (HRC)
5) Internal medium speed oscillator (MRC)
6) Internal low-speed oscillator (LRC)

The maximum operating clock frequency of the system clock can reach 200 MHz. SWDT has an independent clock source: SWDT dedicated internal low-speed oscillator (SWDTLRC). The real-time clock (RTC) uses an external low-speed oscillator or an internal low-speed oscillator as a clock

source. The 48MHz clock of USB-FS and I2S communication clock can choose system clock, MPLL, UPLL as the clock source.

For each clock source, it can be turned on and off individually. It is recommended to turn off unused clock sources to reduce power consumption.

1.4.5 Power Control (PWC)

Power controller is used to control the supply, switching and detection of multiple power domains in multiple operation modes and low power modes. The power controller is composed of power control logic (PWCL) and power voltage detection unit (PVD).

The operating voltage (VCC) of the chip is 1.8 V to 3.6 V. A voltage regulator (LDO) supplies power to the VDD and VDDR domains, and a VDDR voltage regulator (RLDO) supplies power to the VDDR domain in power-down mode. The chip provides three operating modes of super high speed, high speed and super low speed through the power control logic (PWCL), and three low power modes such as sleep, stop and power down.

The power voltage detection unit (PVD) provides functions such as power-on reset (POR), power-down reset (PDR), brown-out reset (BOR), programmable voltage detection 1 (PVD1), and programmable voltage detection 2 (PVD2). Among them, POR, PDR, and BOR control the reset action of the chip by detecting the VCC voltage. PVD1 detects the VCC voltage and resets or interrupts the chip according to the register settings. PVD2 detects VCC voltage or external input detection voltage, and generates reset or interrupt according to register selection.

After the chip enters power-down mode, the VDDR area can maintain power through RLDO to ensure that the real-time clock module (RTC) and wake-up timer (WKTM) can continue to operate, and maintain the data of 4KB low-power SRAM (Ret-SRAM). The analog blocks are equipped with dedicated supply pins for improved analog performance.

1.4.6 Initialization Configuration (ICG)

After the chip is reset, the hardware circuit reads the main flash memory address 0x0000_0400~0x0000_041F (where 0x0000_0408~0x0000_041F is the reserved function address, the 24 bytes address requires the user to set all 1 to ensure normal chip operation) and loads the data to the initialization configuration register. The users need to program or erase FLASH sector 0 to modify the initialization configuration register.

1.4.7 Embedded FLASH Interface (EFM)

The FLASH interface accesses the FLASH through the ICODE, DCODE and MCODE buses. This interface can perform programming, sector erase and full erase operations on the FLASH; it accelerates code execution through the instruction prefetch and cache mechanism.

Main features:

- Maximum 512KByte FLASH space
- I-CODE bus 16Byte prefetch value
- Shared 64 caches (1Kbyte) on the I-CODE and D-CODE buses
- Provide 960Bbyte one-time programming area (OTP)
- Supports low-power read operations
- Support boot swap function
- Support security protection and data encryption*1

*1: For the specific specifications of Flash security protection and data encryption, please consult the sales window.

1.4.8 Built-in SRAM (SRAM)

This product has 4KB power-down mode retention SRAM (Ret_SRAM) and 188KB system SRAM (SRAMH/SRAM1/SRAM2/SRAM3).

SRAM can be accessed by byte, half word (16 bits) or full word (32 bits). Read and write operations are performed at CPU speed, with insertable wait cycles.

Ret_SRAM can provide 4KB data holding space in Power down mode.

SRAM3 has ECC check (Error Checking and Correcting). ECC check is one-check-two code, which can correct one bit error and check two bit errors; SRAMH/SRAM1/SRAM2/Ret_SRAM has parity check (Even- parity check), each byte of data has a parity bit.

1.4.9 General IO (GPIO)

Main Features of GPIO:

- Each port group has 16 I/O Pins, which may be less than 16 depending on actual configuration
- Support pull-up
- Support push-pull, open-drain output mode
- Supports high, medium and low drive modes
- Support for external interrupt input
- Support I/O pin peripheral function multiplexing, each I/O pin has a maximum of 16 optional multiplexing functions, and some I/Os have a maximum of 64 optional functions
- Individual I/O pins can be programmed independently
- Each I/O pin can select 2 functions to be valid at the same time (does not support 2 output functions to be valid at the same time)

1.4.10 Interrupt Control (INTC)

The function of the interrupt controller (INTC) is to select an interrupt event request as an interrupt input to the NVIC to wake up WFI; as an event input to wake up WFE. Select interrupt event request as the wake-up condition of low power consumption mode (sleep mode and stop mode); interrupt control function of external pins NMI and EIRQ; interrupt/event selection function of software interrupt.

Main specifications:

1) NVIC interrupt vector: Please refer to the user manual for the actual number of interrupt vectors used (excluding the 16 interrupt lines of Cortex™-M4F), each interrupt vector can select the corresponding peripheral interrupt event request according to the interrupt selection register. For more instructions on exceptions and NVIC programming, please refer to Chapter 5: Exceptions and Chapter 8: Nested Vectored Interrupt Controller in the "ARM Cortex™-M4F Technical Reference Manual".
2) Programmable priority: 16 programmable priorities (using 4-bit interrupt priority).
3) Non-maskable interrupts: In addition to NMI pins as non-maskable interrupt sources, multiple system interrupt event requests can be independently selected as non-maskable interrupts, and each interrupt event request is equipped with independent enable selection, suspend, and clear pending registers.
4) Equipped with 16 external pin interrupts.
5) Configure various peripheral interrupt event requests, please refer to the interrupt event request sequence number list for details.
6) Equipped with 32 software interrupt event requests.
7) Interrupt wakes up system sleep mode and stop mode.

1.4.11 Automatic Operation System (AOS)

The automatic operation system (Automatic Operation System) is used to realize the linkage between peripheral hardware circuits without the help of the CPU. Use the events generated by the peripheral circuit as the AOS source (AOS Source), such as the comparison and matching of the timer, timing overflow, the periodic signal of the RTC, and the various states of the communication module's sending and receiving data (idle, receiving data full, sending data end, send data empty), ADC conversion end, etc., to trigger other peripheral circuit actions. The triggered peripheral circuit action is called AOS target (AOS Target).

1.4.12 Keyboard Scanning (KEYSCAN)

This product is equipped with a keyboard control module (KEYSCAN) 1 unit. The KEYSCAN module supports keyboard array (row and column) scanning, the column is driven by an independent scan

output KEYOUTm (m=0~7), and the row KEYINn (n=0~15) is input as EIRQn (n=0~15) is detected. This module realizes the key recognition function through the line scan query method.

1.4.13 Memory Protection Unit (MPU)

The MPU can provide protection to the memory, and can improve the security of the system by preventing unauthorized access.

This product has built-in four MPU units for host and one MPU unit for IP.

Among them, the ARM MPU provides the access control of the CPU to the entire 4G address space.

DMA MPU (DMPU) provides DMA_1/DMA_2/USB FS DMA's read and write access control to the entire 4G address space. When accessing the prohibited space, the MPU action can be set to ignore/bus error/non-maskable interrupt/reset.

The IP MPU provides access control to system IP and security-related IP in non-privileged mode.

1.4.14 DMA Controller (DMA)

DMA is used to transfer data between memory and peripheral functional modules. It can exchange data between memory, between memory and peripheral functional modules and between peripheral functional modules without CPU involvement.

- DMA bus is independent of CPU bus and transmitted according to AMBA AHB-Lite bus protocol.
- With 8 independent channels (4 channels each for DMA_1 and DMA_2), different DMA transfer functions can be operated independently
- For each channel, the source of the boot request is configured via a separate trigger source
- One block per request
- The data block is a minimum of one data and can be up to 1024 data
- Each data can be configured to 8 bits, 16 bits or 32 bits
- Up to 65535 transmissions can be configured
- The source address and target address can be independently configured as fixed, auto-increment, auto-decrement, loop or jump with a specified offset
- Three types of interrupts can be generated, block transport complete interrupt, transport complete interrupt, and transport error interrupt. Each interrupt can be configured with a mask or not. Where block transport is complete, transport complete can be used as event output, as trigger source input for other peripheral modules with hardware trigger function
- Support for linked transmission to enable multiple blocks of data to be transmitted at a time
- Support channel reset triggered by external events
- You can set the module stop state to reduce power consumption when not in use

1.4.15 Voltage Comparator (CMP)

CMP is a peripheral module that compares two analog voltages INP and INM and outputs the comparison result. CMP has 3 independent comparison channels, and the analog voltage INP and INM of each comparison channel have 4 input sources. When in use, one INP can be selected for a single comparison with one INM, or multiple INPs can be scanned and compared with the same INM. The comparison result can be read through registers, can also be output to external pins, and can also generate interrupts and events.

1.4.16 Analog-to-Digital Converter (ADC)

12-bit ADC is an analog-to-digital converter with successive approximation. It has a maximum of 16 analog input channels, which can convert external ports and internal analog signals. These channels can be arbitrarily combined into a sequence for scan-by-scan conversion, and the sequence can be converted for single or continuous scans. It supports multiple consecutive conversions on any specified channel and averages the conversion results. The ADC module also carries the analog watchdog function, monitors the conversion result of any specified channel, and detects whether it exceeds the threshold set by the user.

Main Features of ADC:

- High performance
  - Configurable 12-bit, 10-bit and 8-bit resolution
  - The frequency ratio of peripheral clock PCLK4 and A/D conversion clock ADCLK can be selected:
    - PCLK4: ADCLK=1:1, 2:1, 4:1, 8:1, 1:2, 1:4
    - ADCLK can choose a PLL that is asynchronous to the system clock HCLK. At this time, the clock sources of PCLK4 and ADCLK are fixed as PLL at the same time, and the frequency ratio is 1:1. The original frequency division setting is invalid.
  - 2.5MSPS (PCLK4=ADCLK=60MHz, 12 bits, sampling 17 cycles)
  - The sampling time of each channel is independently programmed
  - Channel-independent data register
  - Data register configurable data alignment
  - Consecutive multiple conversion average function
  - Simulation watchdog, monitoring conversion results
  - The ADC module can be set to stop when not in use
- Analog input channel
  - Maximum 16 external analog input channels
  - 1 internal reference voltage
- Conversion start condition
  - Software Setup Conversion Started

  - Start of Peripheral Device Synchronization Trigger Conversion
  - External Pin Triggering Start
- Conversion mode
  - 2 scan sequences A and B, optionally specifying a single or multiple channels
  - Sequence A single scan
  - Sequence A continuous scanning
  - Double sequence scanning, sequence A and B independently select trigger source, sequence B has higher priority than A
  - Synchronous mode (for devices with two or three ADCs)
- Interrupt and Event Signal Output
  - Sequence A scan end interrupt EOCA_INT and event EOCA_EVENT
  - Sequence B scan end interrupt EOCB_INT and event EOCB_EVENT
  - Analog watchdog channel compares interrupt CHCMP_INT and event CHCMP_EVENT, sequence compare interrupt SEQCMP_INT and event SEQCMP_EVENT
  - The above 4 events can start DMA

1.4.17 Temperature Sensor (OTS)

OTS can obtain the temperature inside the chip to support the reliability operation of the system. After using software or hardware to trigger the temperature measurement, OTS provides a set of temperature-related digital quantities, and the temperature value can be calculated through the calculation formula.

1.4.18 Advanced Control Timer (Timer6)

Advanced Control Timer 6 (Timer6) is a high-performance timer with a 16-bit count width, which can be used to count and generate different forms of clock waveforms, and output them for external use. The timer supports two waveform modes of triangle wave and sawtooth wave, and can generate various PWM waveforms; software synchronous counting and hardware synchronous counting can be realized between units; each reference value register supports cache function; supports 2-phase quadrature encoding and 3-phase quadrature Cross coding; support EMB control. This series of products is equipped with 3 units of Timer6.

1.4.19 General Control Timer (Timer4)

General control timer 4 (Timer4) is a timer module for three-phase motor control. It provides three-phase motor control schemes for various applications. The timer supports triangular wave and sawtooth wave modes and generates various PWM waveforms. Supporting cache function; Support EMB control. 3 unit of Timer 4 is carried in this product family.

1.4.20 Emergency Brake Module (EMB)

The Emergency Brake Module is a functional module that notifies the timer to stop the output of PWM signals to the external motor when certain conditions are met. The following events are used to generate notifications:

- Change of input level of external port
- Level of PWM output port occurs in phase (same high or same low)
- Voltage comparator comparison results
- External oscillator stop oscillation
- Write register software control

1.4.21 General Timer (TimerA)

General Timer A (Timer A) is a timer with 16-bit count width and 8 PWM outputs. The timer supports two waveform modes of triangle wave and sawtooth wave, and can generate various PWM waveforms; it supports software synchronous start counting; the comparison reference value register supports buffer function; it supports 2-phase quadrature encoding counting and 3-phase quadrature encoding counting. This series of products is equipped with 6 units TimerA, which can realize a maximum of 48 PWM outputs.

1.4.22 General Timer (Timer0)

General timer 0 (Timer0) is a basic timer that can realize synchronous counting and asynchronous counting. The timer contains 2 channels, which can generate compare match events during counting. The event can trigger interrupt, or can be output as an event to control other modules. This series of products is equipped with 2 units of Timer0.

1.4.23 Real Time Clock (RTC)

A real-time clock (RTC) is a counter that stores time information in BCD format. Record the specific calendar time from 00 to 99. Support 12/24-hour time system, automatically calculate the number of days 28, 29 (leap year), 30 and 31 according to the month and year.

1.4.24 Watchdog Counter (WDT)

There are two watchdog counters, one is a dedicated watchdog counter (SWDT) whose count clock source is a dedicated internal RC (WDTCLK: 10KHz), and the other is a general watchdog counter (WDT) whose count clock source is PCLK3). The dedicated watchdog and general watchdog are 16-bit down counters used to monitor software failures due to external disturbances or unforeseen logic conditions that deviate from the normal operation of the application program.

Both watchdogs support window functions. The window interval can be preset before the count starts, and when the count value is within the window interval, the counter can be refreshed and the count restarted.

1.4.25 Serial Communication Interface (USART)

This product is equipped with 4 units of serial communication interface module (USART). The serial communication interface module (USART) can flexibly perform full-duplex data exchange with external devices; this USART supports universal asynchronous serial communication interface (UART), clock synchronous communication interface, and smart card interface (ISO/IEC7816-3). Support modem operation (CTS/RTS operation), multiprocessor operation.

1.4.26 Integrated Circuit Bus (I2C)

This product is equipped with 3 units of integrated circuit bus (I2C). I2C is used as an interface between the microcontroller and the I2C serial bus. Provide multi-master mode function, which can control the protocol and arbitration of all I2C buses. Standard mode and fast mode are supported.

1.4.27 Serial Peripheral Interface (SPI)

This product is equipped with 4-channel serial peripheral interface SPI, supports high-speed full-duplex serial synchronous transmission, and facilitates data exchange with peripheral devices. Users can set the range of 3/4-wire, host/slave and baud rate as needed.

1.4.28 Quad-wire Serial Peripheral Interface (QSPI)

The Quad Serial Peripheral Interface (QSPI) is a memory control module designed to communicate with serial ROMs with an SPI-compatible interface. Its objects mainly include serial flash memory, serial EEPROM and serial FeRAM.

1.4.29 Integrated Circuit Audio Bus (I2S)

I2S (Inter_IC Sound Bus), integrated circuit built-in audio bus, which is dedicated to data transmission between audio devices. This product is equipped with 4 I2S and has the following characteristics.

Function	Main characteristics
Communication mode	· Support full-duplex and half-duplex communication · Support host mode or slave mode operation
Data format	· Optional channel length: 16/32 bits · Optional transmission data length: 16/24/32 bits · Data shift order: MSB start
Baud rate	· 8-bit programmable linear prescaler for precise audio sampling frequency · Support sampling frequency 192k, 96k, 48k, 44.1k, 32k, 22.05k, 16k, 8k · Can output driving clock to drive external audio components, the ratio is fixed at 256*Fs (Fs is the audio sampling frequency)
Support I2S protocol	· I2S Philips Standard · MSB Alignment Standard · LSB Alignment Standard · PCM standard
Data buffer	· With 2-word deep, 32-bit wide input and output FIFO buffer area
Timer	· Can use internal I2SCLK (UPLLR/UPLLQ/UPLLP/MPLLR/MPLLQ/MPLLP); can also be supplied by external clock on I2S_EXCK pin
Interrupt	· An interrupt is generated when the effective space of the send buffer reaches the alarm threshold · An interrupt is generated when the effective space of the receive buffer reaches the alarm threshold · The receiving data area is full and there is still a request to write data, and the receiving overflows · The sending data area is empty and there are still sending requests, sending underflow · The sending data area is full and there is still a request to write data, sending overflow

1.4.30 CAN Communication Interface (CAN)

This product is equipped with a CAN communication interface module (CAN), and is equipped with a 512Byte RAM for CAN to store sending/receiving messages. Support CAN2.0B protocol specified in ISO11898-1 and TTCAN protocol specified in ISO11898-4.

1.4.31 USB2.0 Full Speed Module (USB FS)

This product is equipped with one unit of USB2.0 full-speed module (USB FS), and built-in full-speed PHY on chip. The USB FS is a dual-role (DRD) controller that supports both slave and host functions. In host mode, USB FS supports both full-speed and low-speed transceivers, while in slave mode only full-speed transceivers are supported.

The USB FS module equipped with this product can generate SOF events when the host mode successfully sends the SOF token or the slave mode successfully receives the SOF token.

1.4.32 Cryptographic Coprocessing Module (CPM)

The encryption co-processing module (CPM) includes three sub-modules: AES encryption and decryption algorithm processor, HASH security hash algorithm, and TRNG true random number generator.

The AES encryption and decryption algorithm processor follows the standard data encryption and decryption standards, and can realize encryption and decryption operations with a key length of 128 bits.

The HASH secure hash algorithm is the SHA-2 version of SHA-256 (Secure Hash Algorithm), which complies with the national standard "FIPS PUB 180-3" issued by the US National Institute of Standards and Technology, and can process messages with a length of no more than 2^64 bits. Produces a 256-bit message digest output.

TRNG true random number generator is a random number generator based on continuous analog noise, providing 64bit random numbers.

1.4.33 Data Computing Unit (CRC)

The Data Computing Unit (Data Computing Unit) is a module that simply processes data without the help of a CPU. Each DCU unit has 3 data registers, which can add, subtract and compare the size of 2 data, as well as the window comparison function. This product is equipped with 4 DCU units, and each unit can independently complete its own functions.

1.4.34 CRC Unit (CRC)

The CRC algorithm of this module complies with the definition of ISO/IEC 13239 and adopts 32-bit and 16-bit CRC respectively. The CRC32 generating polynomial is $X^{32}+ X^{26}+ X^{23}+ X^{22}+ X^{16}+ X^{12}+ X^{11}+ X^{10}+ X^{8}+ X^{7}+ X^{5}+ X^{4}+ X^{2}+ X+ 1$. The generating polynomial of CRC16 is $X^{16}+ X^{12}+ X^{5}+ 1$.

1.4.35 SDIO Controller (SDIOC)

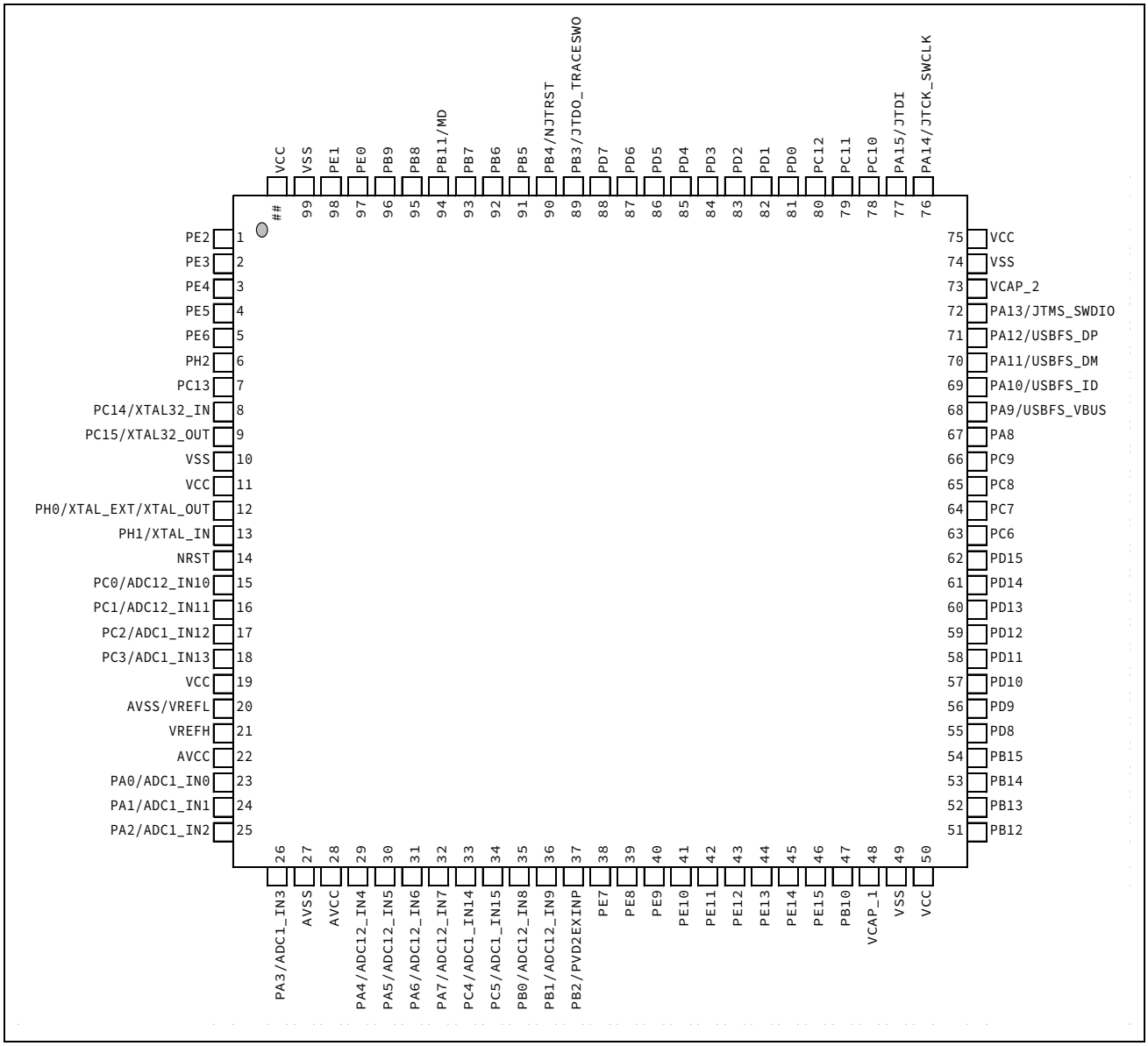
The SDIO controller is the host in the SD/SDIO/MMC communication protocol. This product has 2 SDIO controllers, and each SDIO controller provides a host interface for communicating with SD cards supporting SD2.0 protocol, SDIO devices and MMC devices supporting eMMC4.51 protocol. The characteristics of SDIOC are as follows:

- Support SDSC, SDHC, SDXC format SD card and SDIO device
- Support one-line (1bit) and four-wire (4bit) SD bus
- Support one-line (1bit), four-wire (4bit) and eight-wire (8bit) MMC bus
- With card identification and hardware write protection function

2 Pin Configuration and Functions (Pinouts)

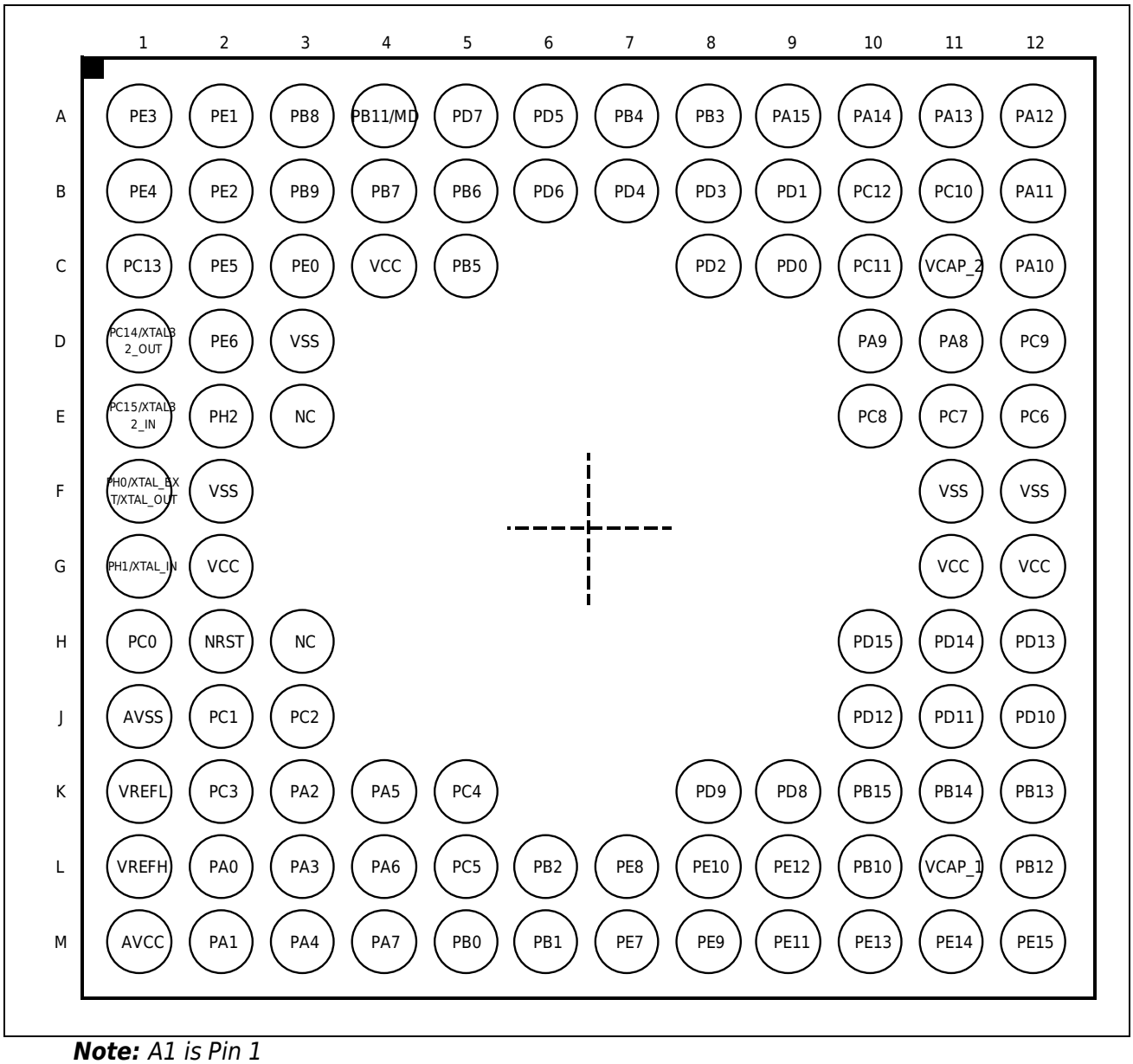
2.1 Pin Configuration Diagram

HC32F460PETB-LQFP100/ HC32F460PCTB-LQFP100



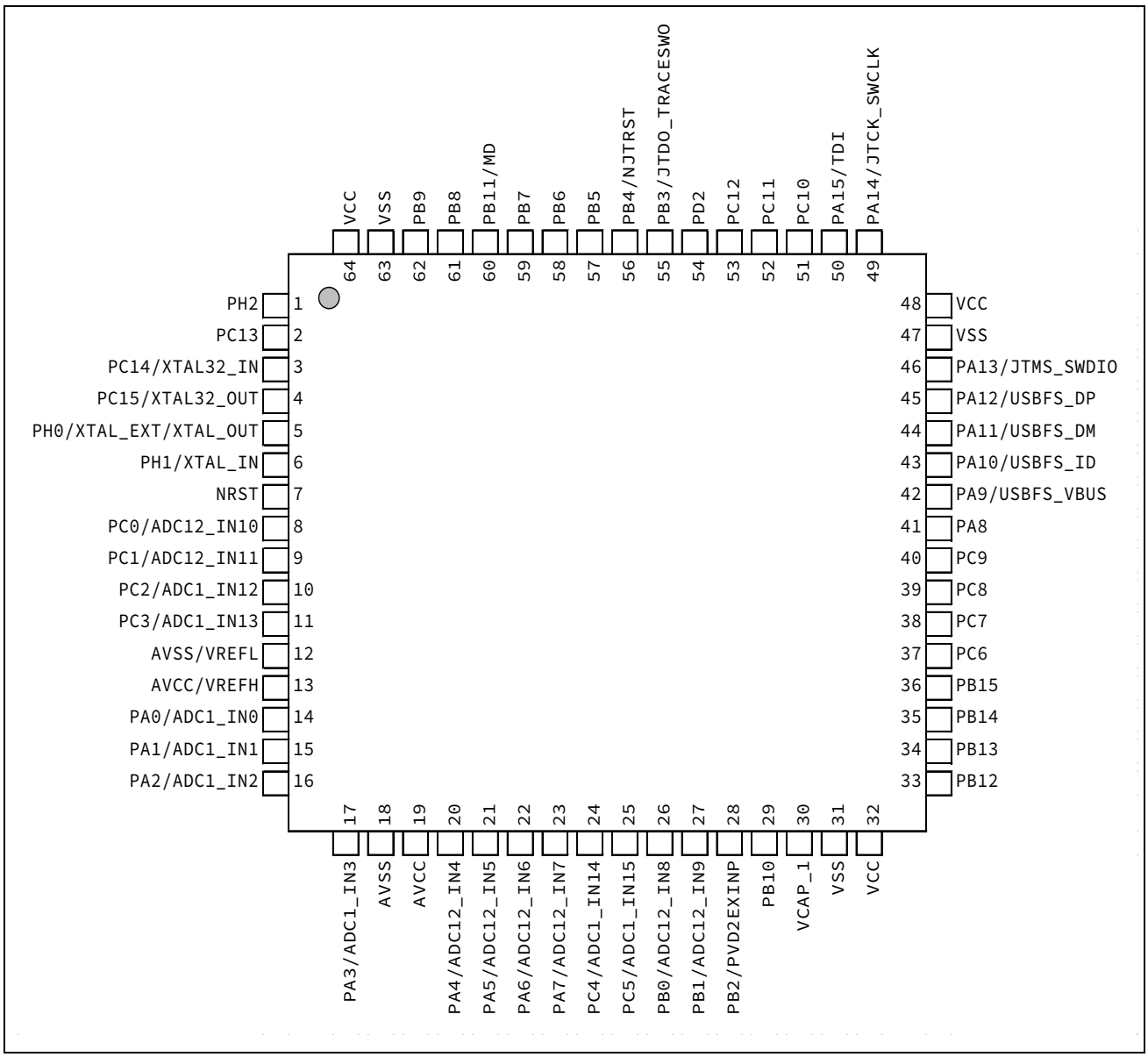
HC32F460PEHB-VFBGA100

(Top View)

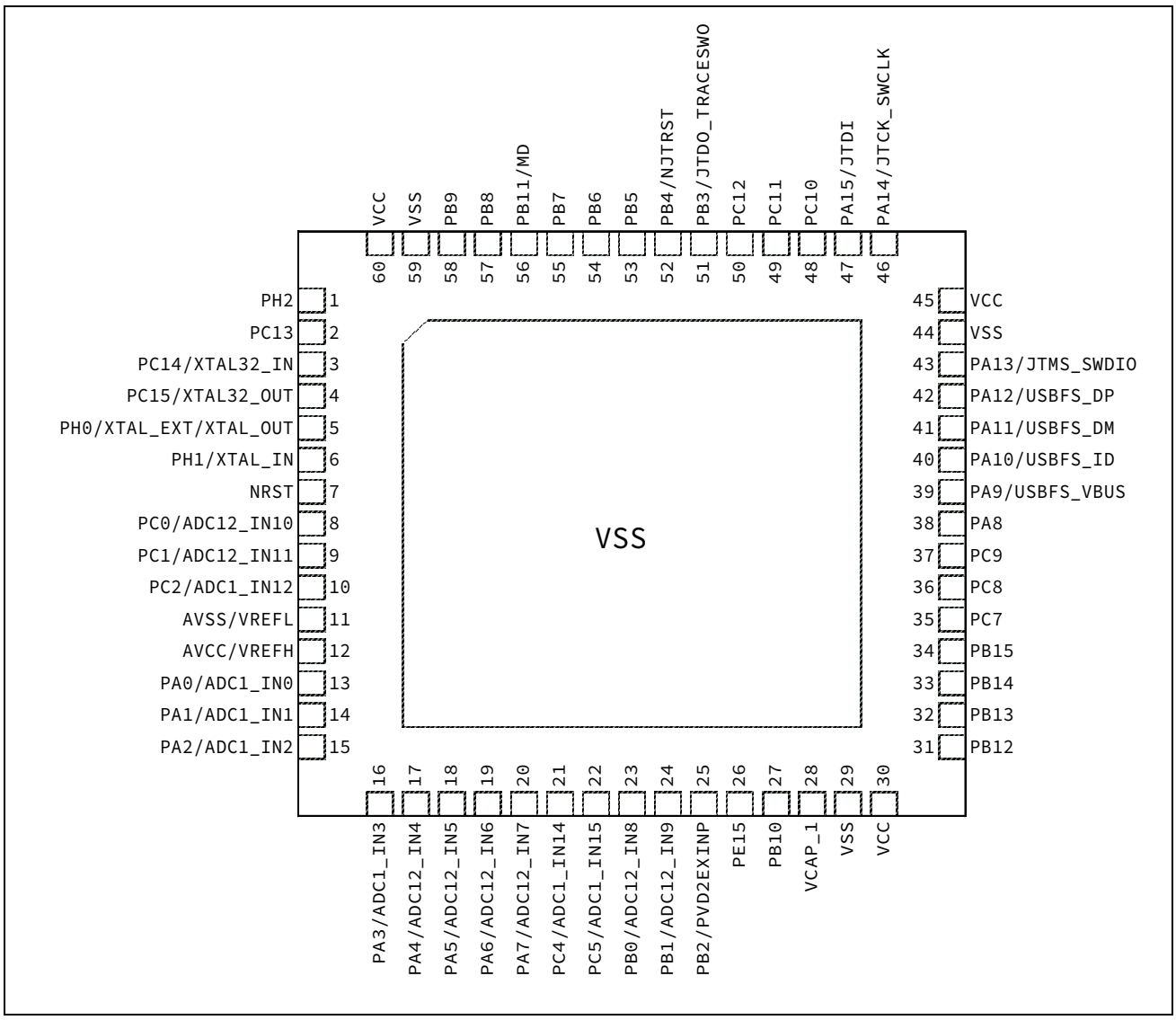


Note: *A1 is Pin 1*

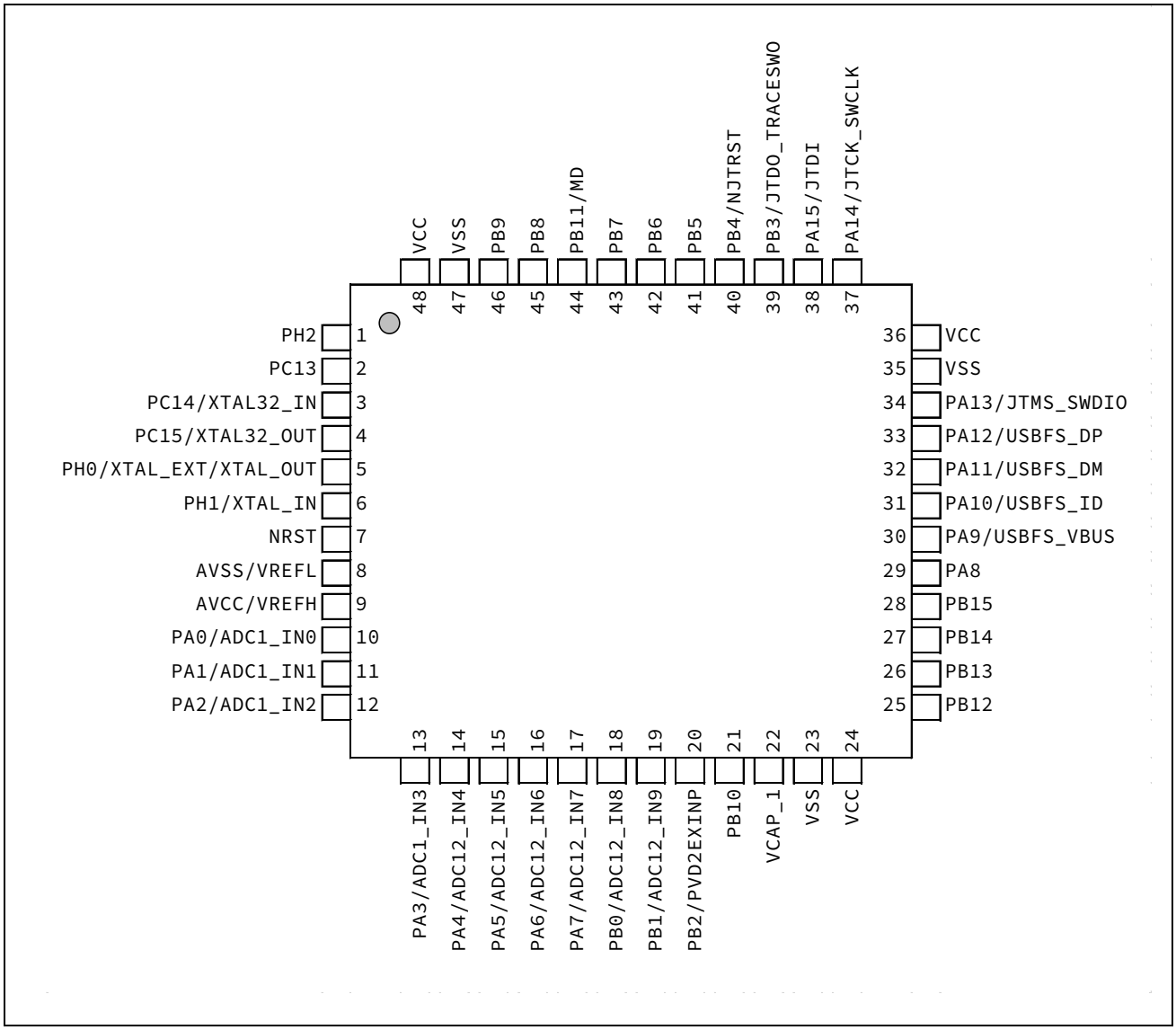
HC32F460KETA-LQFP64/HC32F460KCTA-LQFP64



HC32F460KEUA-QFN60TR



HC32F460JETA-LQFP48/ HC32F460JCTA-LQFP48



HC32F460JEUA-QFN48TR

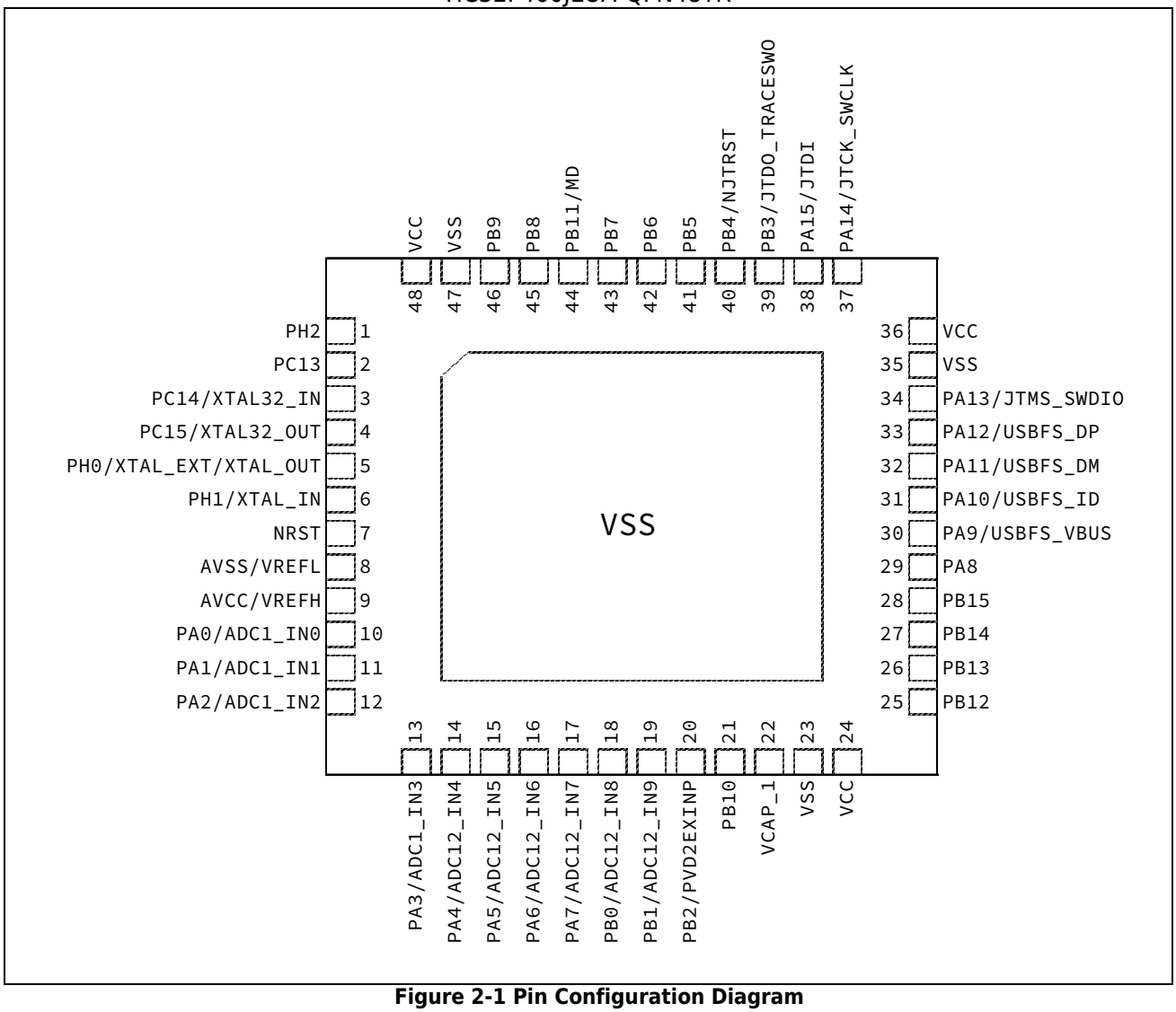


Figure 2-1 Pin Configuration Diagram

2.2 Pin Function Table

Table 2-1 Pin Function Table

LQFP100	VFBGA100	LQFP64	QFN60	LQFP/QFN48	Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16~31	Func32~63
									GPO	other	TIM4	TIM6	TIMA	TIMA	EMB,TIMA	USART/SPI/ QSPI	KEY	SDIO	USBFS/I2S	-	-	-	EVNTPT	EVENTOUT	-	Communication Funcs
1	B2	-	-	-	PE2	-	EIRQ2	TRACECK	GPO	-	-	-	TIMA_3_PWM5	-	-	USART3_CK	-	-	-	-	-	-	-	EVENTOUT	-	Func_Grp2
2	A1	-	-	-	PE3	-	EIRQ3	TRACED0	GPO	-	-	-	TIMA_3_PWM6	-	-	USART4_CK	-	-	-	-	-	-	-	EVENTOUT	-	Func_Grp2
3	B1	-	-	-	PE4	-	EIRQ4	TRACED1	GPO	-	-	-	TIMA_3_PWM7	-	-	-	-	-	-	-	-	-	-	EVENTOUT	-	Func_Grp2
4	C2	-	-	-	PE5	-	EIRQ5	TRACED2	GPO	-	-	-	TIMA_3_PWM8	-	-	-	-	-	-	-	-	-	-	EVENTOUT	-	Func_Grp2
5	D2	-	-	-	PE6	-	EIRQ6	TRACED3	GPO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT	-	Func_Grp2
6	E2	1	1	1	PH2	-	EIRQ2	-	GPO	FCMREF	TIM4_2_CLK	-	TIMA_4_PWM7	-	EMB_IN4	-	-	SDIO2_D4	I2S3_EXCK	-	-	-	-	EVENTOUT	-	Func_Grp2
7	C1	2	2	2	PC13	-	EIRQ13	-	GPO	RTC_OUT	-	-	TIMA_4_PWM8	-	-	-	-	SDIO2_CK	I2S3_MCK	-	-	-	EVNTP313	-	-	Func_Grp2
8	D1	3	3	3	PC14	XTAL32_IN	EIRQ14	-	GPO	-	-	-	TIMA_4_PWM5	-	-	-	-	-	-	-	-	-	EVNTP314	-	-	-
9	E1	4	4	4	PC15	XTAL32_OUT	EIRQ15	-	GPO	-	-	-	TIMA_4_PWM6	-	-	-	-	-	-	-	-	-	EVNTP315	-	-	-
10	F2	-	-	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
11	G2	-	-	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
12	F1	5	5	5	PH0	XTAL_EXT/XTAL_OUT	EIRQ0	-	GPO	-	-	-	-	TIMA_5_PWM3	-	-	-	-	-	-	-	-	-	-	-	-
13	G1	6	6	6	PH1	XTAL_IN	EIRQ1	-	GPO	-	-	-	-	TIMA_5_PWM4	-	-	-	-	-	-	-	-	-	-	-	-
14	H2	7	7	7	NRST	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	H1	8	8	-	PC0	ADC12_IN10/CMP3_INP3	EIRQ0	-	GPO	-	-	-	TIMA_2_PWM5	-	-	-	-	SDIO2_D5	-	-	-	-	EVNTP300	EVENTOUT	-	Func_Grp1
16	J2	9	9	-	PC1	ADC12_IN11	EIRQ1	-	GPO	-	-	-	TIMA_2_PWM6	-	-	-	-	SDIO2_D6	-	-	-	-	EVNTP301	EVENTOUT	-	Func_Grp1
17	J3	10	10	-	PC2	ADC1_IN12	EIRQ2	-	GPO	-	-	-	TIMA_2_PWM7	-	EMB_IN3	-	-	SDIO2_D7	-	-	-	-	EVNTP302	EVENTOUT	-	Func_Grp1
18	K2	11	-	-	PC3	ADC1_IN13/CMP1_INM2	EIRQ3	-	GPO	-	-	-	TIMA_2_PWM8	-	-	-	-	SDIO1_WP	-	-	-	-	EVNTP303	EVENTOUT	-	Func_Grp1
19	-	-	-	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
20	J1	12	11	8	AVSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	K1	-	-	-	VREFL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
21	L1	-	-	-	VREFH	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
22	M1	13	12	9	AVCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
23	L2	14	13	10	PA0	ADC1_IN0/CMP1_INP1	EIRQ0/WKUP0_0	-	GPO	-	TIM4_2_OUH	-	TIMA_2_PWM1/TIMA_2_CLKA	-	TIMA_2_TRIG	SPI1_SS1	-	SDIO2_D4	-	-	-	-	EVNTP100	EVENTOUT	-	Func_Grp1
24	M2	15	14	11	PA1	ADC1_IN1/CMP1_INP2	EIRQ1	-	GPO	-	TIM4_2_OUL	-	TIMA_2_PWM2/TIMA_2_CLKB	TIMA_3_TRIG	-	SPI1_SS2	-	SDIO2_D5	-	-	-	-	EVNTP101	EVENTOUT	-	Func_Grp1
25	K3	16	15	12	PA2	ADC1_IN2/CMP1_INP3	EIRQ2	-	GPO	-	TIM4_2_OVH	-	TIMA_2_PWM3	TIMA_5_PWM1/TIMA_5_CLKA	-	SPI1_SS3	-	SDIO2_D6	-	-	-	-	EVNTP102	EVENTOUT	-	Func_Grp1
26	L3	17	16	13	PA3	ADC1_IN3/PGAVSS/CMP1_INP4	EIRQ3	-	GPO	-	TIM4_2_OVL	-	TIMA_2_PWM4	TIMA_5_PWM2/TIMA_5_CLKB	-	-	-	SDIO2_D7	-	-	-	-	EVNTP103	EVENTOUT	-	Func_Grp1
27	-	18	-	-	AVSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	E3	-	-	-	NC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
28	-	19	-	-	AVCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
29	M3	20	17	14	PA4	ADC12_IN4/CMP2_INP1/CMP3_INP4	EIRQ4	-	GPO	-	TIM4_2_OWH	-	-	TIMA_3_PWM5	-	USART2_CK	KEYOUT0	-	I2S1_EXCK	-	-	-	EVNTP104	EVENTOUT	-	Func_Grp1
30	K4	21	18	15	PA5	ADC12_IN5/CMP2_INP2	EIRQ5	-	GPO	-	TIM4_2_OWL	-	TIMA_2_PWM1/TIMA_2_CLKA	TIMA_3_PWM6	TIMA_2_TRIG	-	KEYOUT1	-	I2S1_MCK	-	-	-	EVNTP105	EVENTOUT	-	Func_Grp1
31	L4	22	19	16	PA6	ADC12_IN6/CMP2_INP3	EIRQ6	-	GPO	-	-	-	-	TIMA_3_PWM1/TIMA_3_CLKA	EMB_IN2	-	KEYOUT2	SDIO1_CMD	-	-	-	-	EVNTP106	EVENTOUT	-	Func_Grp1
32	M4	23	20	17	PA7	ADC12_IN7/CMP1_INM1/CMP2_INM1/CMP3_INM1	EIRQ7	-	GPO	-	TIM4_1_OUL	TIM6_1_PWMB	TIMA_1_PWM5	TIMA_3_PWM2/TIMA_3_CLKB	EMB_IN3	-	KEYOUT3	SDIO2_WP	-	-	-	-	EVNTP107	EVENTOUT	-	Func_Grp1

LQFP100	VFBGA100	LQFP64	QFN60	LQFP/QFN48	Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16~31	Func32~63
									GPO	other	TIM4	TIM6	TIMA	TIMA	EMB,TIMA	USART/SPI/ QSPI	KEY	SDIO	USBFS/I2S	-	-	-	EVNTPT	EVENTOUT	-	Communication Funcs
33	K5	24	21	-	PC4	ADC1_IN14/CMP2_IN M2	EIRQ4	-	GPO	-	TIM4_2_OUH	-	-	TIMA_3_PWM7	-	USART1_CK	-	SDIO2_CD	-	-	-	-	EVNTP304	EVENTOUT	-	Func_Grp1
34	L5	25	22	-	PC5	ADC1_IN15/CMP3_IN M2	EIRQ5	-	GPO	-	TIM4_2_OUL	-	-	TIMA_3_PWM8	-	-	-	SDIO2_CMD	-	-	-	-	EVNTP305	EVENTOUT	-	Func_Grp1
35	M5	26	23	18	PB0	ADC12_IN8/CMP3_IN P1	EIRQ0	-	GPO	-	TIM4_1_OVL	TIM6_2_PWMB	TIMA_1_PWM6	TIMA_3_PWM3	-	USART4_CK	KEYOUT4	SDIO2_CMD	-	-	-	-	EVNTP200	EVENTOUT	-	Func_Grp1
36	M6	27	24	19	PB1	ADC12_IN9/CMP3_IN P2	EIRQ1/WKUP0_ 1	-	GPO	-	TIM4_1_OWL	TIM6_3_PWMB	TIMA_1_PWM7	TIMA_3_PWM4	-	QSPI_QSSN	KEYOUT5	SDIO2_D3	I2S2_EXCK	-	-	-	EVNTP201	EVENTOUT	-	Func_Grp1
37	L6	28	25	20	PB2	PVD2EXINP	EIRQ2/WKUP0_ 2	-	GPO	VCOUT123	-	TIM6_TRIGB	TIMA_1_PWM8	-	EMB_IN1	QSPI_QSIO3	-	SDIO2_D2	I2S2_MCK	-	-	-	EVNTP202	EVENTOUT	-	Func_Grp1
38	M7	-	-	-	PE7	-	EIRQ7	-	GPO	ADTRG1	-	TIM6_TRIGA	TIMA_1_TRIG	-	-	USART1_CK	-	-	-	-	-	-	-	EVENTOUT	-	-
39	L7	-	-	-	PE8	-	EIRQ8	-	GPO	-	TIM4_1_OUL	TIM6_1_PWMB	TIMA_1_PWM5	-	-	-	-	-	-	-	-	-	-	EVENTOUT	-	-
40	M8	-	-	-	PE9	-	EIRQ9	-	GPO	-	TIM4_1_OUH	TIM6_1_PWMA	TIMA_1_PWM1/TIM A_1_CLKA	-	-	-	-	-	-	-	-	-	-	EVENTOUT	-	-
41	L8	-	-	-	PE10	-	EIRQ10	-	GPO	-	TIM4_1_OVL	TIM6_2_PWMB	TIMA_1_PWM6	-	-	-	-	-	-	-	-	-	-	EVENTOUT	-	-
42	M9	-	-	-	PE11	-	EIRQ11	-	GPO	-	TIM4_1_OVH	TIM6_2_PWMA	TIMA_1_PWM2/TIM A_1_CLKB	-	-	-	-	-	-	-	-	-	-	EVENTOUT	-	-
43	L9	-	-	-	PE12	-	EIRQ12	-	GPO	-	TIM4_1_OWL	TIM6_3_PWMB	TIMA_1_PWM7	-	-	SPI1_SS1	-	-	-	-	-	-	-	EVENTOUT	-	Func_Grp2
44	M10	-	-	-	PE13	-	EIRQ13	-	GPO	-	TIM4_1_OWH	TIM6_3_PWMA	TIMA_1_PWM3	-	-	SPI1_SS2	-	-	-	-	-	-	-	EVENTOUT	-	Func_Grp2
45	M11	-	-	-	PE14	-	EIRQ14	-	GPO	-	TIM4_1_CLK	-	TIMA_1_PWM4	-	-	SPI1_SS3	-	SDIO1_CD	-	-	-	-	-	EVENTOUT	-	Func_Grp2
46	M12	-	26	-	PE15	-	EIRQ15	-	GPO	-	-	-	TIMA_1_PWM8	TIMA_5_TRIG	EMB_IN2	USART4_CK	-	SDIO1_WP	-	-	-	-	-	EVENTOUT	-	Func_Grp2
47	L10	29	27	21	PB10	-	EIRQ10	-	GPO	ADTRG2	TIM4_2_OVH	-	TIMA_2_PWM3	TIMA_5_PWM8	-	QSPI_QSIO2	-	SDIO1_D7	I2S3_EXCK	-	-	-	EVNTP210	EVENTOUT	-	Func_Grp2
48	L11	30	28	22	VCAP_1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
49	F12	31	29	23	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
50	G12	32	30	24	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
51	L12	33	31	25	PB12	-	EIRQ12	-	GPO	VCOUT1	TIM4_2_OVL	TIM6_TRIGB	TIMA_1_PWM8	-	EMB_IN2	QSPI_QSIO1	-	SDIO2_D1	I2S3_MCK	-	-	-	EVNTP212	EVENTOUT	-	Func_Grp2
52	K12	34	32	26	PB13	-	EIRQ13	-	GPO	VCOUT2	TIM4_1_OUL	TIM6_1_PWMB	TIMA_1_PWM5	-	-	QSPI_QSIO0	-	SDIO2_D0	-	-	-	-	EVNTP213	EVENTOUT	-	Func_Grp2
53	K11	35	33	27	PB14	-	EIRQ14	-	GPO	VCOUT3	TIM4_1_OVL	TIM6_2_PWMB	TIMA_1_PWM6	-	-	QSPI_QSCK	-	SDIO1_D6	-	-	-	-	EVNTP214	EVENTOUT	-	Func_Grp2
54	K10	36	34	28	PB15	-	EIRQ15	-	GPO	RTC_OUT	TIM4_1_OWL	TIM6_3_PWMB	TIMA_1_PWM7	TIMA_6_TRIG	EMB_IN4	USART3_CK	-	SDIO1_CK	-	-	-	-	EVNTP215	EVENTOUT	-	Func_Grp2
55	K9	-	-	-	PD8	-	EIRQ8	-	GPO	-	TIM4_3_OUL	-	-	TIMA_6_PWM1/TIM A_6_CLKA	-	QSPI_QSIO0	KEYOUT7	-	-	-	-	-	EVNTP408	EVENTOUT	-	Func_Grp2
56	K8	-	-	-	PD9	-	EIRQ9	-	GPO	-	TIM4_3_OVL	-	-	TIMA_6_PWM2/TIM A_6_CLKB	-	QSPI_QSIO1	KEYOUT6	-	-	-	-	-	EVNTP409	EVENTOUT	-	Func_Grp2
57	J12	-	-	-	PD10	-	EIRQ10	-	GPO	-	TIM4_3_OWL	-	-	TIMA_6_PWM3	-	QSPI_QSIO2	KEYOUT5	-	-	-	-	-	EVNTP410	EVENTOUT	-	Func_Grp2
58	J11	-	-	-	PD11	-	EIRQ11	-	GPO	-	TIM4_3_CLK	-	-	TIMA_6_PWM4	-	QSPI_QSIO3	KEYOUT4	-	-	-	-	-	EVNTP411	EVENTOUT	-	Func_Grp2
59	J10	-	-	-	PD12	-	EIRQ12	-	GPO	-	-	-	TIMA_4_PWM1/TIM A_4_CLKA	TIMA_5_PWM5	-	-	-	-	-	-	-	-	EVNTP412	EVENTOUT	-	-
60	H12	-	-	-	PD13	-	EIRQ13	-	GPO	-	-	-	TIMA_4_PWM2/TIM A_4_CLKB	TIMA_5_PWM6	-	-	-	-	-	-	-	-	EVNTP413	EVENTOUT	-	-
61	H11	-	-	-	PD14	-	EIRQ14	-	GPO	-	-	-	TIMA_4_PWM3	TIMA_5_PWM7	-	-	-	-	-	-	-	-	EVNTP414	EVENTOUT	-	-
62	H10	-	-	-	PD15	-	EIRQ15	-	GPO	-	-	-	TIMA_4_PWM4	TIMA_5_PWM8	-	-	-	-	-	-	-	-	EVNTP415	EVENTOUT	-	-
63	E12	37	-	-	PC6	-	EIRQ6	-	GPO	-	-	-	TIMA_3_PWM1/TIM A_3_CLKA	TIMA_5_PWM8	-	QSPI_QSCK	KEYOUT3	SDIO1_D6	-	-	-	-	EVNTP306	EVENTOUT	-	Func_Grp2
64	E11	38	35	-	PC7	-	EIRQ7	-	GPO	-	TIM4_2_CLK	-	TIMA_3_PWM2/TIM A_3_CLKB	TIMA_5_PWM7	-	QSPI_QSSN	KEYOUT2	SDIO1_D7	I2S2_EXCK	-	-	-	EVNTP307	EVENTOUT	-	Func_Grp2
65	E10	39	36	-	PC8	-	EIRQ8	-	GPO	-	TIM4_2_OWH	-	TIMA_3_PWM3	TIMA_5_PWM6	-	USART3_CK	KEYOUT1	SDIO1_D0	I2S2_MCK	-	-	-	EVNTP308	EVENTOUT	-	Func_Grp2
66	D12	40	37	-	PC9	-	EIRQ9	-	GPO	MCO_2	TIM4_2_OWL	-	TIMA_3_PWM4	TIMA_5_PWM5	-	-	KEYOUT0	SDIO1_D1	-	-	-	-	EVNTP309	EVENTOUT	-	Func_Grp1
67	D11	41	38	29	PA8	-	EIRQ8/WKUP2_ 0	-	GPO	MCO_1	TIM4_1_OUH	TIM6_1_PWMA	TIMA_1_PWM1/TIM A_1_CLKA	-	-	USART1_CK	-	SDIO1_D1	USBFS_SOF	-	-	-	EVNTP108	EVENTOUT	-	Func_Grp1
68	D10	42	39	30	PA9	-	EIRQ9/WKUP2_ 1	-	GPO	-	TIM4_1_OVH	TIM6_2_PWMA	TIMA_1_PWM2/TIM A_1_CLKB	-	-	-	-	SDIO1_D2	USBFS_VBUS	-	-	-	EVNTP109	EVENTOUT	-	Func_Grp1
69	C12	43	40	31	PA10	-	EIRQ10/WKUP2 _2	-	GPO	-	TIM4_1_OWH	TIM6_3_PWMA	TIMA_1_PWM3	TIMA_5_TRIG	-	-	-	SDIO1_CD	USBFS_ID	-	-	-	EVNTP110	EVENTOUT	-	Func_Grp1

LQFP100	VFBGA100	LQFP64	QFN60	LQFP/QFN48	Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16~31	Func32~63
									GPO	other	TIM4	TIM6	TIMA	TIMA	EMB,TIMA	USART/SPI/ QSPI	KEY	SDIO	USBFS/I2S	-	-	-	EVNTPT	EVENTOUT	-	Communication Funcs
70	B12	44	41	32	PA11	-	EIRQ11/WKUP2_3	-	GPO	-	TIM4_1_CLK	-	TIMA_1_PWM4	-	EMB_IN1	-	-	SDIO2_CD	USBFS_DM	-	-	-	EVNTP111	EVENTOUT	-	Func_Grp1
71	A12	45	42	33	PA12	-	EIRQ12/WKUP3_0	-	GPO	-	TIM4_3_OWL	TIM6_TRIGA	TIMA_1_TRIG	TIMA_6_PWM1/TIMA_6_CLKA	-	-	-	SDIO2_WP	USBFS_DP	-	-	-	EVNTP112	EVENTOUT	-	Func_Grp1
72	A11	46	43	34	PA13	-	EIRQ13/WKUP3_1	JTMS_SWDIO	GPO	-	-	-	TIMA_2_PWM5	TIMA_6_PWM2/TIMA_6_CLKB	-	SPI2_SS1	-	SDIO2_D3	-	-	-	-	EVNTP113	EVENTOUT	-	Func_Grp1
73	C11	-	-	-	VCAP_2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
74	F11	47	44	35	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
75	G11	48	45	36	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
76	A10	49	46	37	PA14	-	EIRQ14/WKUP3_2	JTCK_SWCLK	GPO	-	-	-	TIMA_2_PWM6	TIMA_6_PWM3	TIMA_4_TRIG	SPI2_SS2	-	SDIO2_D2	I2S1_EXCK	-	-	-	EVNTP114	EVENTOUT	-	Func_Grp1
77	A9	50	47	38	PA15	-	EIRQ15/WKUP3_3	JTDI	GPO	-	-	-	TIMA_2_PWM1/TIMA_2_CLKA	TIMA_6_PWM4	TIMA_2_TRIG	SPI2_SS3	-	SDIO2_D1	I2S1_MCK	-	-	-	EVNTP115	EVENTOUT	-	Func_Grp1
78	B11	51	48	-	PC10	-	EIRQ10	-	GPO	-	TIM4_3_OUH	-	TIMA_2_PWM7	TIMA_5_PWM1/TIMA_5_CLKA	-	-	-	SDIO1_D2	-	-	-	-	EVNTP310	EVENTOUT	-	Func_Grp1
79	C10	52	49	-	PC11	-	EIRQ11	-	GPO	-	TIM4_3_OVH	-	TIMA_2_PWM8	TIMA_5_PWM2/TIMA_5_CLKB	-	-	-	SDIO1_D3	-	-	-	-	EVNTP311	EVENTOUT	-	Func_Grp1
80	B10	53	50	-	PC12	-	EIRQ12	-	GPO	-	TIM4_3_OWH	-	TIMA_4_TRIG	TIMA_5_PWM3	-	-	-	SDIO1_CK	-	-	-	-	EVNTP312	EVENTOUT	-	Func_Grp1
81	C9	-	-	-	PD0	-	EIRQ0	-	GPO	VCOUT123	-	-	-	TIMA_5_PWM4	-	-	-	-	-	-	-	-	EVNTP400	EVENTOUT	-	Func_Grp1
82	B9	-	-	-	PD1	-	EIRQ1	-	GPO	-	-	-	TIMA_3_TRIG	TIMA_6_PWM5	-	-	-	-	-	-	-	-	EVNTP401	EVENTOUT	-	Func_Grp1
83	C8	54	-	-	PD2	-	EIRQ2	-	GPO	-	-	-	TIMA_2_PWM4	TIMA_6_PWM6	-	-	-	SDIO1_CMD	-	-	-	-	EVNTP402	EVENTOUT	-	Func_Grp1
84	B8	-	-	-	PD3	-	EIRQ3	-	GPO	VCOUT1	-	-	-	TIMA_6_PWM7	-	-	-	-	-	-	-	-	EVNTP403	EVENTOUT	-	-
85	B7	-	-	-	PD4	-	EIRQ4	-	GPO	VCOUT2	-	-	-	TIMA_6_PWM8	-	-	-	-	-	-	-	-	EVNTP404	EVENTOUT	-	-
86	A6	-	-	-	PD5	-	EIRQ5	-	GPO	VCOUT3	-	-	-	-	-	-	-	-	-	-	-	-	EVNTP405	EVENTOUT	-	-
87	B6	-	-	-	PD6	-	EIRQ6	-	GPO	-	-	-	-	-	-	USART2_CK	-	-	-	-	-	-	EVNTP406	EVENTOUT	-	-
88	A5	-	-	-	PD7	-	EIRQ7	-	GPO	-	-	-	-	-	-	USART2_CK	-	-	-	-	-	-	EVNTP407	EVENTOUT	-	-
89	A8	55	51	39	PB3	-	EIRQ3/WKUP0_3	JTDO_TRACESWO	GPO	FCMREF	TIM4_3_CLK	-	TIMA_2_PWM2/TIMA_2_CLKB	TIMA_6_PWM5	-	-	-	SDIO2_D0	-	-	-	-	EVNTP203	EVENTOUT	-	Func_Grp2
90	A7	56	52	40	PB4	-	EIRQ4/WKUP1_0	NJTRST	GPO	-	TIM4_3_OWL	-	TIMA_3_PWM1/TIMA_3_CLKA	TIMA_6_PWM6	-	-	-	SDIO1_D0	-	-	-	-	EVNTP204	EVENTOUT	-	Func_Grp2
91	C5	57	53	41	PB5	-	EIRQ5/WKUP1_1	-	GPO	-	TIM4_3_OWH	-	TIMA_3_PWM2/TIMA_3_CLKB	TIMA_6_PWM7	-	-	-	SDIO1_D3	I2S4_EXCK	-	-	-	EVNTP205	EVENTOUT	-	Func_Grp2
92	B5	58	54	42	PB6	-	EIRQ6/WKUP1_2	-	GPO	ADTRG2	TIM4_3_OVL	-	TIMA_4_PWM1/TIMA_4_CLKA	TIMA_6_PWM8	-	-	-	SDIO2_CK	I2S4_MCK	-	-	-	EVNTP206	EVENTOUT	-	Func_Grp2
93	B4	59	55	43	PB7	-	EIRQ7/WKUP1_3	-	GPO	ADTRG1	TIM4_3_OVH	-	TIMA_4_PWM2/TIMA_4_CLKB	-	-	-	-	SDIO1_D0	-	-	-	-	EVNTP207	EVENTOUT	-	Func_Grp2
94	A4	60	56	44	PB11/MD	-	NMI	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVNTP211	-	-	-
95	A3	61	57	45	PB8	-	EIRQ8	-	GPO	-	TIM4_3_OUL	-	TIMA_4_PWM3	-	-	-	KEYOUT7	SDIO1_D4	USBFS_DRVVBUS	-	-	-	EVNTP208	EVENTOUT	-	Func_Grp2
96	B3	62	58	46	PB9	-	EIRQ9	-	GPO	-	TIM4_3_OUH	-	TIMA_4_PWM4	TIMA_6_TRIG	-	SPI2_SS1	KEYOUT6	SDIO1_D5	-	-	-	-	EVNTP209	EVENTOUT	-	Func_Grp2
97	C3	-	-	-	PE0	-	EIRQ0	-	GPO	MCO_1	-	-	TIMA_4_TRIG	-	-	SPI2_SS2	-	-	-	-	-	-	-	EVENTOUT	-	Func_Grp2
98	A2	-	-	-	PE1	-	EIRQ1	-	GPO	MCO_2	TIM4_3_CLK	-	-	-	-	SPI2_SS3	-	-	-	-	-	-	-	EVENTOUT	-	Func_Grp2
99	D3	63	59	47	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
100	C4	64	60	48	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	H3	-	-	-	NC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Note:

– In the above table, there are 64 pins that support the function selection of Func32~63. Func32~63 is mainly for serial communication functions (including USART, SPI, I2C, I2S, CAN), which are divided into two groups, Func_Grp1 and Func_Grp2. Please refer to Table 22 Table 2-2 for details.

Table 2-2 Func32~63 Table

	Func32	Func33	Func34	Func35	Func36	Func37	Func38	Func39	Func40	Func41	Func42	Func43	Func44	Func45	Func46	Func47
Func_Grp1	USART1_TX	USART1_RX	USART1_RTS	USART1_CTS	USART2_TX	USART2_RX	USART2_RTS	USART2_CTS	SPI1_MOSI	SPI1_MISO	SPI1_SS0	SPI1_SCK	SPI2_MOSI	SPI2_MISO	SPI2_SS0	SPI2_SCK
Func_Grp2	USART3_TX	USART3_RX	USART3_RTS	USART3_CTS	USART4_TX	USART4_RX	USART4_RTS	USART4_CTS	SPI3_MOSI	SPI3_MISO	SPI3_SS0	SPI3_SCK	SPI4_MOSI	SPI4_MISO	SPI4_SS0	SPI4_SCK

	Func48	Func49	Func50	Func51	Func52	Func53	Func54	Func55	Func56	Func57	Func58	Func59	Func60	Func61	Func62	Func63
Func_Grp1	I2C1_SDA	I2C1_SCL	I2C2_SDA	I2C2_SCL	I2S1_SD	I2S1_SDIN	I2S1_WS	I2S1_CK	I2S2_SD	I2S2_SDIN	I2S2_WS	I2S2_CK				
Func_Grp2	I2C3_SDA	I2C3_SCL	CAN_TxD	CAN_RxD	I2S3_SD	I2S3_SDIN	I2S3_WS	I2S3_CK	I2S4_SD	I2S4_SDIN	I2S4_WS	I2S4_CK				

Table 2-3 Port Configuration

Package	Port Group	Bits																Pin Count	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Total	
LQFP100 VFBGA100	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	83
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortE	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	
LQFP64	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	52
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	-	-	-	-	-	-	-	-	-	-	-	-	-	o	-	-	1	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	
QFN60	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	50
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	-	o	o	-	o	o	o	14	
	PortE	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	o	1	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	
LQFP48 QFN48	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	38
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	-	-	-	-	-	-	-	-	-	-	-	-	-	3	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		

Table 2-4 General Functional Specifications

Port		Pull-up	Open-Drain Output	Driving Capacity	5V Withstand Voltage	Remark
PortA	PA0~PA10 PA13~PA15	Support	Support	Low Medium High	Support *	
	PA11, PA12	Support	Support	Low Medium High	not support	
PortB	PB0~PB10, PB12~PB15	Support	Support	Low Medium High	Support *	
	PB11	Support	-	-	Support	input only
PortC	PC0~PC15	Support	Support	Low Medium High	Support *	
PortD	PD0~PD15	Support	Support	Low Medium High	Support	
PortE	PE0~PE15	Support	Support	Low Medium High	Support	
PortH	PH0~PH2	Support	Support	Low Medium High	Support	

Note:

– Input voltage must not be higher than VREFH/AVCC when used as an analog function.

2.3 Pin Function Description

Table 2-5 Pin Function Description

Categories	Functional name	I/O	Note
Power	VCC	I	Power supply
	VSS	I	Source ground
	VCAP_1~2	IO	Core voltage
	AVCC	I	Analog power
	AVSS	I	Analog power ground
	VREFH	I	Analog reference voltage
	VREFL	I	Analog reference voltage
System	NRST	I	Reset pin, low effective
	MD	I	mode pin
PVD	PVD2EXINP	I	PVD2 external input comparison voltage
Clock	XTAL_IN	IO	External high-speed (4-25MHz) oscillator interface
	XTAL_EXT/XTAL_OUT	IO	XTAL_EXT external clock input
	XTAL32_IN	I	External low-speed (32K) oscillator interface
	XTAL32_OUT	O	
	MCO_1~2	O	Internal clock output
GPIO	GPIOxy (x= A~E,H, y=0~15)	IO	General input/output
EVENTOUT	EVENTOUT	O	Cortex-M4 CPU event output
EIRQ	EIRQx (x=0~15)	I	Shielded external interrupt
	WKUPx_y (x,y=0~3)	I	PowerDown mode external wake-up input
	NMI	I	Non-shielded external interrupt
Event Port	EVNTPxy (x=1~4, y=0~15)	IO	Event port input and output functions
Key	KEYOUTx(x=0~7)	O	KEYSCAN scan output signal
JTAG/SWD	JTCK_SWCLK	I	Online debugging interface
	JTMS_SWDIO	IO	
	JTDO_TRACESWO	O	
	JTDI	I	
	NJTRST	I	
TRACE	TRACECK	O	Trace debug sync clock output
	TRACED0~3	O	Trace debug data output
FCM	FCMREF	I	External reference clock input for clock frequency measurement
RTC	RTCOUT	O	1 Hz clock output
Timer4 (x=1~3)	TIM4_x_CLK	I	Counting clock port input
	TIM4_x_OUH	IO	PWM port U-phase output
	TIM4_x_OUL	IO	PWM port U-phase output
	TIM4_x_OVH	IO	PWM port V-phase output

Categories	Functional name	I/O	Note
	TIM4_x_OVL	IO	PWM port V-phase output
	TIM4_x_OWH	IO	PWM port W-phase output
	TIM4_x_OWL	IO	PWM port W-phase output
Timer6 (x=1~3)	TIM6_TRIGA	I	External event trigger A input
	TIM6_TRIGB	I	External event trigger B input
	TIM6_x_PWMA	IO	External Event Trigger Input or PWM Port Output
	TIM6_x_PWMB	IO	External Event Trigger Input or PWM Port Output
TimerA (x=1~6)	TIMA_x_TRIG	I	External event trigger input
	TIMA_x_PWM1/TIMA_x_CLKA	IO	External event trigger input or PWM port output or count clock port input
	TIMA_x_PWM2/TIMA_x_CLKB	IO	External event trigger input or PWM port output or count clock port input
	TIMA_x_PWMy (y=3~8)	IO	External Event Trigger Input or PWM Port Output
EMB	EMB_INx (x=1~4)	I	Groupx (x=1~4) port input control signal
USARTx (x=1~4)	USARTx_TX	IO	Send data
	USARTx_RX	IO	Receiving data
	USARTx_CK	IO	Communication clock
	USARTx RTS	O	Request to send a signal
	USARTx CTS	I	clear send signal
SPIx (x=1~4)	SPIx_MISO	IO	Primary input/secondary output data transfer pin
	SPIx_MOSI	IO	Primary output/slave input data transfer pin
	SPIx_SCK	IO	Transmission clock
	SPIx_SS0	IO	Select input/output pin from machine
	SPIx_SS1~3	O	Slave select output pin
QSPI	QSPI_QSIO0~3	IO	Data line
	QSPI_QSCK	O	Clock output
	QSPI_QSSN	O	Slave selection
I2Cx (x=1~3)	I2Cx_SCL	IO	Clock line
	I2Cx_SDA	IO	Data line
I2Sx (x=1~4)	I2Sx_SD	IO	Serial data
	I2Sx_SDIN	I	Full duplex serial data input
	I2Sx_WS	IO	word selection
	I2Sx_CK	IO	Serial clock
	I2Sx_EXCK	I	External timer
	I2Sx_MCK	O	master clock
CAN	CAN_TxD	O	Send data
	CAN_RxD	I	Receiving data
SDIOx	SDIOx_Dy (y=0~7)	IO	SD data signal
	SDIOx_CK	O	SD clock output signal
	SDIOx_CMD	IO	SD command and reply signal

Categories	Functional name	I/O	Note
	SDIOx_CD	I	SD card identification status signal
	SDIOx_WP	I	SD card write protection status signal
USBFS	USBFS_DM	IO	USBFS on-chip full-speed PHY D- signal
	USBFS_DP	IO	USBFS on-chip full-speed PHY D+ signal
	USBFS_VBUS	I	USBFS VBUS signal
	USBFS_ID	I	USBFS ID signal
	USBFS_SOF	O	USBFS SOF pulse output signal
	USBFS_DRVVBUS	O	USBFS VBUS driver permission signal
CMPx (x=1~3)	VCOUT1	O	Analog comparison channel 1 result output
	VCOUT2	O	Analog comparison channel 2 result output
	VCOUT3	O	Analog comparison channel 3 result output
	VCOUT123	O	Analog comparison channel 1~3 result OR output
	CMPx_INPy	I	Analog comparator channel x positive terminal voltage y input
	CMPx_INMy	I	Analog comparator channel x negative terminal voltage y input
ADC	ADTRG1	I	ADC1 AD conversion external start source
	ADTRG2	I	ADC2 AD conversion external start source
	ADC1_INx (x=0~3,12~15)	I	ADC1 external analog input port
	ADC12_INx (x=4~11)	I	ADC1 and ADC2 share the external analog input port
	PGAVSS	I	PGA Ground input

2.4 Pin Instruction

Table 2-6 Pin Use Instructions

Pin Name	Usage Notes
VCC	Power source, 1.8 V ~ 3.6 V voltage, and close to VSS pin to decouple capacitor (refer to Electrical Characteristics (ECs))
VSS	Source ground, connected to 0V
VCAP_1~2	Core voltage, connected to VSS pin to stabilize core voltage (refer to Electrical Characteristics (ECs))
AVCC	Analog power supply, supplying power to analog modules, connected to the same voltage as VCC (refer toElectrical Characteristics (ECs)) When not using the analog module, please short it with VCC
AVSS/VREFL	Analog power ground/reference voltage, connected to the same voltage as AVSS (refer toElectrical Characteristics (ECs)) When not using the analog module, please short it with VSS
VREFH	Analog reference voltage of ADC1 and ADC2, connected to a voltage not higher than AVCC When not using ADC, please short it with AVCC
PB11/MD	Mode input, fixed to input state. When the reset pin (NRST) is released (from low to high), the pin must be fixed at high level. Recommended resistance (4.7 KΩ) to VCC (pull-up)
NRST	Reset pin, low effective. Resistance to VCC when not in use (pull-up)
Pxy, x=A~E, H, y=0~15	General pin. When used as an input, the input voltage on 5V-tolerant pins must not exceed 5 V. When the input voltage exceeds VCC, the internal pull-up is disabled. For pins that are not 5V-tolerant, the input voltage must not exceed VCC. When used as an analog input, the analog voltage should not exceed VREFH/AVCC Hang out when not in use or connect to VCC (pull-up)/VSS (pull-down)

3 Electrical Characteristics (ECs)

3.1 Parameter Conditions

All voltages are VSS-based unless otherwise specified.

3.1.1 Minimum and Maximum

Unless otherwise specified, the minimum and maximum values of all devices are guaranteed by design or performance tests at worst ambient temperature, supply voltage and clock frequency.

3.1.2 Typical Value

Unless otherwise specified, typical data are obtained by design or characteristic test analysis at T_A = 25 °C and VCC = 3.3 V.

3.1.3 Typical Curve

Unless otherwise specified, all typical curves are not tested for design reference only.

3.1.4 Load Capacitance

Figure 3-1 (Left) shows the load conditions used to measure the pin parameters.

3.1.5 Pin Input Voltage

Figure 3-1 (Right) shows how to measure the input voltage at the device pins.

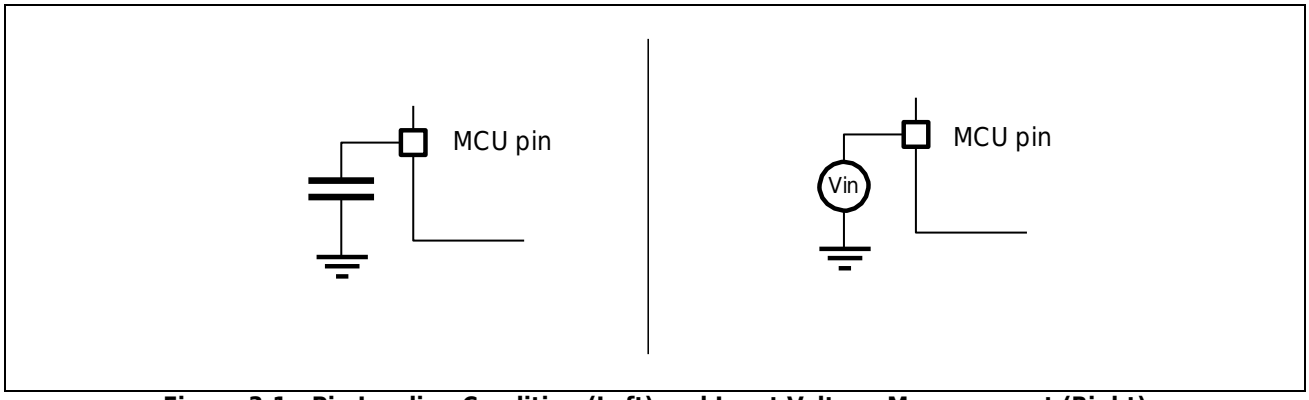


Figure 3-1 Pin Loading Condition (Left) and Input Voltage Measurement (Right)

3.1.6 Power Supply Scheme

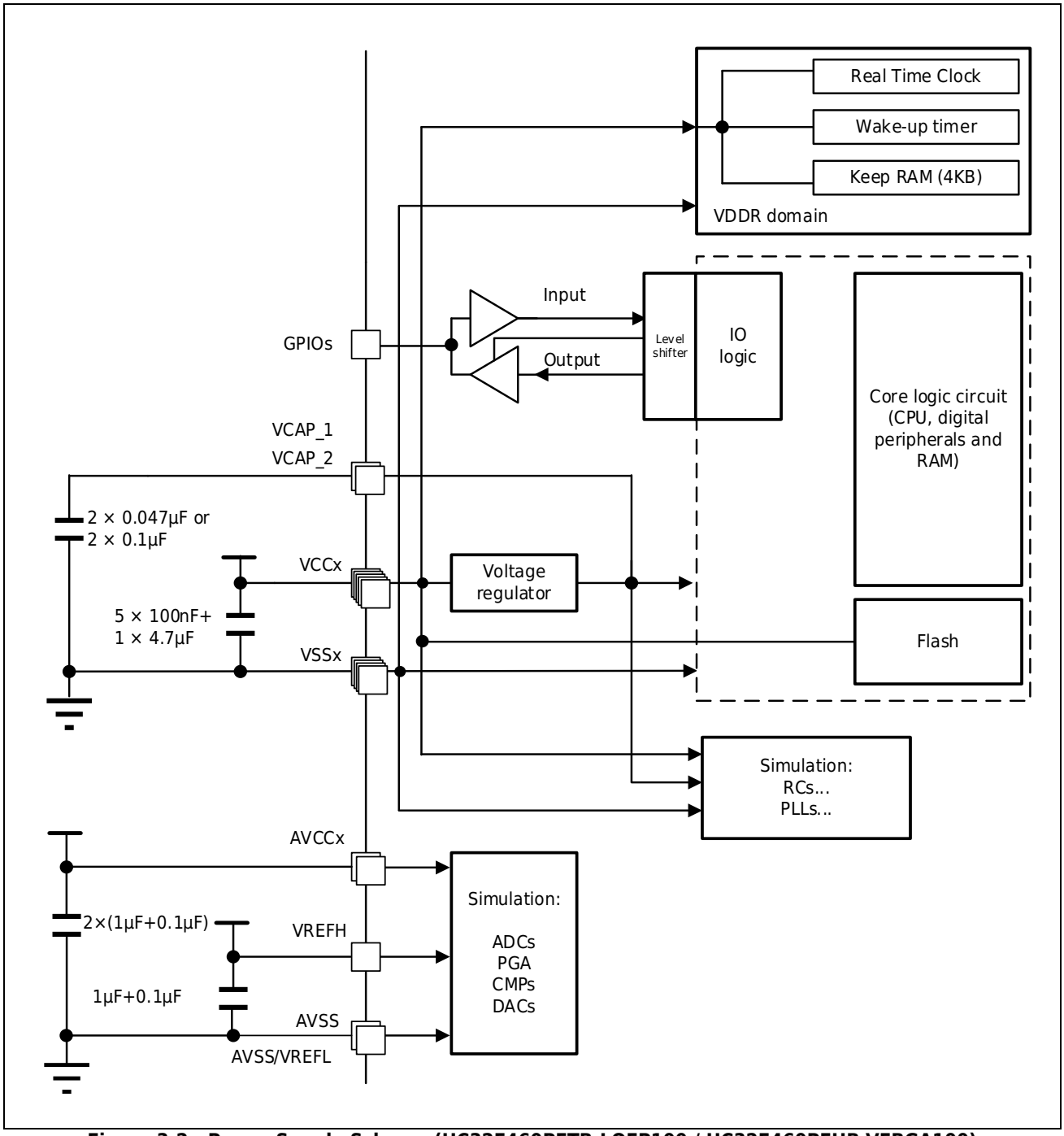


Figure 3-2 Power Supply Scheme (HC32F460PETB-LQFP100 / HC32F460PEHB-VFBGA100)

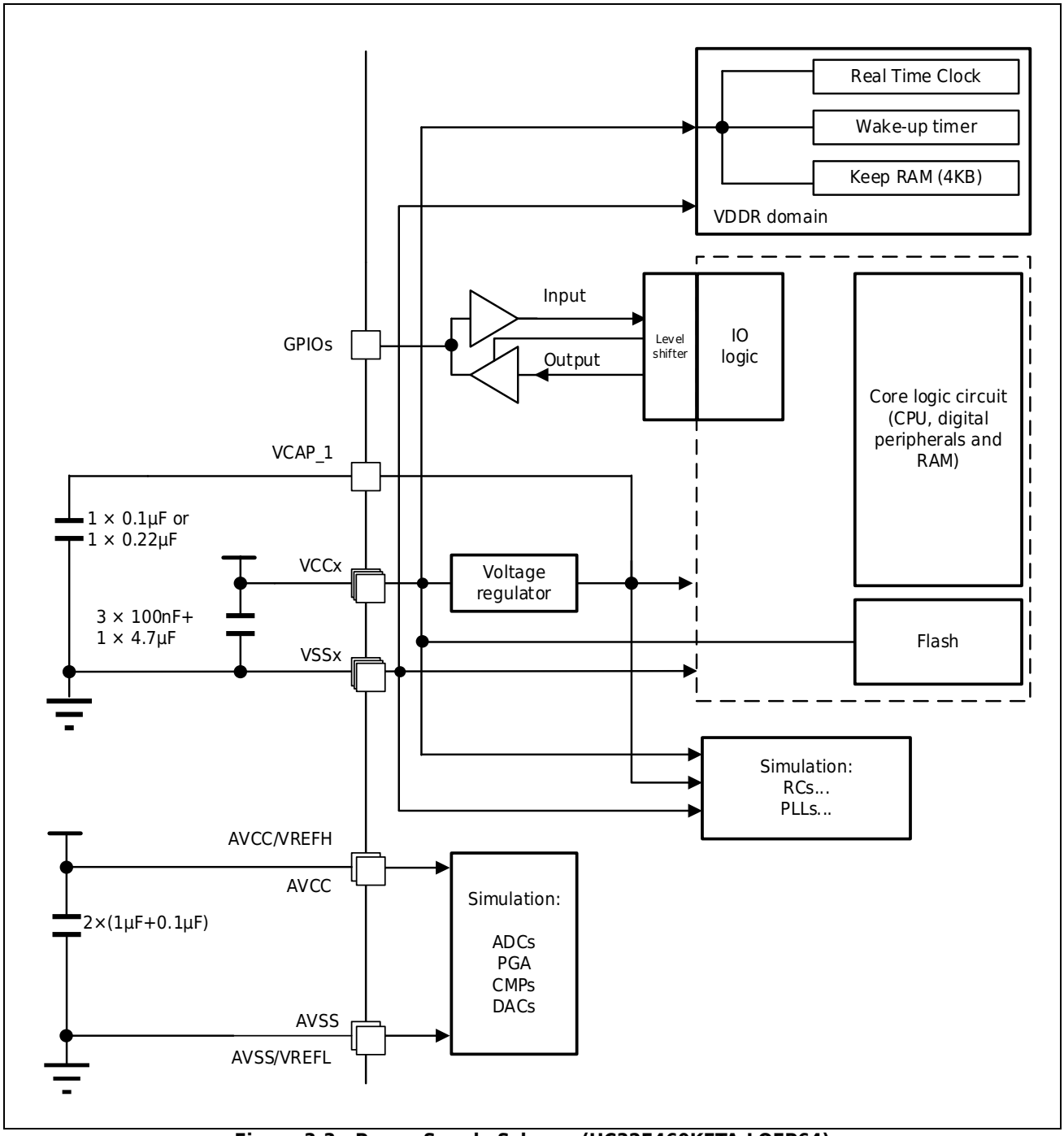


Figure 3-3 Power Supply Scheme (HC32F460KETA-LQFP64)

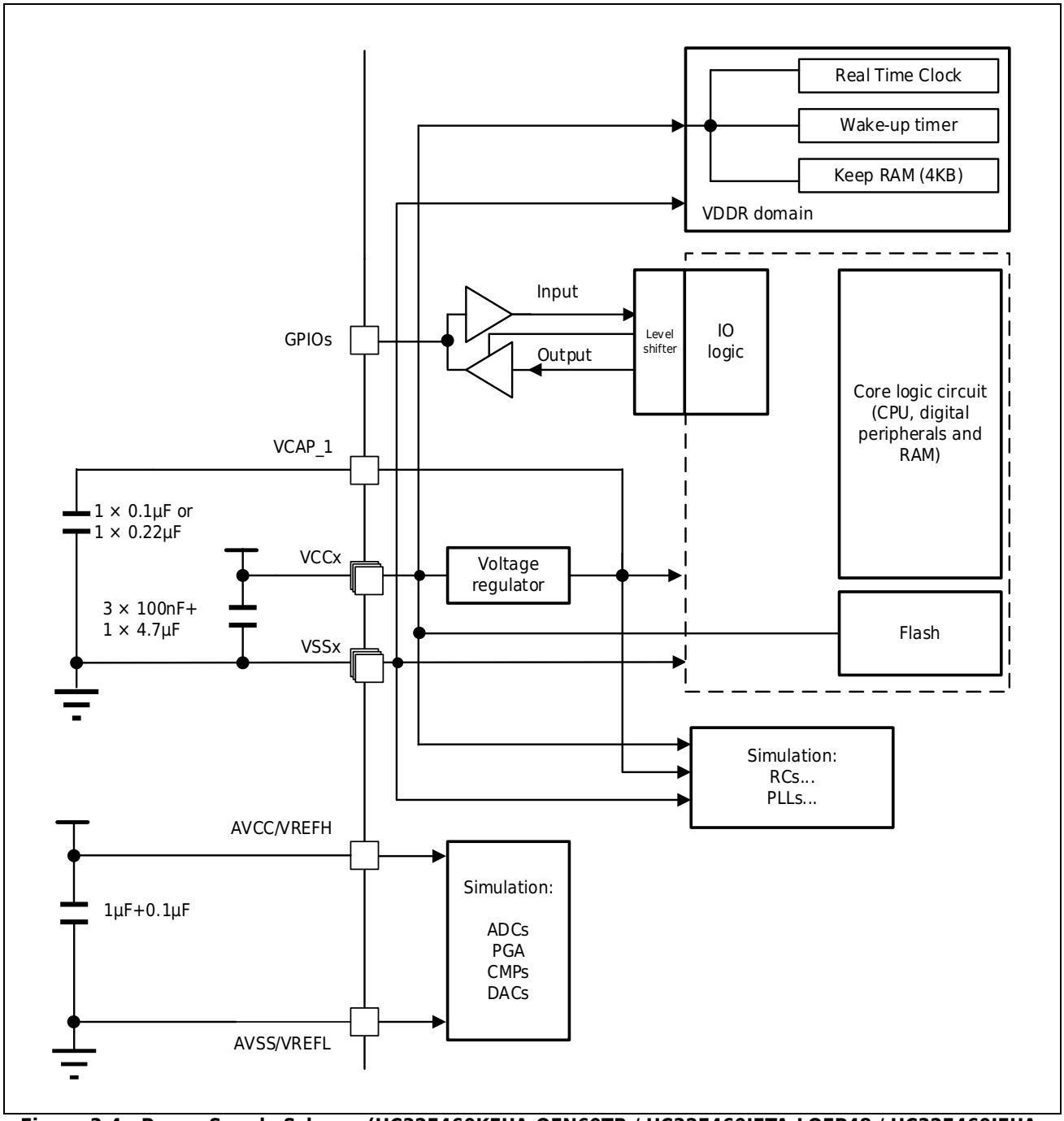


Figure 3-4 Power Supply Scheme (HC32F460KEUA-QFN60TR / HC32F460JETA-LQFP48 / HC32F460JEUA-QFN48TR)

1. A 4.7µF ceramic capacitor must be connected to one of the VCC pins.
2. AVSS=VSS.
3. Each supply pair (e.g., VCC/VSS, AVCC/AVSS...) must be decoupled with filter ceramic capacitors as described above. These capacitors must be placed as close as possible to or below the appropriate pins on the underside of the PCB to ensure proper device operation. Filtering capacitors are not recommended to reduce PCB size or cost. This may result in abnormal operation of the device.
4. The capacitors used by the VCAP_1/VCAP_2 pins of the chip are as follows: 1) For chips with

both VCAP_1 and VCAP_2 pins, each pin can use a 0.047 μF or 0.1 μF capacitor (the total capacity is 0.094 μF or 0.2 μF). 2) Chips with only VCAP_1 pins can use 0.1 μF or 0.22 μF capacitors. When waking up from power-down mode, VCAP_1/VCAP_2 needs to be charged during the core voltage establishment process. On the one hand, the smaller VCAP_1/VCAP_2 total capacity can shorten the charging time and bring fast response capability to the application; on the other hand, the larger VCAP_1/VCAP_2 total capacity will prolong the charging time, but also provide stronger electromagnetic compatibility (EMC). Users can choose a larger or smaller capacitance value according to the requirements of electromagnetic compatibility and system response speed. The total capacity of VCAP_1/VCAP_2 of the chip must match the assignment of the PWC_PWRC3.PDTS bit. When the total capacity of VCAP_1/VCAP_2 is 0.2 μF or 0.22 μF, it is necessary to ensure that the PWC_PWRC3.PDTS bit is cleared before entering power-down mode. When the total capacity of VCAP_1/VCAP_2 is 0.094 μF or 0.1 μF, it is necessary to ensure that the PWC_PWRC3.PDTS bit is set before entering power-down mode.

5. The stability of the main voltage regulator is achieved by connecting an external capacitor to the VCAP_1 (or VCAP_1/VCAP_2) pin, and the value of the capacitor CEXT is determined according to the stability requirements of the system. The capacitance value CEXT and ESR requirements are as follows:

Table 3-1 VCAP_1/VCAP_2 Working Conditions

Symbol	Parameter	Conditions
C_{EXT}	Capacitance value of external capacitance	0.047μF / 0.1μF / 0.22μF
ESR	Equivalent series resistance ESR of external capacitor	< 0.3Ω

3.1.7 Current Consumption Measurement

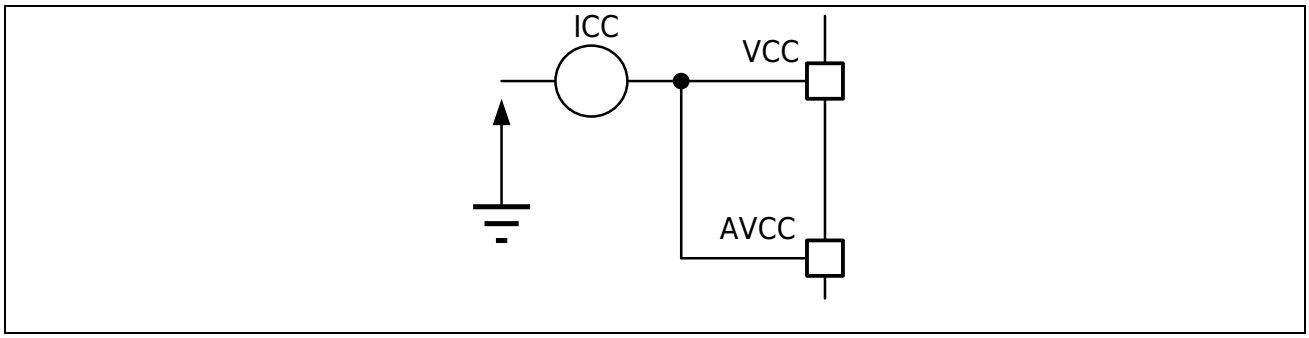


Figure 3-5 Current Consumption Measurement Solution

3.2 Absolute Maximum Ratings

Permanent damage to the device may result if loads exceeding the absolute maximum ratings listed in Table 3-2 Voltage Characteristics, Table 3-3 Voltage Characteristics and Table 3-4 Thermal Characteristics are applied to the device. These values are just rated stresses and do not mean that the device works properly under these conditions. Long-term operation may affect the reliability.

Table 3-2 Voltage Characteristics

Symbol	Item	Minimum Value	Maximum Value	Unit
V_{CC}-V_{SS}	External main supply voltage (including AVCC, VCC) (1)	-0.3	4.0	V
V_{IN}	Input voltage on 5V tolerant pin (2)	V_{SS}–0.3	VCC+4.0 (Maximum 5.8V)	
	Input voltage on PA11/USBFS_DM and PA12/USBFS_DP pins	V_{SS}–0.3	4.0	
$V_{ESD(HBM)}$	Electrostatic Discharge Voltage (Human Body Model)	Please refer to 3.3.5 [Electrical Sensitivity]		-

1. All main power (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to an external power supply, within the limits allowed.
2. The maximum value of V_{IN} must always be followed. For information on the maximum allowable current values, See Table 3-3.

Table 3-3 Voltage Characteristics

Symbol	Item	Maximum value	Unit
ΣI_{VCC}	Total current flowing into all VCC_X supply lines (source current) (1)	240	mA
ΣI_{VSS}	Total current flowing out of all VSS_X ground wires (sinking current) (1)	-240	
I_{VCC}	Maximum current flowing into each VCC_X power line (source current) (1)	100	
I_{VSS}	Maximum current out of each VSS_X ground wire (sinking current) (1)	-100	
I_{IO}	Arbitrary I/O and control pin output current	40	
	Output pull current of any I/O and control pin	-40	
ΣI_{IO}	Total output sink current on all I/O and control pins	120	
	Total output source current on all I/O and control pins	-120	

1. All main power (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to an external power supply, within the limits allowed.

Table 3-4 Thermal Characteristics

Symbol	Item	Numerical Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	125	°C

3.3 Operating Conditions

3.3.1 General Operating Conditions

Table 3-5 General Operating Conditions

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{HCLK}	Internal AHB clock frequency	Super speed mode [1] PWRC2.DVS=00 PWRC2.DDAS=1111	0	-	200	MHz
		High speed mode [1] PWRC2.DVS=11 PWRC2.DDAS=1111	0	-	168	
		Super low speed mode PWRC2.DVS=10 PWRC2.DDAS=1000	0	-	8	
V_{CC}	Standard operating voltage	-	1.8	-	3.6	V
V_{AVCC}(2)	Analog working voltage	-	1.8	-	3.6	
V_{IN}	Input voltage on 5V tolerant pin(3)	2 V ≤ VCC ≤ 3.6 V	–0.3	-	5.5	
		VCC ≤ 2 V	–0.3	-	5.2	
	PA11/USBFS_DM PA12/USBFS_DP Input voltage on pin		–0.3	-	V_{CC}+0.3	
T_J	Junction temperature range		-40	-	125	°C

1. According to comprehensive evaluation, it is not tested in production.
2. If the VREFH pin is present, the following condition must be considered: V_{AVCC} - V_{REFH} < 1.2 V.
3. To keep the voltage above VCC+0.3, the internal pull-up/pull-down resistors must be disabled.
4. The voltage can be applied to the 5 V-tolerant pins only after the device's power supplies (VCC, AVCC) have become stable.
5. It is prohibited to directly connect such pins to the power/ground of a non-own chip. It is recommended to use a resistor with a value of 1KΩ or higher for pulling up to the power supply or pulling down to the ground.

3.3.2 Operating Conditions in Case of Power-on/Power-off

TA obeys general operating conditions.

Table 3-6 Operating Conditions in Case of Power-on/Power-off

Symbol	Parameter	Minimum Value	Maximum Value	Unit
t_{VCC}	VCC rising time rate	20	20000	μs/V
	VCC Descending Time Rate	20	20000	

3.3.3 Reset and Power Control Module Characteristics

Table 3-7 Reset and Power Control Block Features

Symbol	Parameter	Conditions		Minimum Value	Typical Value	Maximum Value	Unit
V_{BOR}	Monitoring Voltage of BOR	Super speed mode	ICG1.BOR_LEV [1:0] =00	1.88	1.99	2.09	V
			ICG1.BOR_LEV [1:0] =01	1.99	2.09	2.20	V
			ICG1.BOR_LEV [1:0] =10	2.09	2.20	2.30	V
			ICG1.BOR_LEV [1:0] =11	2.30	2.40	2.51	V
		High speed mode Super low speed mode	ICG1.BOR_LEV [1:0] =00	1.80	1.90	2.00	V
			ICG1.BOR_LEV [1:0] =01	1.90	2.00	2.10	V
			ICG1.BOR_LEV [1:0] =10	2.00	2.10	2.20	V
			ICG1.BOR_LEV [1:0] =11	2.20	2.30	2.40	V
V_{PVD1}	PVD1 Monitoring Voltage[3]	Super speed mode	PVD1LVL [2:0] =000	1.99	2.09	2.20	V
			PVD1LVL [2:0] =001	2.09	2.20	2.30	V
			PVD1LVL [2:0] =010	2.30	2.40	2.51	V
			PVD1LVL [2:0] =011	2.54	2.67	2.79	V
			PVD1LVL [2:0] =100	2.65	2.77	2.90	V
			PVD1LVL [2:0] =101	2.75	2.88	3.00	V
			PVD1LVL [2:0] =110	2.85	2.98	3.11	V
			PVD1LVL [2:0] =111	2.96	3.08	3.21	V
		High speed mode Super low speed mode	PVD1LVL [2:0] =000	1.90	2.00	2.10	V
			PVD1LVL [2:0] =001	2.00	2.10	2.20	V
			PVD1LVL [2:0] =010	2.20	2.30	2.40	V
			PVD1LVL [2:0] =011	2.43	2.55	2.67	V
			PVD1LVL [2:0] =100	2.53	2.65	2.77	V
			PVD1LVL [2:0] =101	2.63	2.75	2.87	V
			PVD1LVL [2:0] =110	2.73	2.85	2.97	V
			PVD1LVL [2:0] =111	2.83	2.95	3.07	V
V_{PVD2}	PVD2 Monitoring Voltage[3]	Super speed mode	PVD2LVL [2:0] =000	2.09	2.20	2.30	V
			PVD2LVL [2:0] =001	2.30	2.40	2.51	V
			PVD2LVL [2:0] =010	2.54	2.67	2.79	V
			PVD2LVL [2:0] =011	2.65	2.77	2.90	V
			PVD2LVL [2:0] =100	2.75	2.88	3.00	V
			PVD2LVL [2:0] =101	2.85	2.98	3.11	V
			PVD2LVL [2:0] =110	2.96	3.08	3.21	V
			PVD2LVL [2:0] =111[2]	1.05	1.15	1.25	V
		High speed mode Super low speed mode	PVD2LVL [2:0] =000	2.00	2.10	2.20	V
			PVD2LVL [2:0] =001	2.20	2.30	2.40	V
			PVD2LVL [2:0] =010	2.43	2.55	2.67	V

Symbol	Parameter	Conditions		Minimum Value	Typical Value	Maximum Value	Unit
			PVD2LVL [2:0] =011	2.53	2.65	2.77	V
			PVD2LVL [2:0] =100	2.63	2.75	2.87	V
			PVD2LVL [2:0] =101	2.73	2.85	2.97	V
			PVD2LVL [2:0] =110 (1)	2.83	2.95	3.07	V
			PVD2LVL [2:0] =111(2)	1.00	1.10	1.20	V
$V_{pvd}hyst$	Hysteresis of PVD1,2 (3)			-	100	-	mV
V_{POR}(1)	Power-on/power-off reset threshold	Rising edge VPOR		1.60	1.68	1.76	V
		Descending edge VPDR		1.56	1.64	1.72	V
$V_{POR}hyst$	POR hysteresis			-	40	-	mV
I_{RUSH}	Surge current when the voltage regulator is powered on (POR or awakens from standby)			-	100	150	mA
T_{NRST}	NRST reset minimum width			500	-	-	ns
T_{IPVD1}	PVD1 reset release time			300	380	460	μs
T_{IPVD2}	PVD2 reset release time			300	380	460	μs
T_{INRST}	NRST reset release time			25	35	50	μs
T_{RIPT}	Internal reset time			140	160	200	μs
T_{RSTBOR}	BOR reset release time			440	520	610	μs
T_{RSTPOR}	Power-on reset release time			-	2500	3000	μs

1. Guarantee of mass production test.
2. When PVD2LVDL [2:0] = 111, the comparison voltage is the external input comparison voltage of PVD2EXINP pin.
3. The PVD1 monitoring voltage is the monitoring voltage when the VCC voltage drops; when PVD2LVL [2:0] is set to 111, the PVD2 monitoring voltage is the monitoring voltage when the PVDEXINP voltage drops, and when PVD2LVD [2:0] is set to a value other than 111 The PVD2 monitoring voltage is the monitoring voltage when the VCC voltage drops.
4. The hysteresis of PVD1,2 is the difference between the monitored voltage when VCC is rising and the monitored voltage when VCC is falling.
   PVD1 monitoring voltage when VCC rises = =Vpvd1+Vpvdhyst.
   PVD2 monitoring voltage when VCC rises = Vpvd2+Vpvdhyst.

3.3.4 Supply Current Characteristics

The current consumption is affected by several parameters and factors, including operating voltage, ambient temperature, I/O pin load, device software configuration, operating frequency, I/O pin switch rate, program position in memory and running code.

The method for measuring the current consumption is described in Figure 3-5 Current Consumption Measurement Solution. The measured values of current consumption in various operating modes described in this section are obtained under laboratory conditions through a set of test codes running on FLASH.

The specific conditions are as follows:

1) All I/O pins are in input mode, with static values (no load) on VCC or VSS.
2) The clock frequency selects the ultra-high-speed mode f_{HCLK}=200MHz, the high-speed mode f_{HCLK}=168MHz/120MHz/24MHz and the ultra-low-speed mode f_{HCLK}=8MHz/1MHz.
3) The power consumption mode is divided into: normal working mode ICC_RUN, sleep mode ICC_SLEEP, stop mode ICC_STP, power down mode ICC_PD and Dhrystone working mode ICC_DHRYSTONE.
4) For peripheral clock ON/OFF, please refer to specific current test items.
5) The PLL is turned on in super high-speed mode f_{HCLK}=200MHz and high-speed mode f_{HCLK}=168MHz/120MHz.

Table 3-8 SuperSpeed Mode Current Consumption

Pattern	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
Super speed mode	f_{HCLK}= 200 MHz	ICC_RUN	While (1), full-module clock OFF	-40	-	16	-	mA
			While (1), full module clock ON	-40	-	29	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	17	-	mA
			CACHE ON	-40	-	19	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	11	-	mA
			Full module clock ON	-40	-	24	-	mA
		ICC_RUN	While (1), full-module clock OFF	25	-	16	-	mA
			While (1), full module clock ON	25	-	29	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	17	-	mA
			CACHE ON	25	-	19	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	11	-	mA
			Full module clock ON	25	-	24	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	22	mA
			While (1), full	85	-	-	35	mA

Pattern	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
			module clock ON					
		ICC_DHRYSTONE	CACHE OFF	85	-	-	22	mA
			CACHE ON	85	-	-	25	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	17	mA
			Full module clock ON	85	-	-	30	mA
		ICC_RUN	While (1), full-module clock OFF	105	-	-	25	mA
			While (1), full module clock ON	105	-	-	39	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	24	mA
			CACHE ON	105	-	-	29	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	21	mA
			Full module clock ON	105	-	-	34	mA

1. Typ voltage condition V_{CC}=3.3V.
2. Max Voltage Condition V_{CC}=1.8~3.6V.

Table 3-9 High Speed Mode Current Consumption1

Pattern	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
High speed mode	f_{HCLK}= 168MHz	ICC_RUN	While (1), full-module clock OFF	-40	-	13	-	mA
			While (1), full module clock ON	-40	-	23	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	14	-	mA
			CACHE ON	-40	-	15	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	9	-	mA
			Full module clock ON	-40	-	19	-	mA
		ICC_RUN	While (1), full-module clock OFF	25	-	13	-	mA
			While (1), full module clock ON	25	-	23	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	14	-	mA
			CACHE ON	25	-	15	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	9	-	mA
			Full module clock ON	25	-	19	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	18	mA
			While (1), full module clock ON	85	-	-	28	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	18	mA
			CACHE ON	85	-	-	20	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	14	mA
			Full module clock ON	85	-	-	24	mA
		ICC_RUN	While (1), full-module clock OFF	105	-	-	20	mA
			While (1), full module clock ON	105	-	-	31	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	19	mA
			CACHE ON	105	-	-	23	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	17	mA
			Full module clock ON	105	-	-	27	mA

1. Typ voltage condition V_{CC}=3.3V.
2. Max Voltage Condition V_{CC}=1.8~3.6V.

Table 3-10 High Speed Mode Current Consumption2

Pattern	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
High speed mode	f_{HCLK}= 120MHz	ICC_RUN	While (1), full-module clock OFF	-40	-	9.5	-	mA
			While (1), full module clock ON	-40	-	16.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	10	-	mA
			CACHE ON	-40	-	11.5	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	7	-	mA
			Full module clock ON	-40	-	14.5	-	mA
		ICC_RUN	While (1), full-module clock OFF	25	-	9.5	-	mA
			While (1), full module clock ON	25	-	16.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	10	-	mA
			CACHE ON	25	-	11.5	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	7	-	mA
			Full module clock ON	25	-	14.5	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	14	mA
			While (1), full module clock ON	85	-	-	22	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	14	mA
			CACHE ON	85	-	-	17	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	12	mA
			Full module clock ON	85	-	-	20	mA
		ICC_RUN	While (1), full-module clock OFF	105	-	-	16	mA
			While (1), full module clock ON	105	-	-	25	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	15	mA
			CACHE ON	105	-	-	19	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	15	mA
			Full module clock ON	105	-	-	22	mA

1. Typ voltage condition V_{CC}=3.3V.
2. Max Voltage Condition V_{CC}=1.8~3.6V.

Table 3-11 High Speed Mode Current Consumption3

Pattern	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
High speed mode	f_{HCLK}= 24MHz	ICC_RUN	While (1), full-module clock OFF	-40	-	3	-	mA
			While (1), full module clock ON	-40	-	6	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	3.5	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	2	-	mA
			Full module clock ON	-40	-	5.5	-	mA
		ICC_RUN	While (1), full-module clock OFF	25	-	3	-	mA
			While (1), full module clock ON	25	-	6	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	3.5	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	2	-	mA
			Full module clock ON	25	-	5.5	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	8	mA
			While (1), full module clock ON	85	-	-	12	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	7	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	8	mA
			Full module clock ON	85	-	-	11	mA
		ICC_RUN	While (1), full-module clock OFF	105	-	-	10	mA
			While (1), full module clock ON	105	-	-	14	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	8	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	10	mA
			Full module clock ON	105	-	-	14	mA

1. Typ voltage condition V_{CC}=3.3V.
2. Max Voltage Condition V_{CC}=1.8~3.6V.

Table 3-12 Ultra Low Speed Mode Current Consumption1

Pattern	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
Super low speed mode	f_{HCLK}= 8MHz	ICC_RUN	While (1), full-module clock OFF	-40	-	1	-	mA
			While (1), full module clock ON	-40	-	3.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	1.5	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	1.2	-	mA
			Full module clock ON	-40	-	3.2	-	mA
		ICC_RUN	While (1), full-module clock OFF	25	-	1	-	mA
			While (1), full module clock ON	25	-	3.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	1.5	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	1.2	-	mA
			Full module clock ON	25	-	3.2	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	4	mA
			While (1), full module clock ON	85	-	-	6	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	4	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	3.5	mA
			Full module clock ON	85	-	-	6	mA
		ICC_RUN	While (1), full-module clock OFF	105	-	-	6	mA
			While (1), full module clock ON	105	-	-	7	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	4.5	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	4	mA
			Full module clock ON	105	-	-	6.5	mA

1. Typ voltage condition V_{CC}=3.3V.
2. Max Voltage Condition V_{CC}=1.8~3.6V.

Table 3-13 Ultra Low Speed Mode Current Consumption2

Pattern	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
Ultra low speed Pattern	f_{HCLK}= 1MHz	ICC_RUN	While (1), full-module clock OFF	-40	-	0.7	-	mA
			While (1), full module clock ON	-40	-	2.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	0.9	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	0.9	-	mA
			Full module clock ON	-40	-	2.4	-	mA
		ICC_RUN	While (1), full-module clock OFF	25	-	0.7	-	mA
			While (1), full module clock ON	25	-	2.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	0.9	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	0.9	-	mA
			Full module clock ON	25	-	2.4	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	4	mA
			While (1), full module clock ON	85	-	-	5	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	3.5	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	3.5	mA
			Full module clock ON	85	-	-	5	mA
		ICC_RUN	While (1), full-module clock OFF	105	-	-	5	mA
			While (1), full module clock ON	105	-	-	5.5	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	4	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	5	mA
			Full module clock ON	105	-	-	5.5	mA

1. Typ voltage condition V_{CC}=3.3V.
2. Max Voltage Condition V_{CC}=1.8~3.6V.

Table 3-14 Low Power Mode Current Consumption

Pattern	Parameter	Symbol	Condition (VCC=3.3V)	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
Stop Mode	-	ICC_STP	PWC_PWRC1.STPDAS=00	-40	-	160	-	μA
			PWC_PWRC1.STPDAS=11	-40	-	30	-	μA
			PWC_PWRC1.STPDAS=00	25	-	220	-	μA
			PWC_PWRC1.STPDAS=11	25	-	80	-	μA
			PWC_PWRC1.STPDAS=00	85	-	-	3600	μA
			PWC_PWRC1.STPDAS=11	85	-	-	3400	μA
			PWC_PWRC1.STPDAS=00	105	-	-	4800	μA
			PWC_PWRC1.STPDAS=11(3)	105	-	-	4600	μA
Power Down Mode	-	ICC_PD	Power down mode 1	-40	-	10	-	μA
			Power down mode 2	-40	-	4	-	μA
			Power down mode 3	-40	-	1.8	-	μA
			Power down mode 4	-40	-	1.8	-	μA
			Power down mode 2+XTAL32+RTC	-40	-	6	-	μA
			Power down mode 2+LRC+RTC	-40	-	9	-	μA
			Power down mode 1	25	-	10	-	μA
			Power down mode 2	25	-	4	-	μA
			Power down mode 3	25	-	1.8	-	μA
			Power down mode 4	25	-	1.8	-	μA
			Power down mode 2+XTAL32+RTC	25	-	6	-	μA
			Power down mode 2+LRC+RTC	25	-	9	-	μA
			Power down mode 1	85	-	-	21	μA
			Power down mode 2	85	-	-	19	μA
			Power down mode 3	85	-	-	19	μA
			Power down mode 4	85	-	-	19	μA
			Power down mode 2+XTAL32+RTC	85	-	-	21	μA
			Power down mode 2+LRC+RTC	85	-	-	21	μA
			Power down mode 1	105	-	-	35	μA
			Power down mode 2	105	-	-	33	μA
			Power down mode 3	105	-	-	30	μA
			Power down mode 4[3]	105	-	-	30	μA
			Power down mode 2+XTAL32+RTC	105	-	-	35	μA
			Power down mode 2+LRC+RTC	105	-	-	35	μA

1. Typ voltage condition V_{CC}=3.3V.
2. Max Voltage Condition V_{CC}=1.8~3.6V.
3. Guarantee of mass production test.

Table 3-15 Analog Module Current Consumption

Item	Parameter	Symbol	Conditions (VCC=AVCC=3.3 V)	Ta (°C)	Product Specifications			Unit
					Min	Typ	Max	
Module Current	-	ICC_MODULE	XTAL Oscillation Mode Large Drive 24 MHz	25	-	1.8	-	mA
			Drive 16 MHz in Oscillation Mode	25	-	1	-	mA
			Oscillating mode small drive 10 MHz	25	-	0.8	-	mA
			Oscillating mode ultra-small drive 8 MHz	25	-	0.6	-	mA
			XTAL 32K	25	-	0.5	-	mA
			HRC	25	-	0.35	-	mA
			PLL（@480 MHz）	25	-	2.3	-	mA
			PLL（@240 MHz）	25	-	1.4	-	mA
			ADC	25	-	1.2	-	mA
			DAC	25	-	70	-	uA
			CMP	25	-	0.11	-	mA
			PGA	25	-	1	-	mA
			USBFS(1)	25	-	6	-	mA

1. Contains the current when the control section communicates with the USBPHY.

3.3.5 Electrical Sensitivity

The chip is tested differently (ESD, LU) using specific measurement methods to determine its performance in terms of electrical susceptibility.

3.3.5.1 Electrostatic discharge (ESD)

Electrostatic discharge is applied to the pins of each sample according to each pin combination. This test complies with JESD22-A114/C101 standard.

Table 3-16 ESD Characteristics

Symbol	Parameter	Conditions	Maximum Value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage	T_A =+25 °C, compliant with JESD22-A114	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging equipment model)	T_A =+25 °C, compliant with JESD22-C101	1000	

3.3.5.2 Static Latch-up

To assess static Latch-up performance, two complementary static Latch-up tests are required on the chip:

- Over-voltage applied to each power supply and analog input pin
- Apply current injection to other input, output and configurable I/O pins

These tests met the EIA/JESD 78 IC Latch-up standard.

Table 3-17 Static Latch-up Features

Symbol	Parameter	Conditions	Maximum Value	Unit
LU	Static Latch-up	T_A =+105 °C, compliant with JESD78	200	mA

3.3.6 Low Power Mode Wake-up Timing

The wake-up time measurement method is from the wake-up event triggering to the CPU execution of the first instruction:

- For stop or sleep mode: Wakeup event is WFE.
- WKUP pins are used to wake up from standby, stop, and sleep modes. All the timings are measured at ambient temperature and VCC=3.3V.

Table 3-18 Low Power Mode Wake Up Time

Symbol	Parameter	Conditions	Typical Value	Maximum Value	Unit
T_{STOP1}	Wakeup from stop mode	PWC_PWRC1.VHRCSD=1 and PWC_PWRC1.VPLLSD=1, the system clock is MRC, and the program is executed on RAM	2	5	μs
T_{STOP2}	Wakeup from stop mode	The system clock is MRC and the program is executed on Flash	8	15	
T_{PD1}(1)	Wake up from power-down mode 1	The total capacity of VCAP_1/VCAP_2 is 0.094μF or 0.1μF	15	25	
		The total capacity of VCAP_1/VCAP_2 is 0.2μF or 0.22μF	20	30	
T_{PD2}(1)	Wake up from power-down mode 2	The total capacity of VCAP_1/VCAP_2 is 0.094μF or 0.1μF	40	50	
		The total capacity of VCAP_1/VCAP_2 is 0.2μF or 0.22μF	45	55	
T_{PD3}(1)	Wake up from power-down mode 3	The total capacity of VCAP_1/VCAP_2 is 0.094μF or 0.1μF	2500	3000	
		The total capacity of VCAP_1/VCAP_2 is 0.2μF or 0.22μF	2500	3000	
T_{PD4}(1)	Wake up from power-down mode 4	The total capacity of VCAP_1/VCAP_2 is 0.094μF or 0.1μF	65	75	
		The total capacity of VCAP_1/VCAP_2 is 0.2μF or 0.22μF	70	80	

1. The total capacity of VCAP_1/VCAP_2 of the chip must match the assignment of the PWC_PWRC3.PDTS bit. When the total capacity of VCAP_1/VCAP_2 is 0.2μF or 0.22μF, it is necessary to ensure that the PWC_PWRC3.PDTS bit is cleared before entering power-down mode. When the total capacity of VCAP_1/VCAP_2 is 0.094μF or 0.1μF, it is necessary to ensure that the PWC_PWRC3.PDTS bit is set before entering power-down mode.

3.3.7 I/O Port Characteristics

General Input/Output Characteristics

Table 3-19 I/O Static Characteristics

Symbol	Parameter		Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{IL}(1)	Schmitt Input low level		1.8≤V_{CC}≤3.6	-	-	0.2V_{CC}	V
V_{IH}(1)	Schmitt Input high level		1.8≤V_{CC}≤3.6	0.8V_{CC}	-	-	V
V_{HYS}	Schmitt Input hysteresis		1.8≤V_{CC}≤3.6	-	0.2	-	V
V_{IL}	CMOS Input Low Voltage (3)		1.8≤V_{CC}≤3.6	-	-	0.3V_{CC}	V
V_{IH}	CMOS Input High Voltage (3)		1.8≤V_{CC}≤3.6	0.7V_{CC}	-	-	V
I_{LKG}(1)	I/O input current		V_{SS}≤V_{IN}≤V_{CC}	-1	-	1	μA
			V_{IN} = 5.5V(2)	-	-	5	μA
R_{PU}(1)(2)	Weak pull-up equivalent resistance	USBFS_DP, USBFS_DM	-	-	1.5	-	KΩ
		In addition to the other input pins of USBFS_DP and USBFS_DM	V_{IN} = V_{SS}	-	30	-	KΩ
C_{IO}	I/O pin capacitance	PA11/USBFS_DM PA12/USBFS_DP	-	-	10	-	pF
		Other input pins except PA11/USBFS_DM and PA12/USBFS_DP	-	-	5	-	pF

1. Guarantee of mass production test.
2. To keep the voltage above V_{CC}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
3. When the SPI functions (MOSI, MISO, SCK, NSS0) or the I2C functions (SDA, SCL) in SMBus mode are selected, the pin input type is CMOS. When other functions are selected, the pin input type is Schmitt.

The output voltage

Table 3-20 Output Voltage Characteristics

Driver Settings	Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum value	Unit
Low drive	V_{OL}(1)(2)	Low level output	I_{IO}=±1.5mA, 1.8≤V_{CC}<2.7	-	-	0.4	V
	V_{OH}(1)(3)	High level output		V_{CC}-0.4	-	-	
	V_{OL}(1)(2)	Low level output	I_{IO}=±3mA, 2.7≤V_{CC}≤3.6	-	-	0.4	
	V_{OH}(1)(3)	High level output		V_{CC}-0.4	-	-	
	V_{OL}(1)(2)	Low level output	I_{IO}=±6mA, 2.7≤V_{CC}≤3.6	-	-	1.3	
	V_{OH}(1)(3)	High level output		V_{CC}-1.3	-	-	
Medium drive	V_{OL}(1)(2)	Low level output	I_{IO}=±3mA, 1.8≤V_{CC}<2.7	-	-	0.4	
	V_{OH}(1)(3)	High level output		V_{CC}-0.4	-	-	
	V_{OL}(1)(2)	Low level output	I_{IO}=±5mA, 2.7≤V_{CC}≤3.6	-	-	0.4	
	V_{OH}(1)(3)	High level output		V_{CC}-0.4	-	-	
	V_{OL}(1)(2)	Low level output	I_{IO}=±12mA, 2.7≤V_{CC}≤3.6	-	-	1.3	
	V_{OH}(1)(3)	High level output		V_{CC}-1.3	-	-	
High drive	V_{OL}(1)(2)	Low level output	I_{IO}=±6mA, 1.8≤V_{CC}<2.7	-	-	0.4	
	V_{OH}(1)(3)	High level output		V_{CC}-0.4	-	-	
	V_{OL}(1)(2)	Low level output	I_{IO}=±8mA, 2.7≤V_{CC}≤3.6	-	-	0.4	
	V_{OH}(1)(3)	High level output		V_{CC}-0.4	-	-	
	V_{OL}(1)(2)	Low level output	I_{IO}=±20mA, 2.7 ≤V_{CC}≤3.6	-	-	1.3	
	V_{OH}(1)(3)	High level output		V_{CC}-1.3	-	-	

1. Guarantee of mass production test.
2. The device's I_{IO} sink current must always be taken into account the absolute maximum ratings specified in Table 3-3. The sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. The device's I_{IO} source current must always adhere to Table 3-3 the listed absolute maximum ratings, and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VCC}.

Input/output AC Characteristics

Table 3-21 I/O AC Characteristics

Driver Settings	Symbol	Parameter	Condition(3)	Minimum Value	Typical Value	Maximum Value	Unit
Low drive	f_{max}(IO)out	Maximum frequency(1)	C_L=30 pF, V_{CC}≥ 2.7 V	-	-	20	MHz
			C_L=30 pF, V_{CC}≥1.8 V	-	-	10	
			C_L=10pF, V_{CC}≥2.7 V	-	-	40	
			C_L=10pF, V_{CC}≥1.8 V	-	-	20	
	t_f(IO)out t_r(IO)out	Output high to low level drop time and output low to high level rise time	C_L=30 pF, V_{CC}≥2.7 V	-	-	15	ns
			C_L=30 pF, V_{CC}≥1.8 V	-	-	25	
			C_L=10pF, V_{CC}≥2.7 V	-	-	7.5	
			C_L=10pF, V_{CC}≥1.8 V	-	-	15	
Medium drive	f_{max}(IO)out	Maximum frequency(1)	C_L=30 pF, V_{CC}≥ 2.7 V	-	-	45	MHz
			C_L=30 pF, V_{CC}≥1.8 V	-	-	22.5	
			C_L=10pF, V_{CC}≥2.7 V	-	-	90	
			C_L=10pF, V_{CC}≥1.8 V	-	-	45	
	t_f(IO)out t_r(IO)out	Output high to low level drop time and output low to high level rise time	C_L=30 pF, V_{CC}≥2.7 V	-	-	7.5	ns
			C_L=30 pF, V_{CC}≥1.8 V	-	-	12	
			C_L=10pF, V_{CC}≥2.7 V	-	-	4	
			C_L=10pF, V_{CC}≥1.8 V	-	-	7.5	
High drive	f_{max}(IO)out	Maximum frequency (1)	C_L=30 pF, V_{CC}≥2.7 V	-	-	100	MHz
			C_L=30 pF, V_{CC}≥1.8 V	-	-	50	
			C_L=10pF, V_{CC}≥2.7 V	-	-	180	
			C_L=10pF, V_{CC}≥1.8 V	-	-	100	
	t_f(IO)out t_r(IO)out	Output high to low level drop time and output low to high level rise time	C_L=30 pF, V_{CC}≥2.7 V	-	-	4	ns
			C_L=30 pF, V_{CC}≥1.8 V	-	-	6	
			C_L=10pF, V_{CC}≥2.7 V	-	-	2.5	
			C_L=10pF, V_{CC}≥1.8 V	-	-	4	

1. The maximum frequency is defined in Figure 3-.
2. The load capacitance C_L must take into account the capacitance of the PCB and the MCU pin (the capacitance of the pin to the board can be roughly estimated as 10pF).

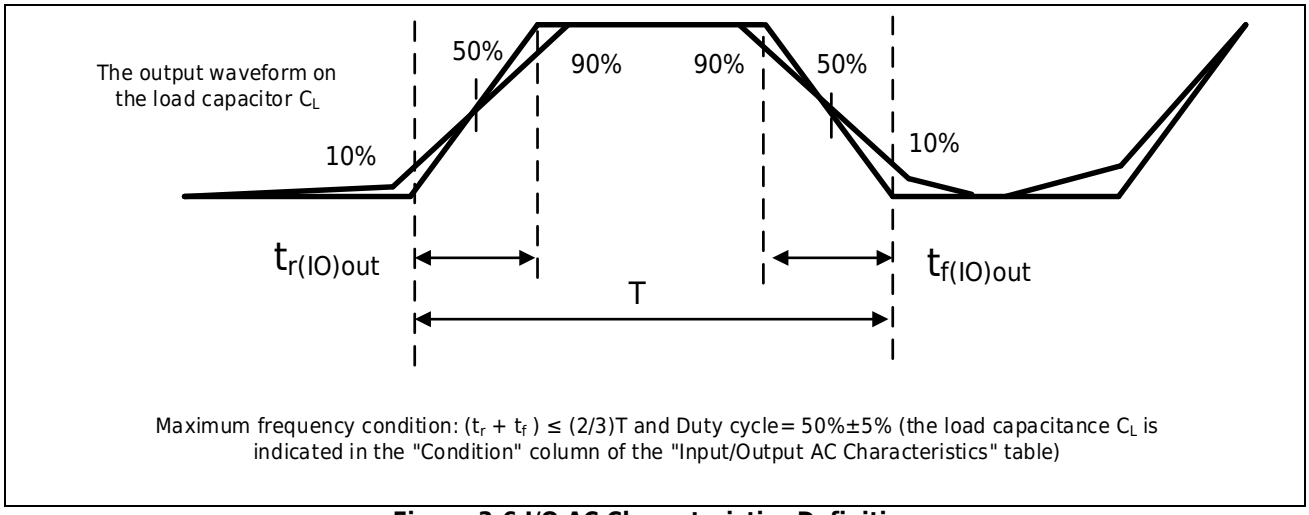


Figure 3-6 I/O AC Characteristics Definition

3.3.8 USART Interface Characteristics

Table 3-22 USART AC Timing

Symbol	Parameter		Minimum value	Maximum value	Unit
t_{cyc}	Input clock cycles	UART	4	-	t_{PCLK1}
		CSI	6	-	
t_{CKw}	Input Clock Width		0.4	0.6	t_{Scyc}
t_{CKr}	Input Clock Rise Time		-	5	ns
t_{CKf}	Input Clock Fall Time		-	5	ns
t_{TD}	Send delay time	CSI	-	28	ns
t_{RDS}	Receive data setup time	CSI	15	-	ns
t_{RDH}	Receive data hold time	CSI	5	-	ns

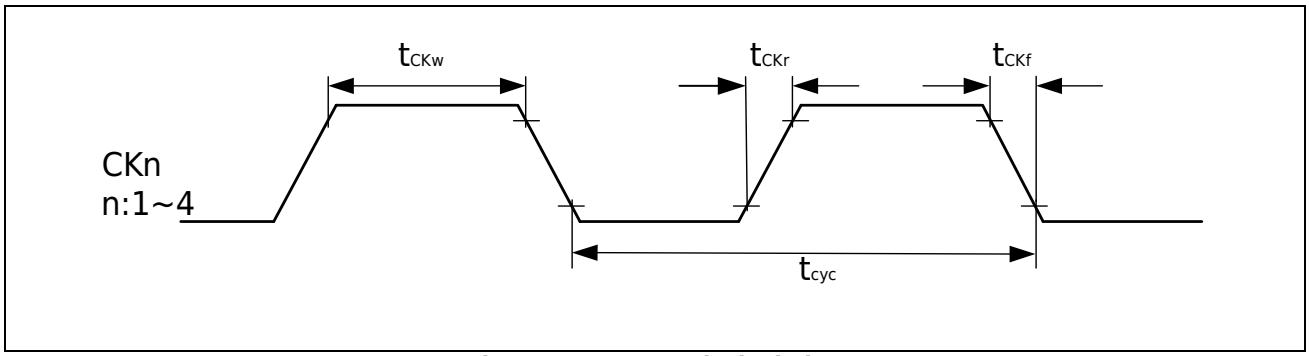


Figure 3-7 USART Clock Timing

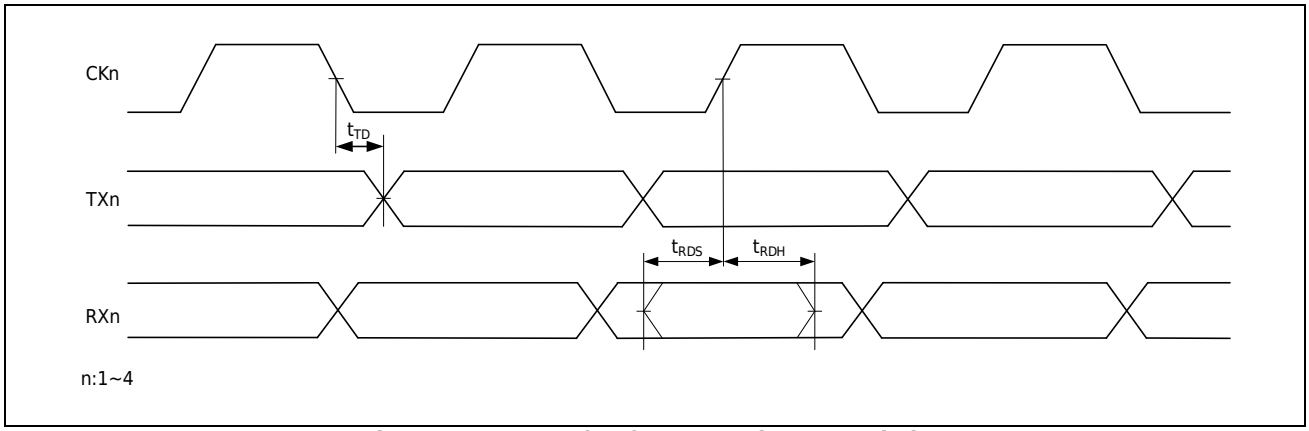


Figure 3-8 USART (CSI) Input and Output Timing

3.3.9 I2S Interface Characteristics

Table 3-23 I2S Electrical Characteristics

Symbol	Performance	Conditions	Min	Max	Unit
f_{MCK}	I2S main clock output	-	256 *8K	256*Fs	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	20	64*Fs	MHz
		Slave data: 32 bits	-	64*Fs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
t_v(WS)	WS valid time	Master mode	0	-	ns
t_h(WS)	WS hold time	Master mode	0	-	
t_{su}(WS)	WS setup time	Slave mode	1	-	
t_h(WS)	WS hold time	Slave mode	0	-	
t_{su}(SD_MR)	Data input setup time	Master receiver	7.5	-	
t_{su}(SD_SR)		Slave receiver	2	-	
t_h(SD_MR)	Data input hold time	Master receiver	0	-	
t_h(SD_SR)		Slave receiver	0	-	
t_v(SD_ST) t_h(SD_ST)	Data output valid time	Slave transmitter (after enable edge)	-	27	
t_v(SD_MT)		Master transmitter (after enable edge)	-	20	
t_h(SD_MT)	Data output hold time	Master transmitter (after enable edge)	2.5	-	

1. Fs: I2S sampling frequency

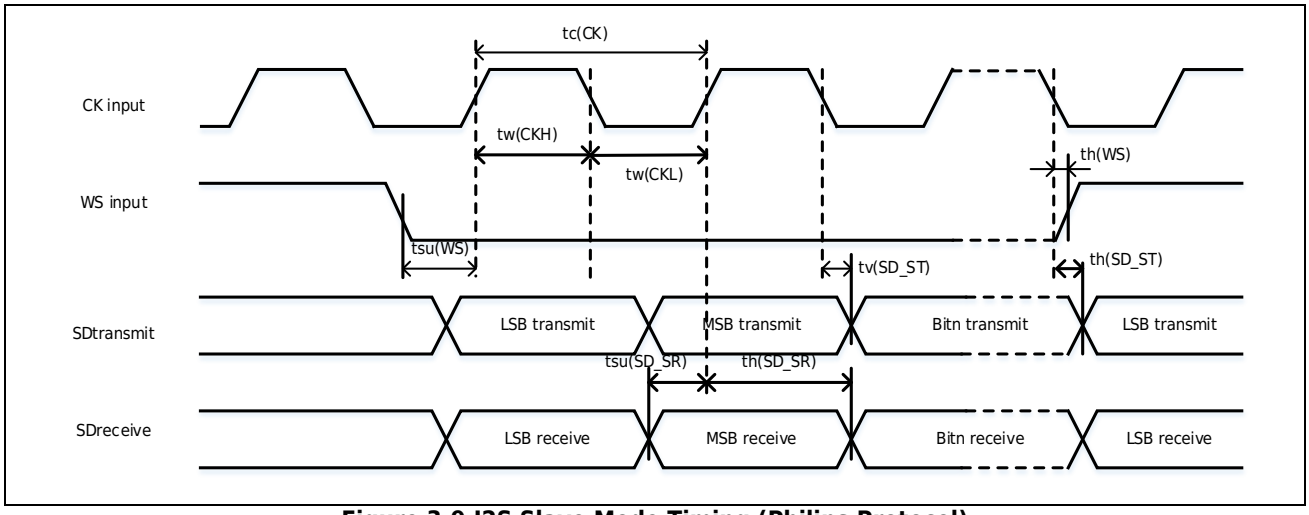


Figure 3-9 I2S Slave Mode Timing (Philips Protocol)

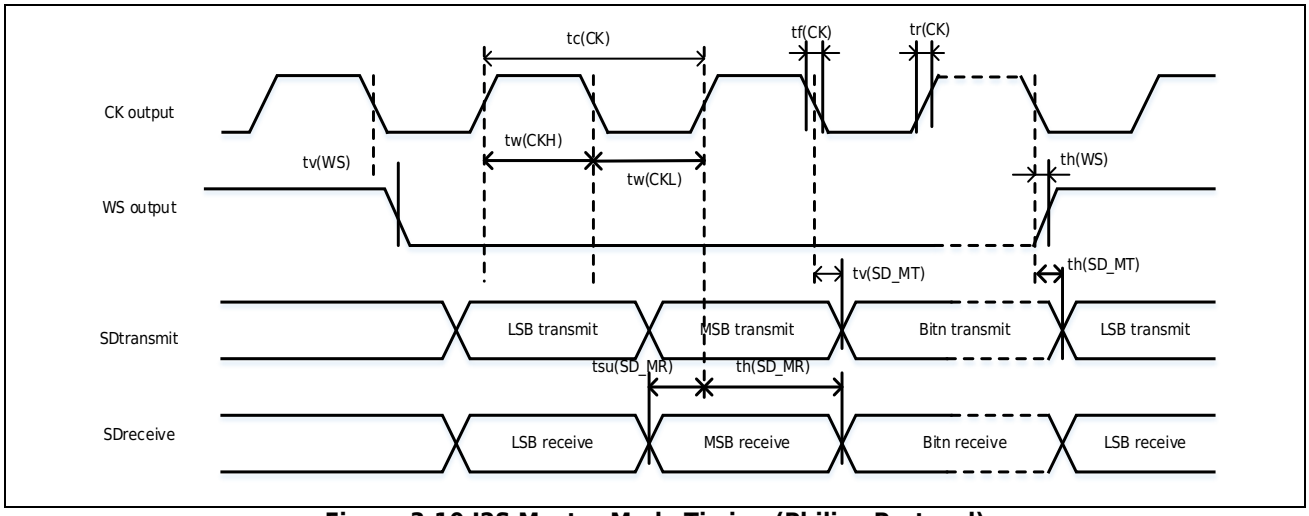


Figure 3-10 I2S Master Mode Timing (Philips Protocol)

3.3.10 I2C Interface Characteristics

Table 3-24 I2C Electrical Characteristics

Symbol	Parameter	Standard Mode (SM)		Fast Mode (FM)		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL frequency	0	100	0	400	KHz
$t_{HD;STA}$	Start condition/restart condition Hold	4.0	-	0.6	-	μs
t_{LOW}	SCL Low Level	4.7	-	1.3	-	μs
t_{HIGH}	SCL High Level	4	-	0.6	-	μs
$t_{SU;STA}$	Restarting Condition Setup	4.7	-	0.6	-	μs
$t_{HD;DAT}$	Data Hold	0	-	0	-	μs
$t_{SU;DAT}$	Data Setup	30+ $t_{I2C\ reference\ clock\ period}$	-	30+ $t_{I2C\ reference\ clock\ period}$	-	ns
t_R	Ascending time of SCL/SDA	-	1000	-	300	ns
t_F	Falling time of SCL/SDA	-	300	-	300	ns
$t_{SU;STO}$	Stop Condition Setup	4	-	0.6	-	μs
t_{BUF}	BUS Idle Time Between Stop Condition and Start Condition	4.7	-	1.3	-	μs
C_b	Load capacitance	-	400	-	400	pF

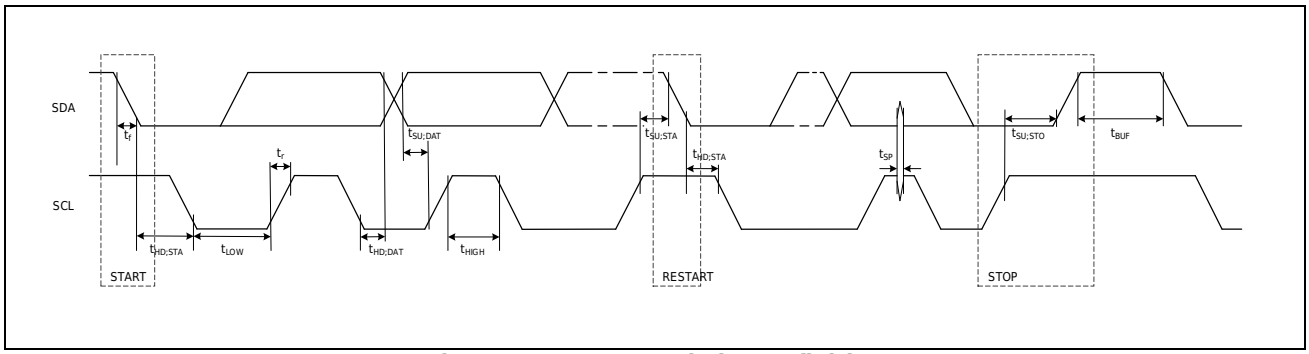


Figure 3-5 I2C Bus Timing Definition

3.3.11 SPI Interface Characteristics

Table 3-25 SPI Electrical Characteristics

Item		Symbol	Min	Max	Unit	Test conditions
SCK clock cycle	Master	tspcyc	2 (pclk ≤60 MHz) 4 (pclk ≤60 MHz)	4096	tpcyc	Figure 3-12 C=30pF
	Slave		6	4096		
SCK clock rise and fall time	Master	tsckr tsckf	-	5	ns	
	Slave		-	1	μs	
Data input setup time	Master	tsu	4	-	ns	Figure 3-13/14/15 C=30pF
	Slave		5	-		
Data input hold time	Master	th	tpcyc	-	ns	
	Slave	-	20	-		
Data output delay	Master	tod	-	8	ns	
	Slave		-	20		
Data output hold time	Master	toh	0	-	ns	
	Slave		0	-		
MOSI/MISO rise and fall time	Master	tdr tdf	-	5	ns	
	Slave		-	1	μs	
SS rise and fall time	Master	tssr tssf	-	5	ns	
	Slave		-	1	μs	

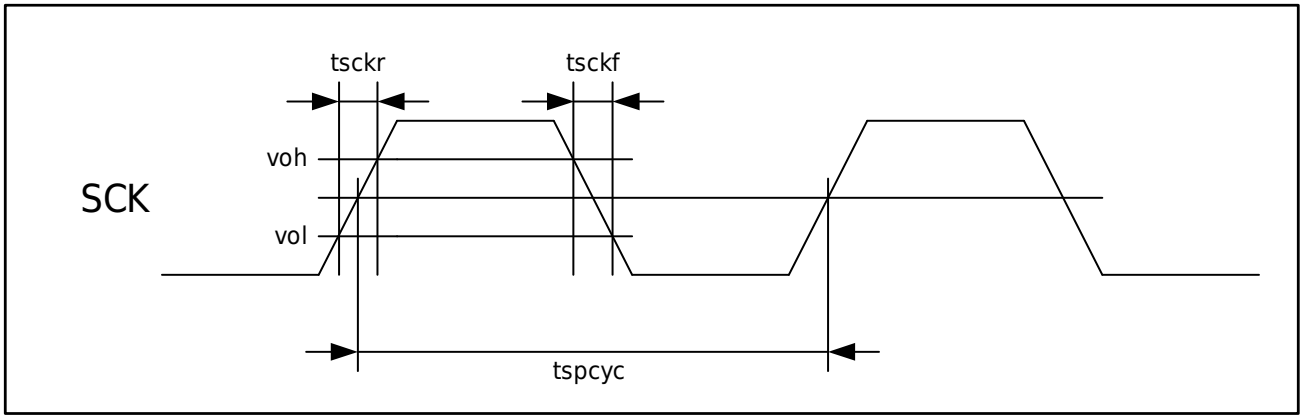


Figure 3-6 SCK Clock Definition

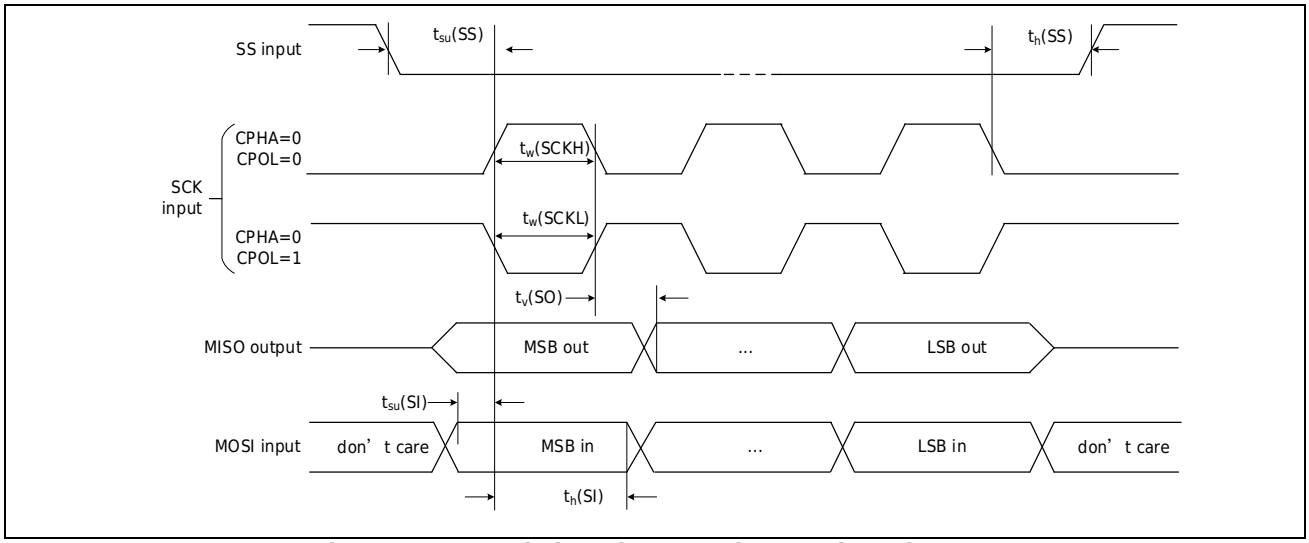


Figure 3-7 SPI Timing Diagram -Slave Mode and CPHA=0

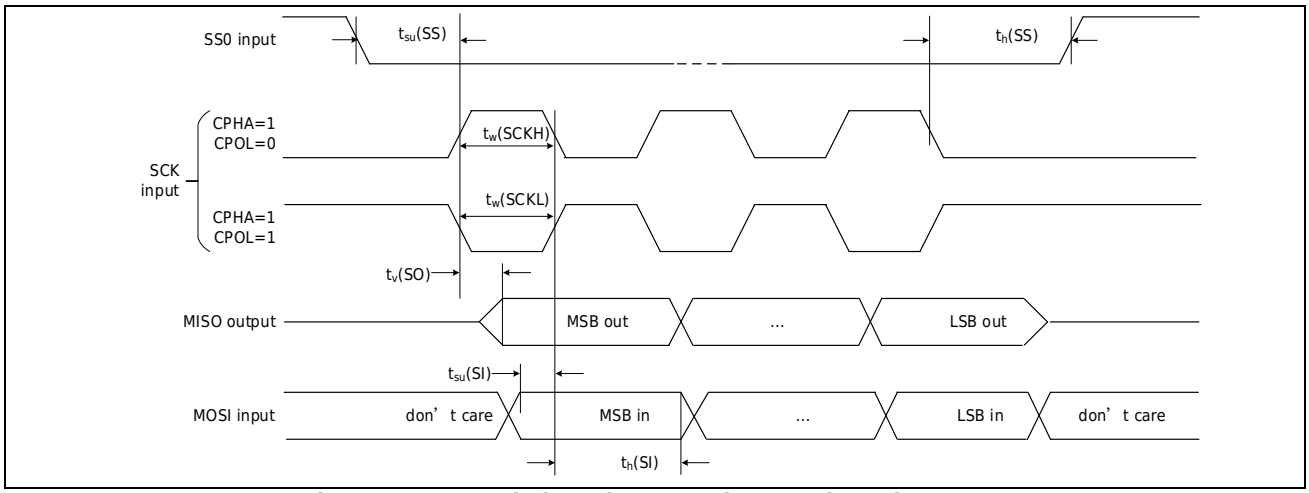


Figure 3-8 SPI Timing Diagram -Slave Mode and CPHA=1

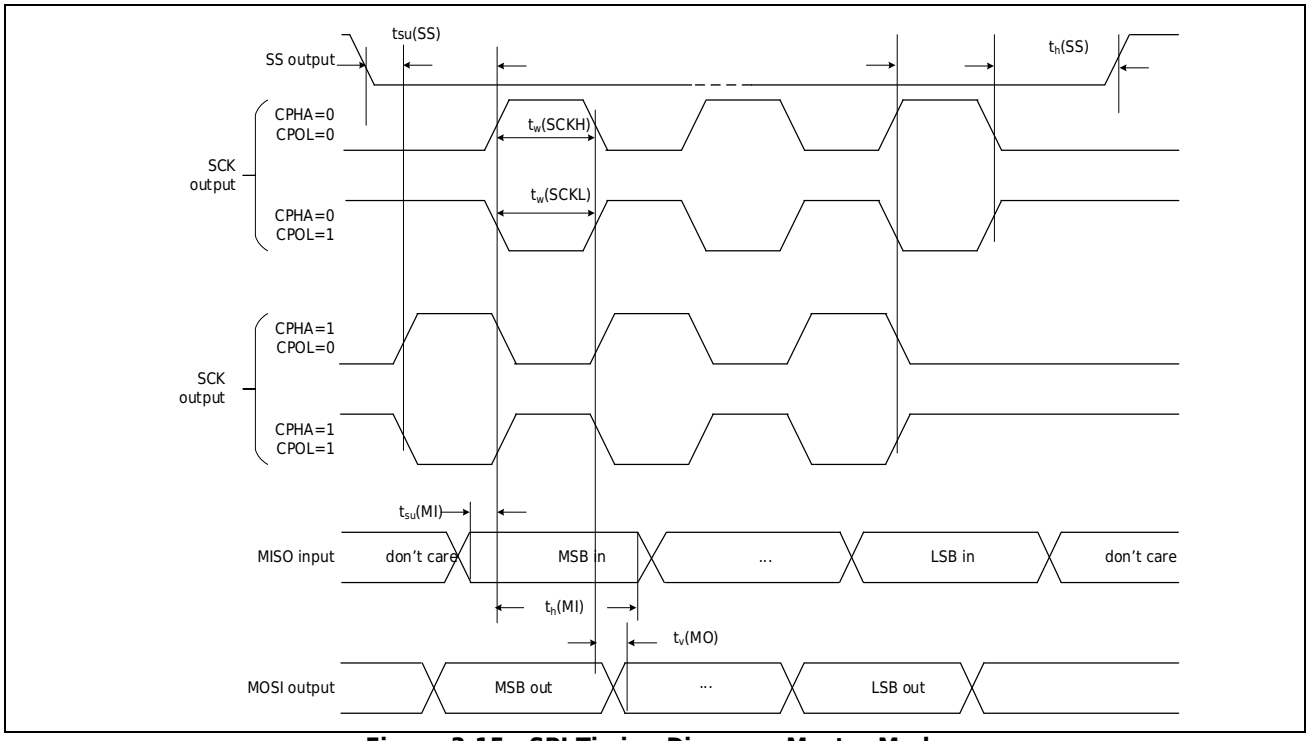


Figure 3-15 SPI Timing Diagram -Master Mode

3.3.12 CAN2.0B Interface Characteristics

For port characteristics of CANx_TX and CANx_RX, please refer to 3.3.7 I/O Port Characteristics.

3.3.13 USB Interface Characteristics

Table 3-26 USB Full-Speed Electrical Characteristics

Symbol		Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
Input	V_{CC}	Operating Voltage	-	3.0(2)	-	3.6	V
	V_{IL}	Input low level	-	-	-	0.8	V
	V_{IH}	Input high level	-	2.0	-	-	V
	V_{DI}	Differential Input Sensitivity	-	0.2	-	-	V
	V_{CM}	Differential Common Mode Voltage	-	0.8	-	2.5	V
Output	V_{OL}(3)	Static output low level	R_L=1.5kΩ to 3.6V(4)	-	-	0.3	V
	V_{OH}(3)	Static output high level	R_L=15kΩ to VSS(4)	2.8	-	3.6	V
	V_{CRS}	Cross-over voltage	C_L=50pF	1.3	-	2.0	V
	t_R	Rise Time	C_L=50pF, 10 %~90 % of $\|V_{OH}-V_{OL}\|$	4	-	20	ns
	t_F	Fall time	C_L=50pF, 10 %~90 % of $\|V_{OH}-V_{OL}\|$	4	-	20	ns
	t_{RFMA}	Rise and fall time ratio t_R/t_F	C_L=50pF	90	-	111.1	%
R_{PD}(3)		Pull-down resistor	V_{IN}= V_{CC}, in host mode	-	15	-	kΩ
R_{PU}(3)		Pull-up resistance	V_{IN}= V_{SS}, idle state	0.900	1.2	1.575	kΩ
			V_{IN}= V_{SS}, in device mode	1.425	2.3	3.090	kΩ

1. All voltages are measured against local ground potential.
2. The function of the USB full-speed transceiver is still guaranteed when the operating voltage is reduced to 2.7V, but the complete USB full-speed electrical characteristics are not guaranteed, which will be degraded in the V_{CC} voltage range of 2.7 to 3.0V.
3. Guarantee of mass production test.
4. R_L is the load connected to the USB full speed drive.

Table 3-27 USB Low-Speed Electrical Characteristics

Symbol		Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
Input	V_{CC}	Operating Voltage	-	3.0(2)	-	3.6	V
	V_{IL}	Input low level	-	-	-	0.8	V
	V_{IH}	Input high level	-	2.0	-	-	V
	V_{DI}	Differential Input Sensitivity	-	0.2	-	-	V
	V_{CM}	Differential Common Mode Voltage	-	0.8	-	2.5	V
Output	V_{OL}(3)	Static output low level	R_L=1.5kΩ to 3.6V(4)	-	-	0.3	V
	V_{OH}(3)	Static output high level	R_L=15kΩ to VSS(4)	2.8	-	3.6	V
	V_{CRS}(3)	Cross-over voltage	C_L=200pF~600pF	1.3	-	2.0	V
	t_R(3)	Rise Time	C_L=200pF~600pF, 10 %~90 % of $\|V_{OH}-V_{OL}\|$	75	-	300	ns
	t_F(3)	Fall time	C_L=200pF~600pF, 10 %~90 % of $\|V_{OH}-V_{OL}\|$	75	-	300	ns
	t_{RFMA}(3)	Rise and fall time ratio t_R/t_F	C_L=200pF~600pF	80	-	125	%
R_{PD}(3)		Pull-down resistor	V_{IN}= V_{CC}, in host mode	14.25	-	24.80	kΩ

1. All voltages are measured against local ground potential.
2. When the operating voltage drops to 2.7V, the function of the USB low-speed transceiver can still be guaranteed, but the complete USB low-speed electrical characteristics cannot be guaranteed, and the latter will be degraded in the V_{CC} voltage range of 2.7 to 3.0V.
3. Guarantee of mass production test.
4. R_L is the load connected to the USB low-speed drive.

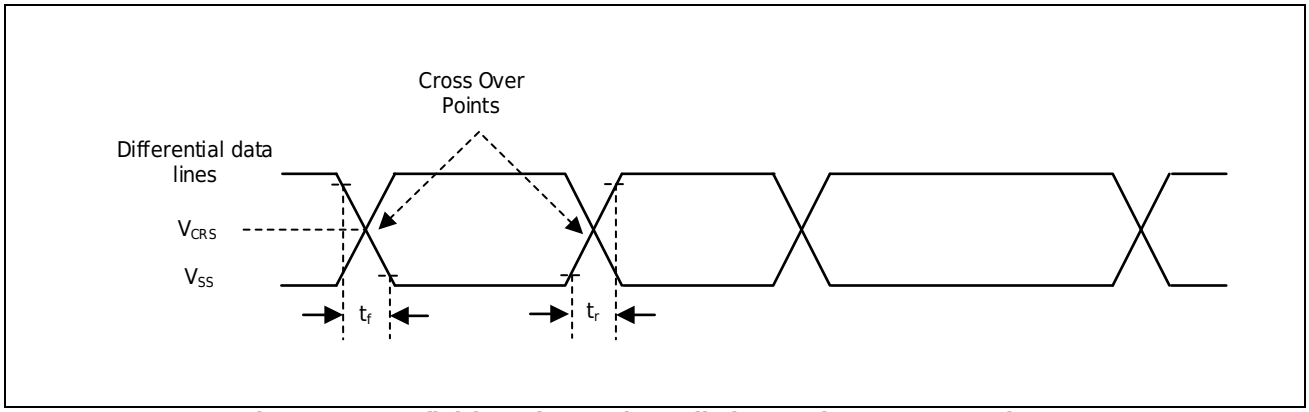


Figure 3-9 Definition of USB Rise/Fall Time and Cross Over Voltage

3.3.14 PLL Characteristic

Table 3-28 PLL Main Performance Indicators

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL PFD (Phase Frequency Detector) input clock(1)	-	1	-	25	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	15	-	240	MHz
f_{VCO_OUT}	PLL VCO output	-	240	-	480	MHz
$Jitter_{PLL}$	Period Jitter	PLL PFD input clock=8MHz, System clock=120MHz, Peak-to-Peak	-	±100	-	ps
	Cycle-to-Cycle Jitter	PLL PFD input clock=8MHz, System clock=120MHz, Peak-to-Peak	-	±150	-	
t_{LOCK}	PLL lock time	-	-	80	120	μs

1. It is recommended to use a higher input clock to obtain good Jitter characteristics.

3.3.15 JTAG Interface Characteristics

Table 3-29 JTAG Interface Features

Symbol	Item	Min	Typ	Max	Unit
t_{TCKcyc}	JTCK clock cycle time	50	-	-	ns
t_{TCKH}	JTCK clock high pulse width	20	-	-	ns
t_{TCKL}	JTCK clock low pulse width	20	-	-	ns
t_{TCKr}	JTCK clock rise time	-	-	5	ns
t_{TCKf}	JTCK clock fall time	-	-	5	ns
t_{TMSs}	JTMS setup time	8	-	-	ns
t_{TMSh}	JTMS hold time	8	-	-	ns
t_{TDIs}	JTDI setup time	8	-	-	ns
t_{TDIh}	JTDI hold time	8	-	-	ns
t_{TDOd}	JTDO data delay time	-	-	20	ns

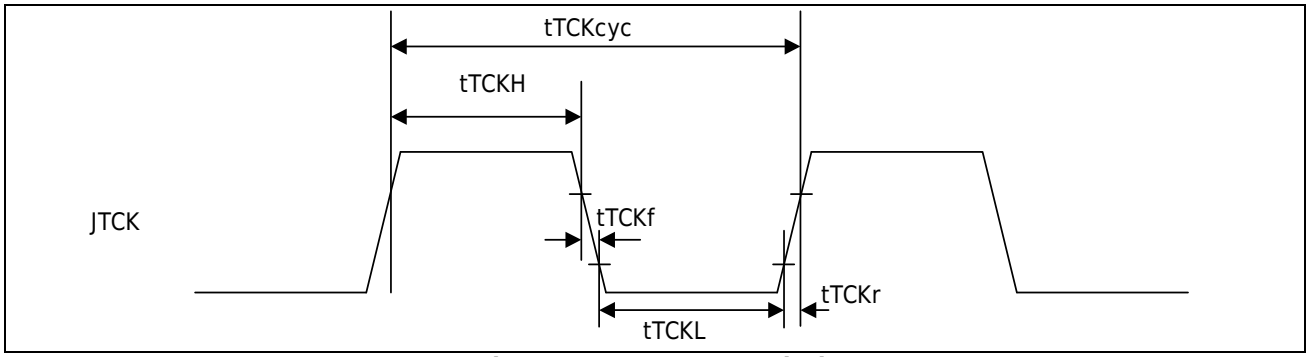


Figure 3-10 JTAG JTCK Clock

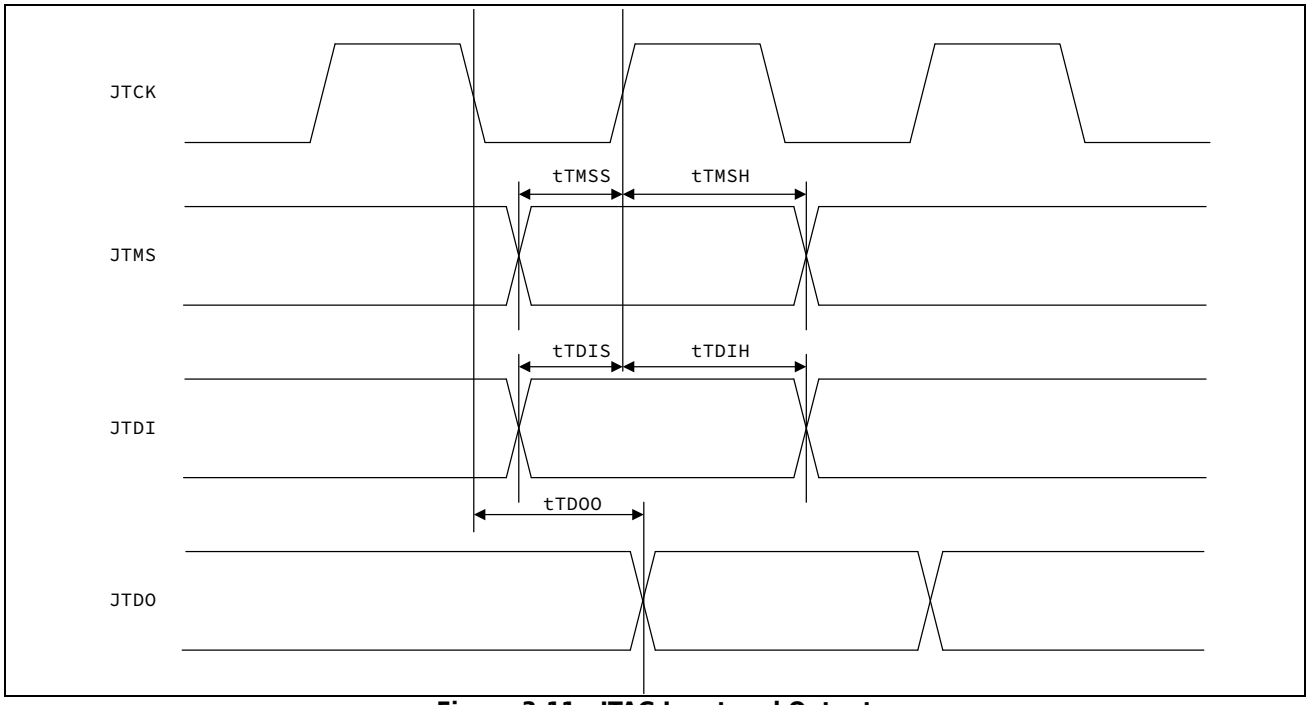


Figure 3-11 JTAG Input and Output

3.3.16 External Timer Characteristic

3.3.16.1 High-speed External Subscriber Clock Generated by External Source

In bypass mode, XTAL oscillator is off and the input pin is standard I/O. External clock signals must take into account I/O static characteristics.

Table 3-30 High-Speed External User Clock Features

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{XTAL_EXT}	User external clock source frequency	-	1	-	25	MHz
V_{IH_XTAL}	XTAL_EXT input pin high level		0.8*V_{CC}	-	V_{CC}	V
V_{IL_XTAL}	XTAL_EXT input pin low level		V_{SS}	-	0.2*V_{CC}	
$t_{r(XTAL)}$ $t_{f(XTAL)}$	XTAL_EXT rise or fall time		-	-	5	ns
$Duty_{(XTAL)}$	duty cycle	-	40	-	60	%

3.3.16.2 High-speed external clock produced by crystal oscillator/ceramic resonator

High-speed external (XTAL) clocks can be produced using a 4 to 25 MHz crystal oscillator/ceramic resonator oscillator. In applications, the resonator and load capacitance must be as close to the oscillator pin as possible to minimize output distortion and vibration stabilization time. For more information on the resonator characteristics (frequency, encapsulation, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 3-31 XTAL 4-25 MHz Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{XTAL_IN}	Oscillator frequency		4	-	25	MHz
R_F(1)	Feedback resistance		-	300	-	kΩ
A_{XTAL}(2)	XTAL accuracy	-	-500	-	500	ppm
G_{mmax}	Oscillator G_m	Wake up	4	-	-	mA/V
$t_{SU(XTAL)}$(3)	Start time	VCC is stable, crystal oscillator=8MHz	-	2.0	-	ms
		VCC is stable, crystal oscillator=4MHz	-	4.0	-	ms

1. Guarantee of mass production test.
2. This parameter depends on the resonator used on the application system.
3. $t_{SU(XTAL)}$ is the start-up time, that is, the time between the software enabling the XTAL to measure until the stable 8MHz oscillation frequency is obtained. This value is measured based on the standard crystal resonator and may vary significantly with the crystal resonator manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors designed for high-frequency applications that meet crystal or resonator requirements (see figure below). C_{L1} and C_{L2} are usually the same size, C_{L1}=C_{L2}=2*(C_L-Cs). Cs is the PCB and MCU pins (XTAL_IN, XTAL_OUT) stray capacitance.

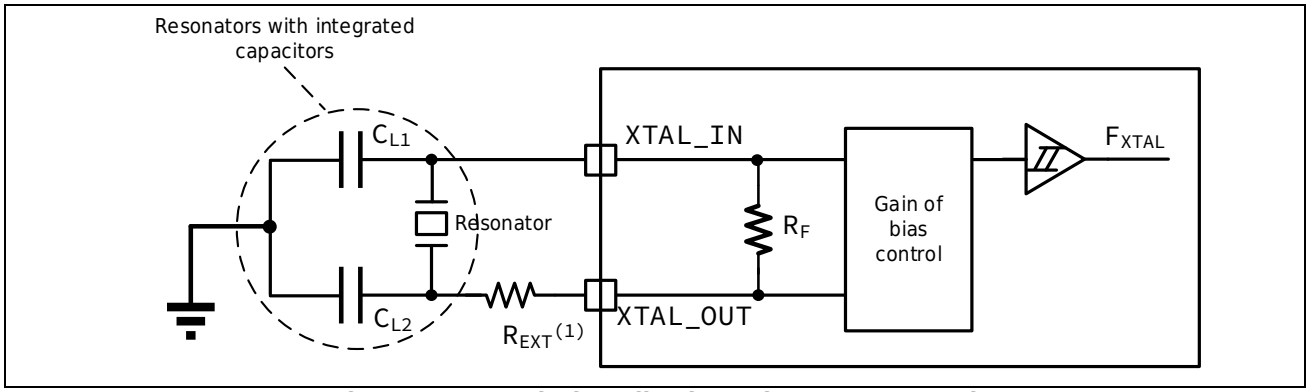


Figure 3-12 Typical Application Using 8 MHz Crystal

1. The value of R_{EXT} depends on the crystal oscillator characteristics.

3.3.16.3 Low-speed external clock generated by crystal oscillator/ceramic resonator

Low-speed external clocks can be produced using an oscillator composed of 32.768 kHz crystal oscillator/ceramic resonator. In applications, the resonator and load capacitance must be as close to the oscillator pin as possible to minimize output distortion and vibration stabilization time. For more information on the resonator characteristics (frequency, encapsulation, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 3-32 XTAL32 Oscillator Features

Symbol	Parameter	Conditions	Specifications			Unit
			Min	Typ	Max	
FXTAL32	Frequency	-	-	32.768	-	kHz
RF(1)	Feedback resistance	-	-	15	-	MΩ
IDD_XTAL32	Power consumption	XTAL32DRV[2:0] =000	-	0.8	-	μA
AXTAL32(2)	XTAL32 precision	-	-500	-	500	ppm
Gmmax	Oscillator Gm	-	5.6	-	-	μA/V
TSUXTAL32	Start time (3)	VCC Stabilization	-	2	-	s

1. Guarantee of mass production test.
2. This parameter depends on the resonator used on the application system.
3. TSUXTAL 32 is the start-up time, which starts with the software enabling XTAL 32 to measure until a stable oscillation frequency of 32.768 kHz is obtained. This value is measured based on the standard crystal resonator and may vary significantly with the crystal resonator manufacturer.

For CL1 and CL2, high quality external ceramic capacitors are recommended (see figure below). CL1 and CL2 are usually the same size, CL1=CL2=2*(CL-Cs). Cs is the PCB and MCU pins (XTAL32_IN, XTAL32_OUT) stray capacitance. If CL1 and CL2 are greater than 18pF, it is recommended to set XTAL32DRV [2:0] =001 (large drive, the typical value of power consumption increases by 0.2 μA).

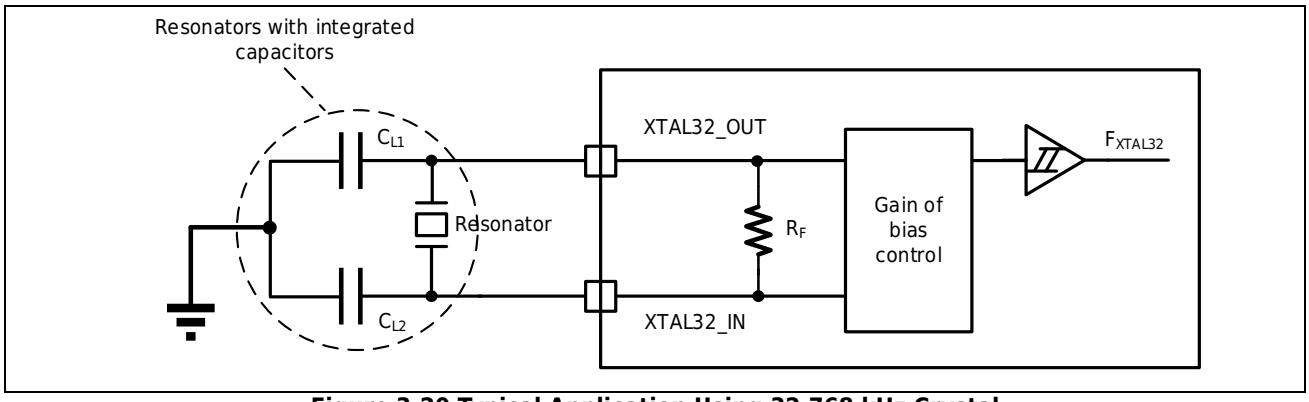


Figure 3-20 Typical Application Using 32.768 kHz Crystal

3.3.17 Internal Timer Characteristics

3.3.17.1 Internal High Speed (HRC) Oscillator

Table 3-33 HRC Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{HRC}	Frequency (1)	Pattern 1	-	16	-	MHz
		Pattern 2	-	20	-	
	User Adjustment Scale	-	-	-	0.2	%
	Frequency Accuracy (1)	T_A = -40 to 105 ℃	-2	-	2	%
		T_A = -20 to 105 ℃	-1.5	-	1.5	%
		T_A = 25 ℃	-0.5	-	0.5	%
$t_{st(HRC)}$	HRC oscillator oscillation stabilization time	-	-	-	15	μs

1. Guarantee of mass production test.

3.3.17.2 Internal Medium Speed (MRC) Oscillator

Table 3-34 MRC Oscillator Characteristics

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit
f_{MRC}(1)	Frequency	7.2	8	8.8	MHz
$t_{st(MRC)}$	MRC Oscillator Settling Time	-	-	3	μs

1. Guarantee of mass production test.

3.3.17.3 Internal Low Speed (LRC) Oscillator

Table 3-35 LRC Oscillator Characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
f_{LRC}(1)	Frequency	27.853	32.768	37.683	kHz
$t_{st(LRC)}$	LRCoscillator Stabilization Time	-	-	36	μs

1. Guarantee of mass production test.

3.3.17.4 SWDT Dedicated Internal Low-Speed (SWDTLRC) Oscillator

Table 3-36 SWDTLRC Oscillator Characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
$f_{SWDTLRC}$(1)	Frequency	9	10	11	kHz
tst(SWDTLRC)	SWDTLRC oscillator stabilization time	-	-	57.1	μs

1. Guarantee of mass production test.

3.3.18 12-bit ADC Characteristic

Table 3-37 ADC Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{AVCC}	Power supply	-	1.8	-	3.6	V
V_{REFH}(1)	positive reference voltage	-	1.8	-	V_{AVCC}	V
f_{ADC}	ADC conversion clock frequency	In super high speed/high speed operation mode V_{AVCC}=2.4 ~3.6 V	1	-	60	MHz
		In super high speed/high speed operation mode V_{AVCC}=1.8 ~2.4 V	1	-	30	
		Super low speed operation mode	1	-	8	
V_{AIN}	Conversion voltage range	-	V_{AVSS}	-	V_{REFH}	V
R_{AIN}	External input impedance	Refer to Formula 1 for details	-	-	50	kΩ
R_{ADC}	Sampling switch resistance	-	-	-	6	kΩ
C_{ADC}	Internal sampling and retention capacitance	-	-	4	7	pF
t_D	Trigger conversion delay	f_{ADC} = 60 MHz	-	-	0.3	μs

Table 3-38 ADC Characteristics (Continued)

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
t_S	Sampling time	f_{ADC}=60MHz	0.183	-	4.266	μs
			11	-	255	1/ f_{ADC}
t_{CONV}	Single-channel total conversion time (Including sampling time)	f_{ADC} = 60 MHz 12-bit resolution	0.4	-	-	μs
		f_{ADC} = 60 MHz 10-bit resolution	0.36	-	-	μs
		f_{ADC} = 60 MHz 8-bit resolution	0.33	-	-	μs
		20 to 268 (sampling time tS + successive approach n-bit resolution + 1)				1/f_{ADC}
f_S	Sampling rate f_{ADC} = 60 MHz	12-bit resolution single ADC	-	-	2.5	Msps
		12-bit resolution time-interpolated dual ADC	-	-	4.6	
t_{ST}	Power-on time	-	-	1	2	μs

1. V_{AVCC}-V_{REFH}<1.2V

Formula 1: RAIN Maximum Formula

$$R_{AIN}=\frac{k-1}{f_{ADC}\times C_{ADC}\times \ln(2^{N+2})}-R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance to make the error lower than 1/4 LSB. Where N = 12 (12-bit resolution), k is the number of sampling cycles defined in the ADC _ SSTR register.

Table 3-39 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Accuracy@ f_{ADC}=60MHz

Symbol	Parameter	Conditions	Typical value	Maximum value	Unit
E_T	Absolute error	In super high speed/high speed operation mode f_{ADC}=60MHz Input source impedance < 1kΩ V_{AVCC}=2.4 ~3.6V	±4.5	±6	LSB
E_O	Offset error		±3.5	±6	LSB
E_G	Gain error		±3.5	±6	LSB
E_D	Differential linear error		±1	±2	LSB
E_L	Integral linear error		±1.5	±3	LSB

Table 3-40 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Accuracy@ f_{ADC}=30MHz

Symbol	Parameter	Conditions	Typical Value	Maximum Value	Unit
E_T	Absolute error	In super high speed/high speed operation mode f_{ADC}=30MHz Input source impedance < 1kΩ V_{AVCC}=2.4 ~3.6V	±4.5	±6	LSB
E_O	Offset error		±3.5	±6	LSB
E_G	Gain error		±3.5	±6	LSB
E_D(1)	Differential linear error		±1	±2	LSB
E_L(1)	Integral linear error		±1.5	±3	LSB

1. Guarantee of mass production test.

Table 3-41 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Accuracy@ f_{ADC}=30MHz

Symbol	Parameter	Conditions	Typical value	Maximum value	Unit
E_T	Absolute error	In super high speed/high speed operation mode f_{ADC}=30MHz Input source impedance < 1kΩ V_{AVCC}=1.8 ~2.4V	±4.5	±6	LSB
E_O	Offset error		±3.5	±6	LSB
E_G	Gain error		±3.5	±6	LSB
E_D	Differential linear error		±1	±2	LSB
E_L	Integral linear error		±2	±3	LSB

Table 3-42 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Accuracy@ f_{ADC}=8MHz

Symbol	Parameter	Conditions	Typical value	Maximum value	Unit
E_T	Absolute error	In ultra-low speed operation mode f_{ADC}=8MHz Input source impedance < 1kΩ V_{AVCC}=1.8 ~3.6V	±4.5	±6	LSB
E_O	Offset error		±3.5	±6	LSB
E_G	Gain error		±3.5	±6	LSB
E_D	Differential linear error		±1	±2	LSB
E_L	Integral linear error		±2	±3	LSB

Table 3-43 ADC1_IN12~15, ADC12_IN8~11 Input Channel Accuracy@ f_{ADC}=60MHz

Symbol	Parameter	Conditions	Typical Value	Maximum Value	Unit
E_T	Absolute error	In super high speed/high speed operation mode f_{ADC}=60MHz Input source impedance < 1kΩ V_{AVCC}=2.4 ~3.6V	±5.5	±7	LSB
E_O	Offset error		±4.5	±7	LSB
E_G	Gain error		±4.5	±7	LSB
E_D	Differential linear error		±1.5	±2	LSB
E_L	Integral linear error		±2.0	±3	LSB

Table 3-44 ADC1_IN12~15, ADC12_IN8~11 Input Channel Accuracy@ f_{ADC}=30MHz

Symbol	Parameter	Conditions	Typical value	Maximum value	Unit
E_T	Absolute error	In super high speed/high speed operation mode f_{ADC}=30MHz Input source impedance < 1kΩ V_{AVCC}=2.4 ~3.6V	±5.5	±7	LSB
E_O	Offset error		±4.5	±7	LSB
E_G	Gain error		±4.5	±7	LSB
E_D(1)	Differential linear error		±1.5	±2	LSB
E_L(1)	Integral linear error		±2.0	±3	LSB

1. Guarantee of mass production test.

Table 3-45 ADC1_IN12~15, ADC12_IN8~11 Input Channel Accuracy @ f_{ADC}=30MHz

Symbol	Parameter	Conditions	Typical value	Maximum value	Unit
E_T	Absolute error	In super high speed/high speed operation mode f_{ADC}=30MHz Input source impedance < 1kΩ V_{AVCC}=1.8 ~2.4V	±5.5	±7	LSB
E_O	Offset error		±4.5	±7	LSB
E_G	Gain error		±4.5	±7	LSB
E_D	Differential linear error		±1.5	±2	LSB
E_L	Integral linear error		±2.5	±3	LSB

Table 3-46 ADC1_IN12~15, ADC12_IN8~11 Input Channel Accuracy@ f_{ADC}=8MHz

Symbol	Parameter	Conditions	Typical value	Maximum value	Unit
E_T	Absolute error	In ultra-low speed operation mode f_{ADC}=8MHz Input source impedance < 1kΩ V_{AVCC}=1.8 ~3.6V	±5.5	±7	LSB
E_O	Offset error		±4.5	±7	LSB
E_G	Gain error		±4.5	±7	LSB
E_D	Differential linear error		±1.5	±2	LSB
E_L	Integral linear error		±2.5	±3	LSB

Table 3-47 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Input Channel Dynamic Accuracy@ fADC=60MHz

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
ENOB	Significant digits	In super high speed/high speed operation mode f_{ADC}=60MHz Input signal frequency = 2kHz Input source impedance < 1kΩ V_{AVCC}=2.4 ~3.6V	10.6	-	Bits
SINAD	SNR		64	-	dB
SNR	SNR		66	-	dB
THD	Total Harmonic Distortion		-	-70	dB

Table 3-48 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Input Channel Dynamic Accuracy@ f_{ADC}=30MHz

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
ENOB	Significant digits	In super high speed/high speed operation mode f_{ADC}=30MHz Input signal frequency = 2kHz Input source impedance < 1kΩ V_{AVCC}=1.8~2.4 V	10.4	-	Bits
SINAD	SNR		62	-	dB
SNR	SNR		64	-	dB
THD	Total Harmonic Distortion		-	-67	dB

Table 3-49 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Input Channel Dynamic Accuracy@ f_{ADC}=8MHz

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
ENOB	Significant digits	In ultra-low speed operation mode f_{ADC}=8 MHz Input signal frequency = 2kHz Input source impedance < 1kΩ V_{AVCC}=1.8~3.6V	10.4	-	Bits
SINAD	SNR		62	-	dB
SNR	SNR		64	-	dB
THD	Total Harmonic Distortion		-	-67	dB

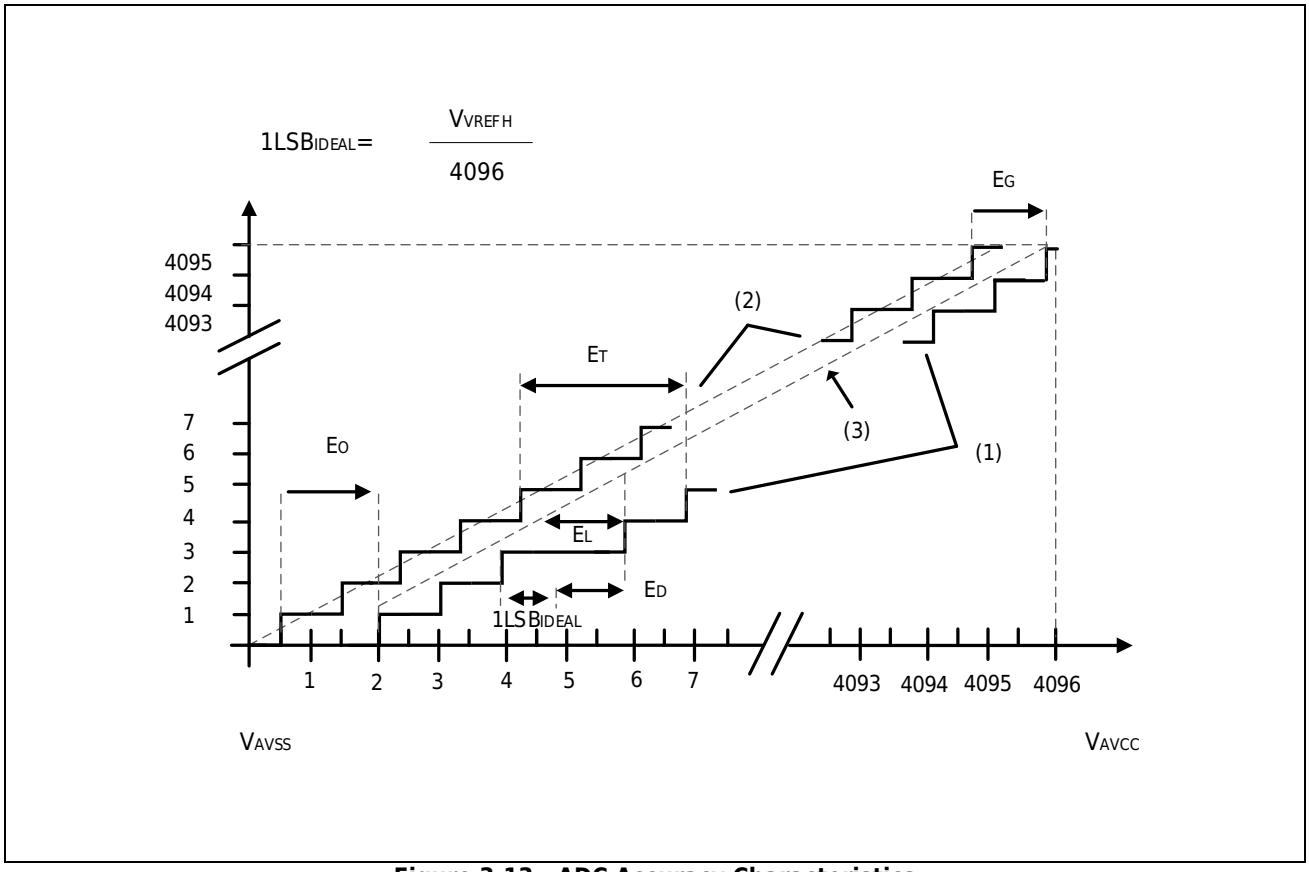


Figure 3-13 ADC Accuracy Characteristics

1. Refer to also table above.
2. Examples of actual transmission curves.
3. Ideal transfer curve.

   E_T = Total Unadjusted Error: The maximum deviation between the actual and ideal transfer curve.

   E_O = Offset Error: The deviation between the first actual transition and the first ideal transition.

   E_G = Gain Error: The deviation between the last ideal transition and the last actual transition.

   E_D = Differential Linearity Error: The maximum deviation between the actual step and the ideal.

   E_L = Integral Linearity Error: The maximum deviation between any actual transformation and the line associated with the endpoints.

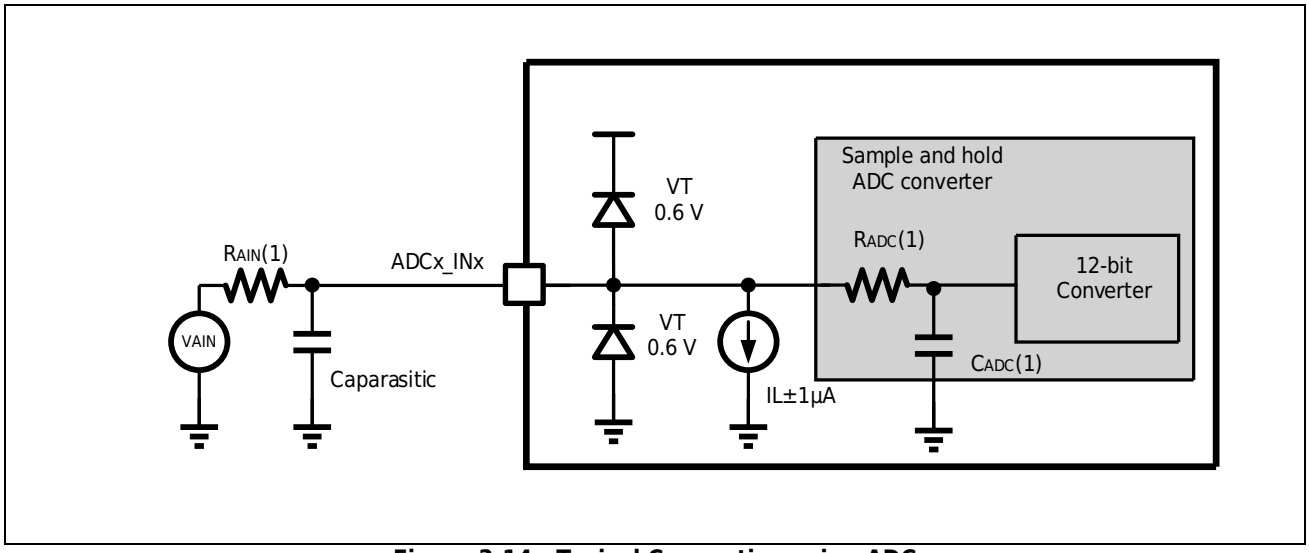


Figure 3-14 Typical Connection using ADC

1. For information on R_{AIN}, R_{ADC}, and C_{ADC} values, refer to Table 3-37.
2. Cparasitic represents PCB capacitance (depending on welding and PCB wiring quality) and pad capacitance (approximately 5pF). Higher values of Cparasitic result in less accurate conversions. To solve this problem, f_{ADC} should be reduced.

General PCB design guidelines

The power supply should be decoupled as shown in the figure below, depending on whether VREFH is connected to AVCC or not and the number of AVCC pins. The 0.1uF capacitor should be a (good quality) ceramic capacitor. These capacitors should be placed as close to the chip as possible.

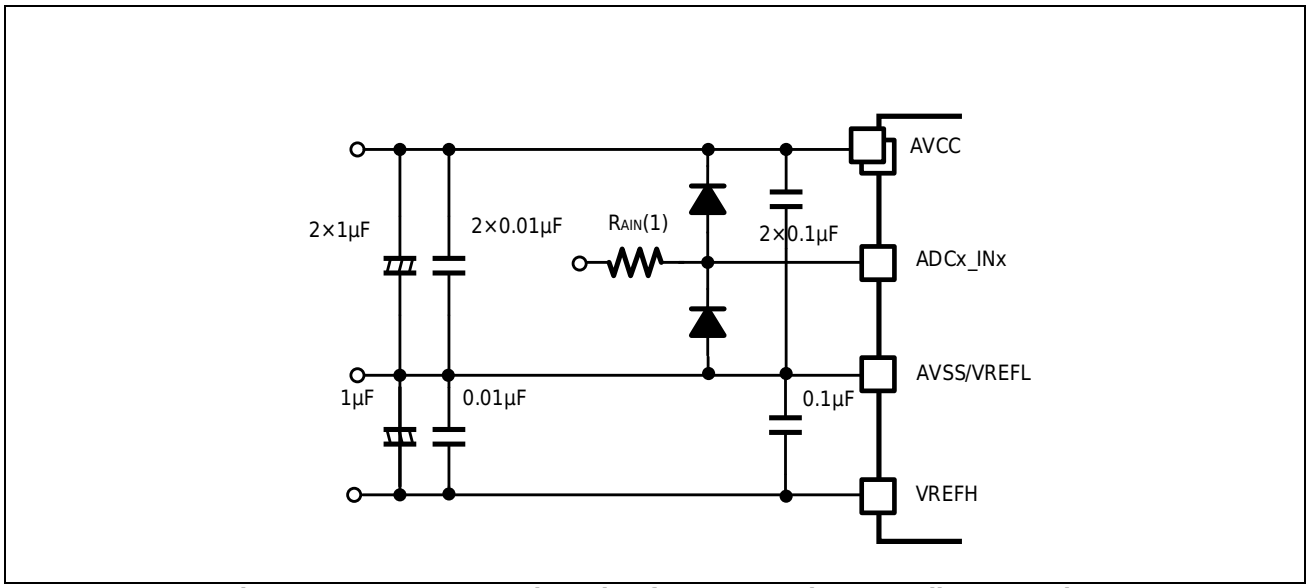


Figure 3-15 Power Supply and Reference Supply Decoupling Example

3.3.19 DAC Characteristic

Table 3-50 DAC Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{AVCC}	Analog supply voltage	-	1.8	3.3	3.6	V
DNL	Differential nonlinearity error (deviation between two consecutive codes -1LSB)	-	-	-	±2	LSB
offset	Offset error (difference between measured value at code (0x80) and ideal value $V_{AVCC}/2$	-	-	-	±2	LSB
$T_{SETTLING}$	Settling Time (Full Scale: Applies to 8-bit input code transitions between lowest and highest input codes until DA0/DA1 reach ±4LSB of final value)	-	-	-	8	μs

3.3.20 Comparator Characteristics

Table 3-51 Comparator Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{AVCC}	Analog supply voltage	-	1.8	3.3	3.6	V
V_I	Input voltage range	-	0	-	V_{AVCC}	V
T_{cmp}	Comparison time	Comparator resolution voltage = 100mV	-	50	100	ns
T_{set}	Input channel switching stabilization time	-	-	100	200	ns

3.3.21 Gain Adjustable Amplifier Characteristics

Table 3-52 Gain Adjustable Amplifier Characteristics

Symbol	Parameter		Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{AVCC}	Analog supply voltage		-	1.8	3.3	3.6	V
V_{OS}(1)	Input offset voltage		-	-8	-	8	mV
V_I	Input voltage range		-	0.1*V_{AVCC}/Gain	-	0.9*V_{AVCC}/Gain	V
G_E	Gain error	Use external port PGAVSS as PGA negative input	Gain=2(1)	-1	-	1	%
			Gain=2.133	-1	-	1	%
			Gain=2.286	-1	-	1	%
			Gain=2.667	-1	-	1	%
			Gain=2.909	-1	-	1	%
			Gain=3.2	-1.5	-	1.5	%
			Gain=3.556	-1.5	-	1.5	%
			Gain=4.0	-1.5	-	1.5	%
			Gain=4.571	-2	-	2	%
			Gain=5.333	-2	-	2	%
			Gain=6.4	-3.0	-	3.0	%
			Gain=8	-3.0	-	3.0	%
			Gain=10.667	-4.0	-	4.0	%
			Gain=16	-4.0	-	4.0	%
			Gain=32(1)	-7.0	-	7.0	%
		Use the internal analog ground AVSS as the PGA negative input	Gain=2(1)	-2	-	2	%
			Gain=2.133	-2	-	2	%
			Gain=2.286	-2	-	2	%
			Gain=2.667	-2	-	2	%
			Gain=2.909	-2	-	2	%
			Gain=3.2	-2.5	-	2.5	%
			Gain=3.556	-2.5	-	2.5	%
			Gain=4.0	-2.5	-	2.5	%
			Gain=4.571	-3.0	-	3.0	%
			Gain=5.333	-3.0	-	3.0	%
			Gain=6.4	-4.0	-	4.0	%
			Gain=8	-4.0	-	4.0	%
			Gain=10.667	-5.0	-	5.0	%
			Gain=16	-5.0	-	5.0	%
			Gain=32(1)	-8.0	-	8.0	%

1. Guarantee of mass production test.

3.3.22 Temperature Sensor

Table 3-53 Temperature Sensor Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
TL	Relative accuracy	According to the user manual, each chip is calibrated individually	-	-	±5	°C

3.3.23 Memory Characteristics

3.3.23.1 Flash memory

Flash memory was erased when the device was delivered to the customer.

Table 3-54 Flash Features

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
I_{VCC}	Supply current	Read mode, V_{CC}=1.8 V~3.6 V	-	-	5	mA
		Programming mode, V_{CC}=1.8 V~3.6 V	-	-	10	
		Block erase mode, V_{CC}=1.8 V~3.6 V	-	-	10	
		Full erase mode, V_{CC}=1.8 V~3.6 V	-	-	10	

Table 3-55 Flash Program Erase Time

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
T_{prog}(1)	Word programming time	Single programming mode	43+2* T_{hclk}(2)	48+4* T_{hclk}(2)	53+6* T_{hclk}(2)	μs
	Word programming time	Continuous programming mode	12+2* T_{hclk}(2)	14+4* T_{hclk}(2)	16+6* T_{hclk}(2)	μs
T_{erase}(1)	Block erase time	-	16+2* T_{hclk}(2)	18+4* T_{hclk}(2)	20+6* T_{hclk}(2)	ms
T_{mas}(1)	Full erase time	-	16+2* T_{hclk}(2)	18+4* T_{hclk}(2)	20+6* T_{hclk}(2)	ms

1. Guarantee of mass production test.
2. T_{hclk} is one cycle of CPU clock.

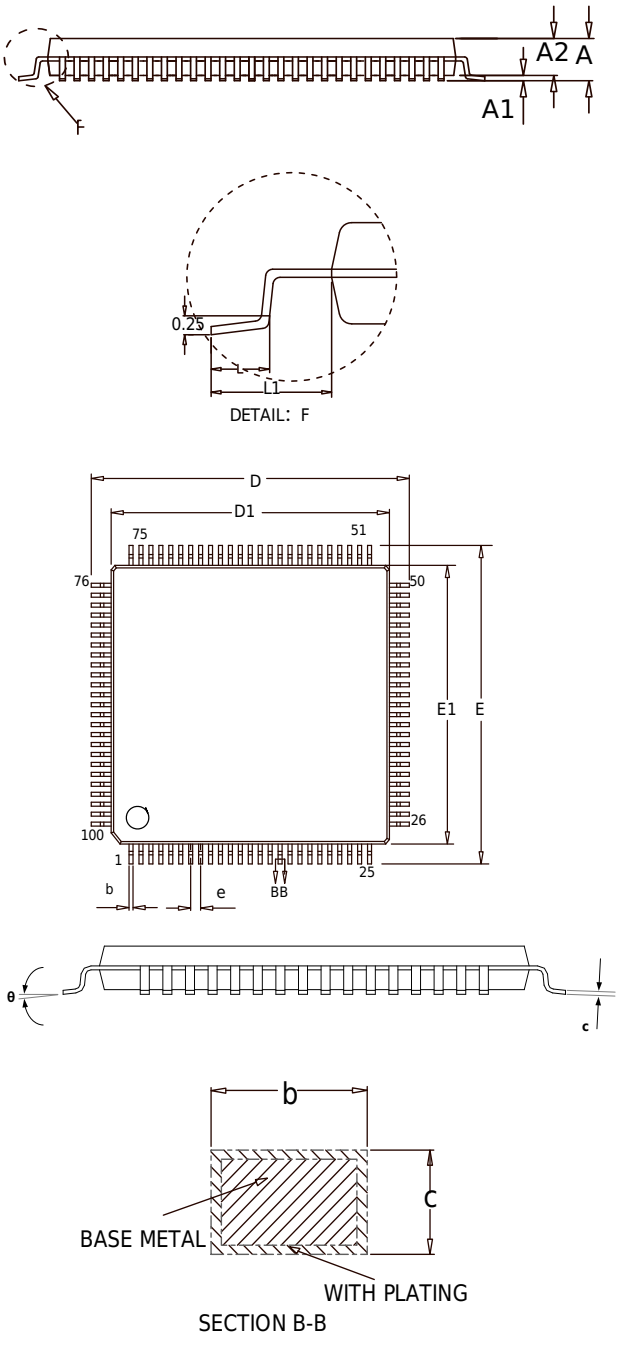
Table 3-56 Flash Memory Erasability and Data Storage Period

Symbol	Parameter	Conditions		Minimum Value	Typical Value	Unit
N_{end}	Program, block erase times	T_A = -40˚C~105˚C	Data Storage Period (T_{ret}): 10 years, T_A=85˚C	-	100,000	times
			Data Storage Period (T_{ret}): 20 years, T_A=85˚C	10,000	-	times

4 Packaging Information

4.1 Packaging Size

LQFP100 packaging

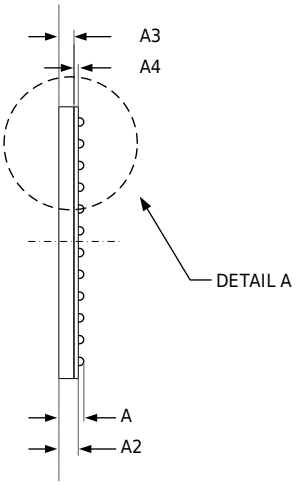


Symbol	14x14 Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
-	-	-	-
b	0.17	-	0.27
-	-	-	-
c	0.09	-	0.20
-	-	-	-
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

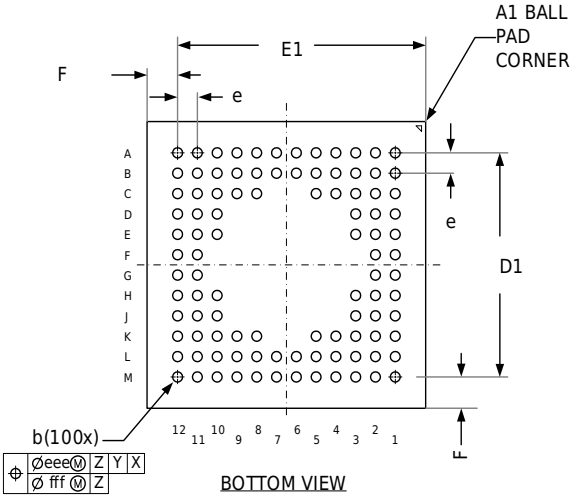
NOTE:

- *Dimensions "D1" and "E1" do not include mold flash.*

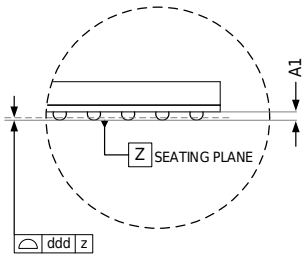
VFBGA100 packaging



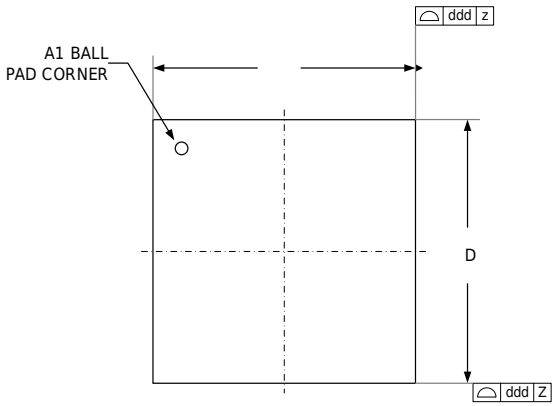
SIDE VIEW



BOTTOM VIEW

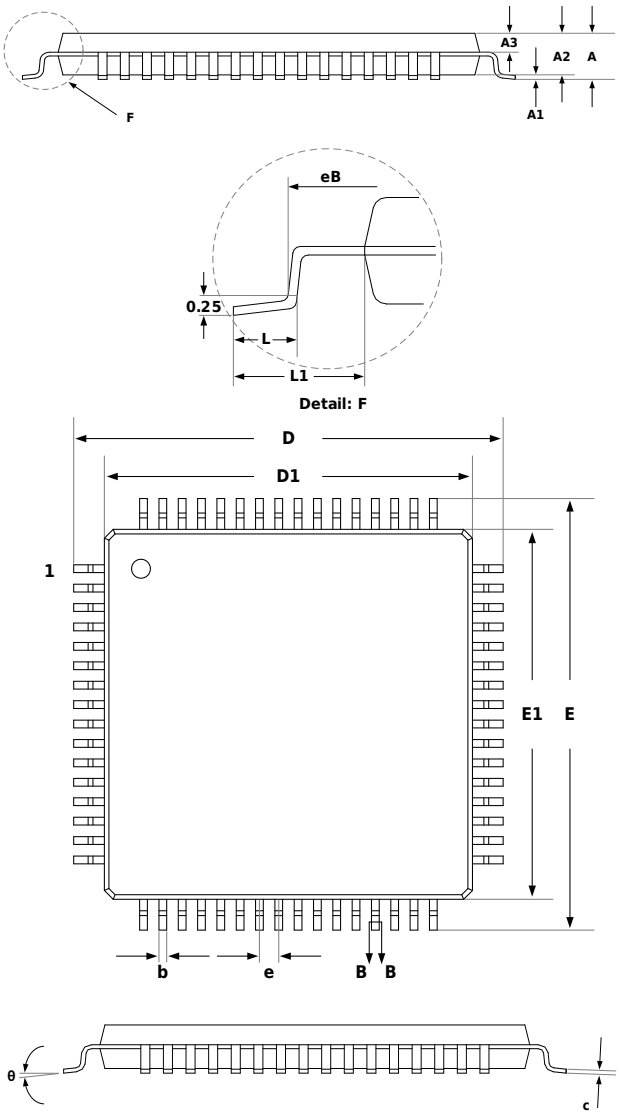


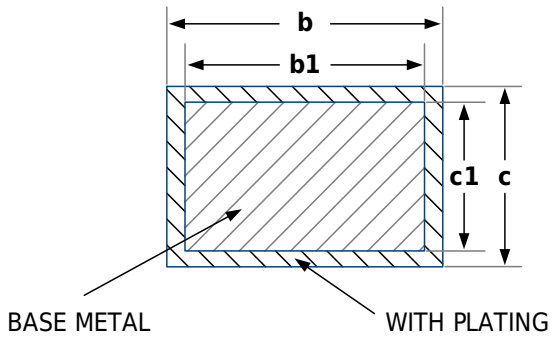
DETAIL A
ROTATED 90°



Symbol	7x7 Millimeter		
	Min	Nom	Max
A	0.67	0.74	0.81
A1	0.11	0.16	0.21
A2	0.54	0.58	0.62
A3		0.45REF	
A4		0.13REF	
b	0.20	0.25	0.30
D	6.90	7.00	7.10
D1	-	5.5	-
E	6.90	7.00	7.10
E1	-	5.5	-
e	-	0.5	-
F		0.75REF	
ddd	-	0.10	-
eee	-	0.15	-
fff	-	0.05	-

LQFP64 packaging





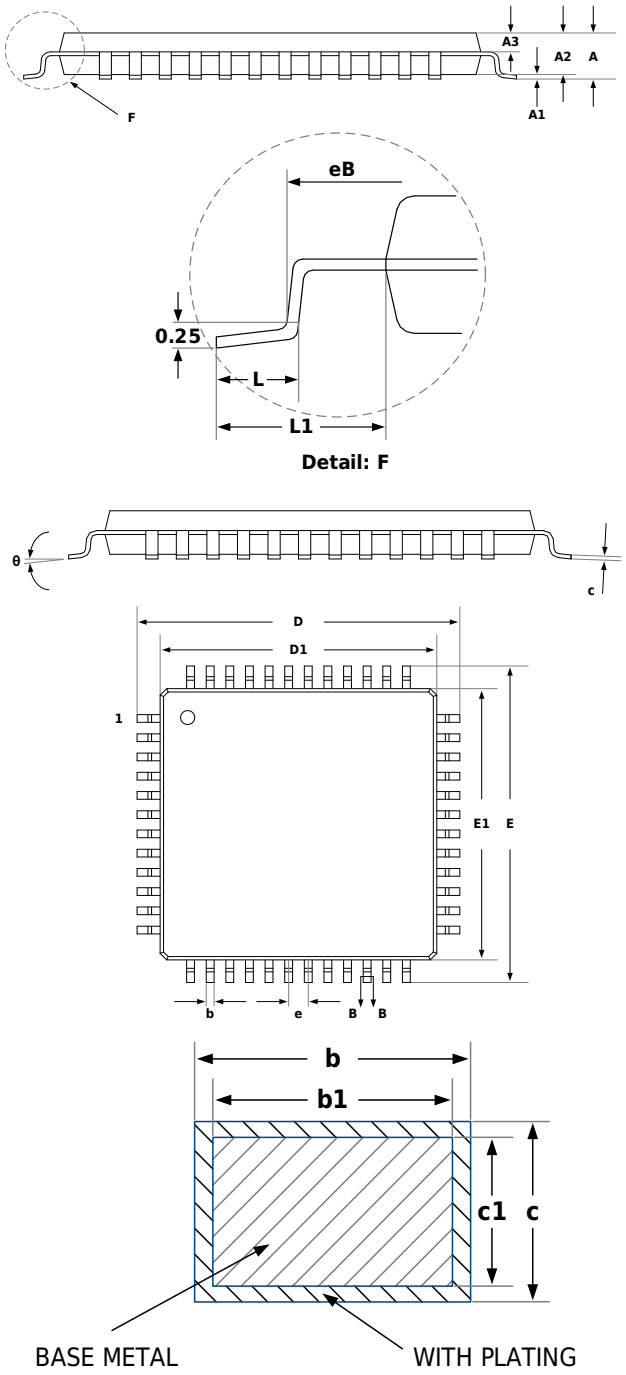
SECTION B-B

Symbol	10x10 Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	7°

NOTE:

- *Dimensions "D1" and "E1" do not include mold flash.*

LQFP48 packaging



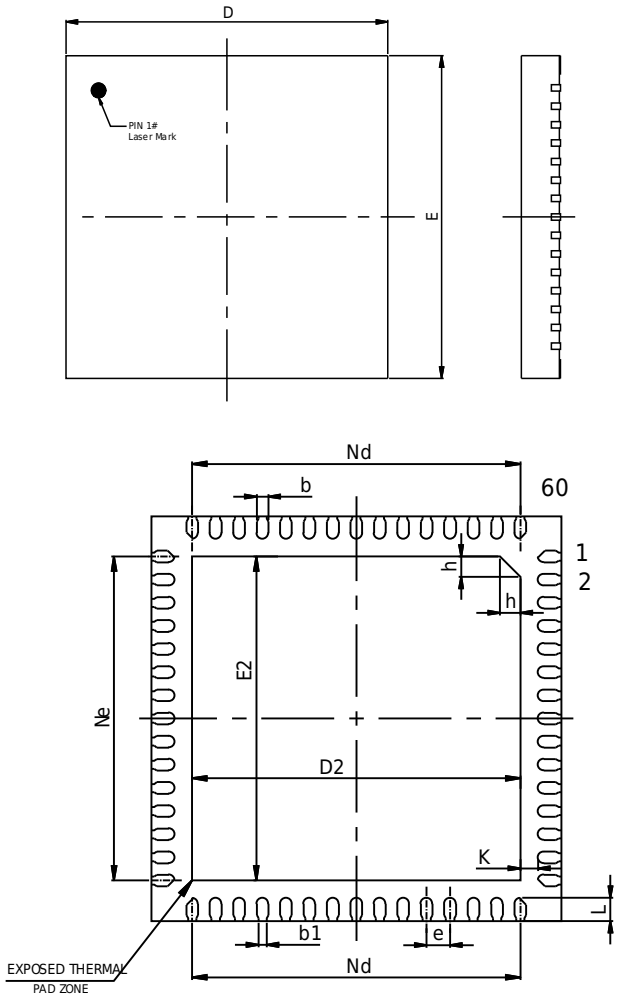
SECTION B-B

Symbol	7x7 Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.40	-	0.65
L1	1.00REF		
θ	0	-	7°

NOTE:

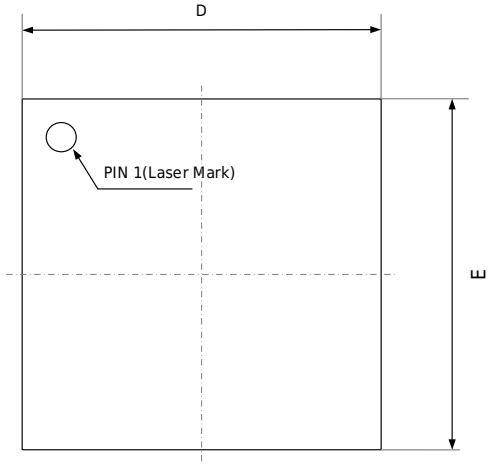
- *Dimensions “D1” and “E1” do not include mold flash.*

QFN60 packaging

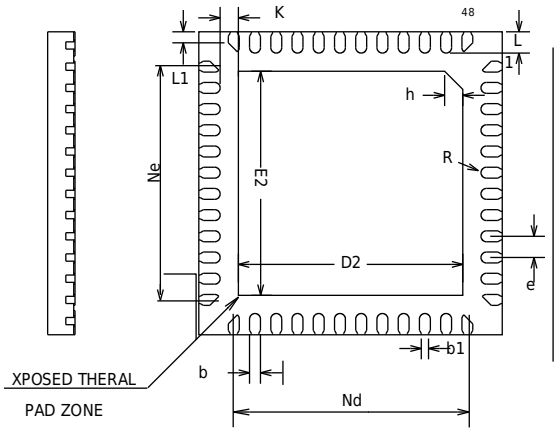


Symbol	7x7 Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.547REF	
b	0.15	0.20	0.25
b1		0.14REF	
c		0.20REF	
c1		0.255REF	
c2		0.18REF	
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
Nd		5.60BSC	
e		0.40BSC	
E	6.90	7.00	7.10
E2	5.50	5.60	5.70
Ne		5.60BSC	
L	0.35	0.40	0.45
K	0.25	0.30	0.35
h	0.30	0.35	0.40

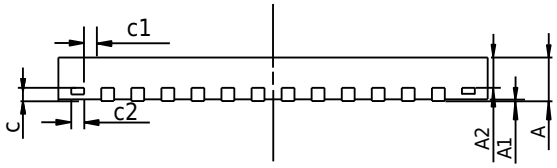
QFN48 packaging



TOP VIEW



BOTTOM VIEW

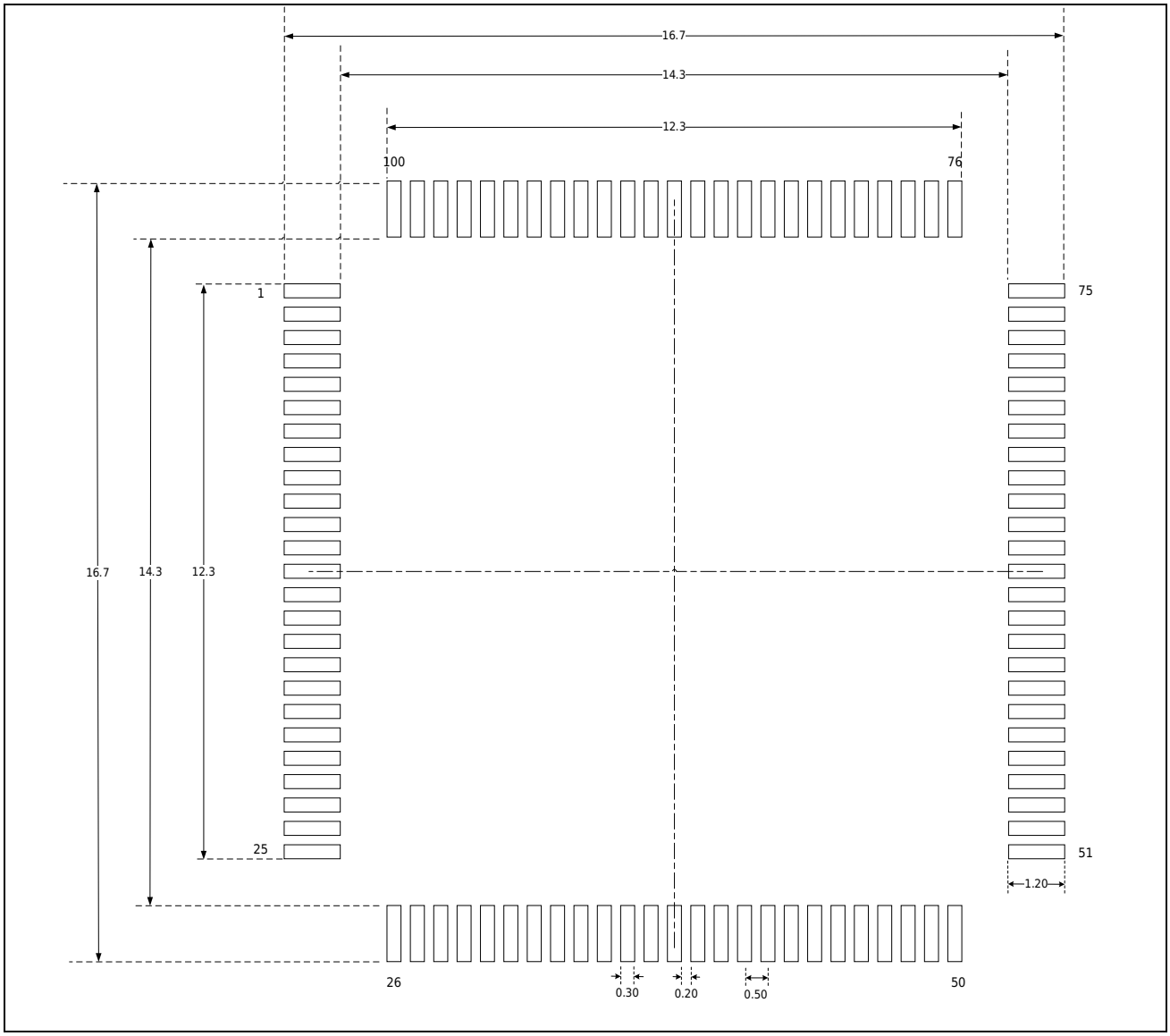


SIDE VIEW

Symbol	5x5 Millimeter		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A2		0.40REF	
b	0.13	0.18	0.23
b1		0.12REF	
c	0.10	0.15	0.20
c1		0.145REF	
c2		0.140REF	
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
e		0.35BSC	
Ne		3.85BSC	
Nd		3.85BSC	
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.30	0.35	0.40
L1	0.13	0.18	0.23
h	0.25	0.30	0.35
L/F Carrier Size		154 x 154	

4.2 Schematic Diagram of Pad

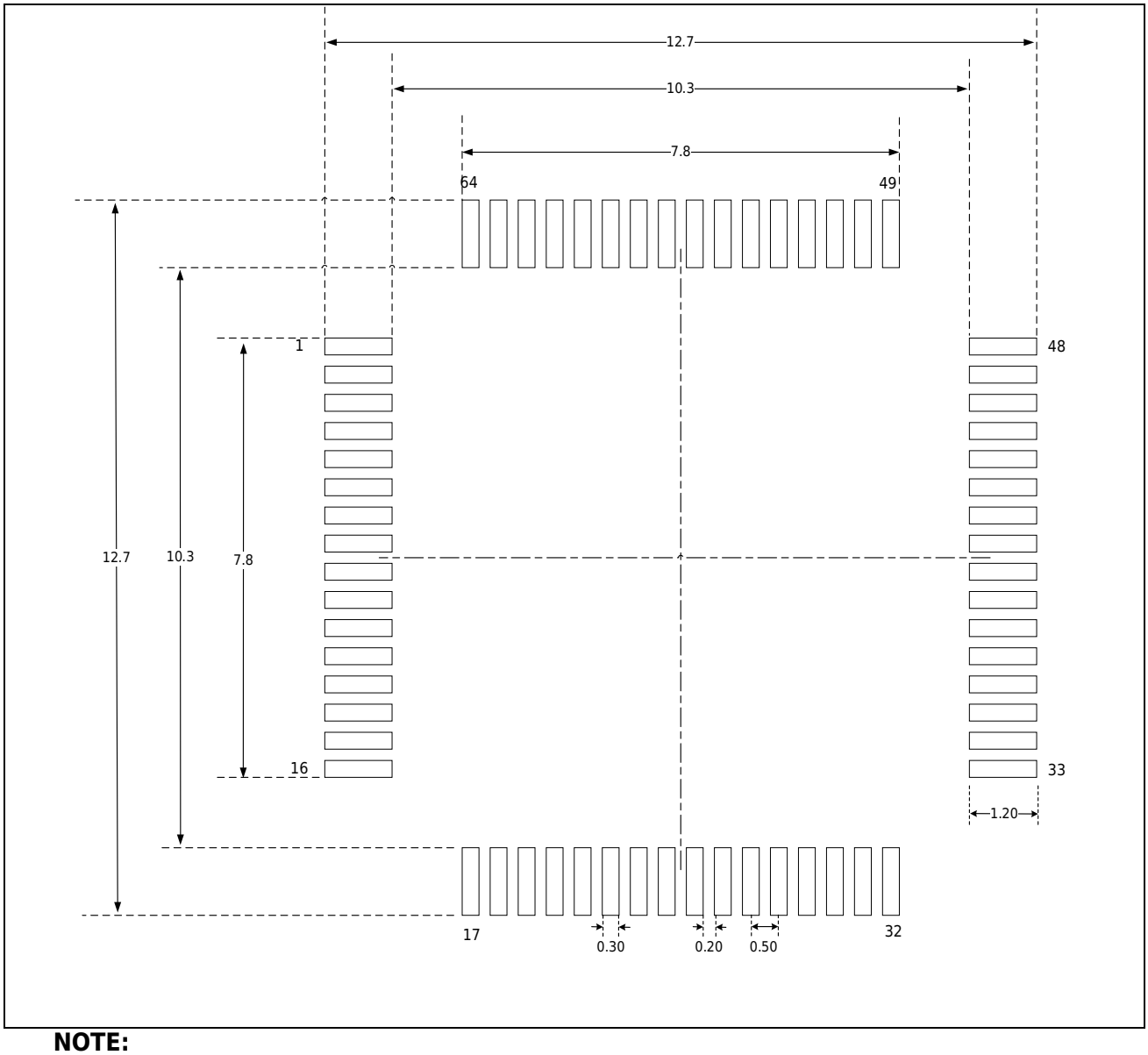
LQFP100 packaging (14mm x 14mm)



NOTE:

- *Dimensions are expressed in millimeters.*
- *Dimensions are for reference only.*

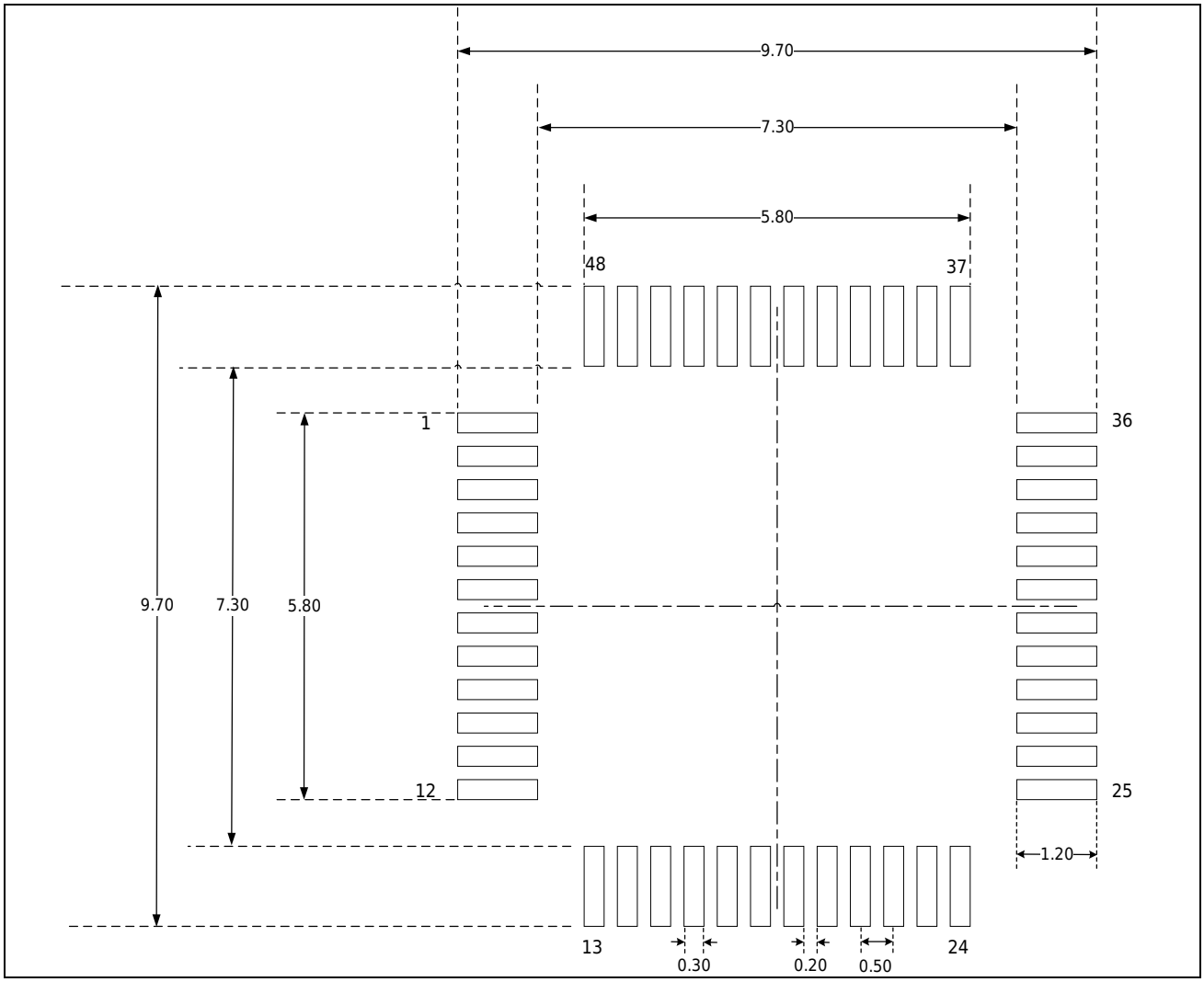
LQFP64 packaging (10mm x 10mm)



NOTE:

- *Dimensions are expressed in millimeters.*
- *Dimensions are for reference only.*

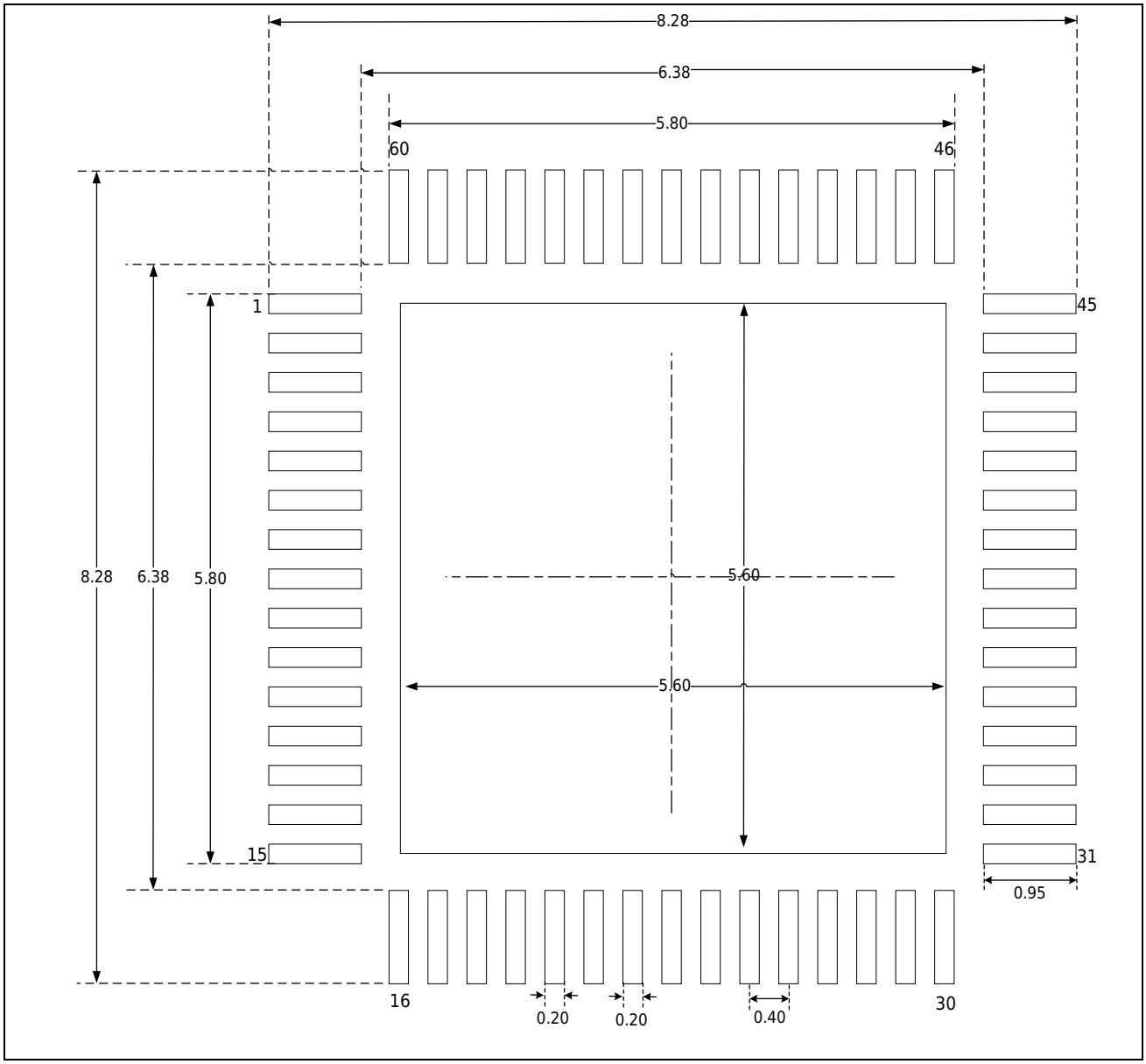
LQFP48 Packaging (7mm x 7mm)



NOTE:

- *Dimensions are expressed in millimeters.*
- *Dimensions are for reference only.*

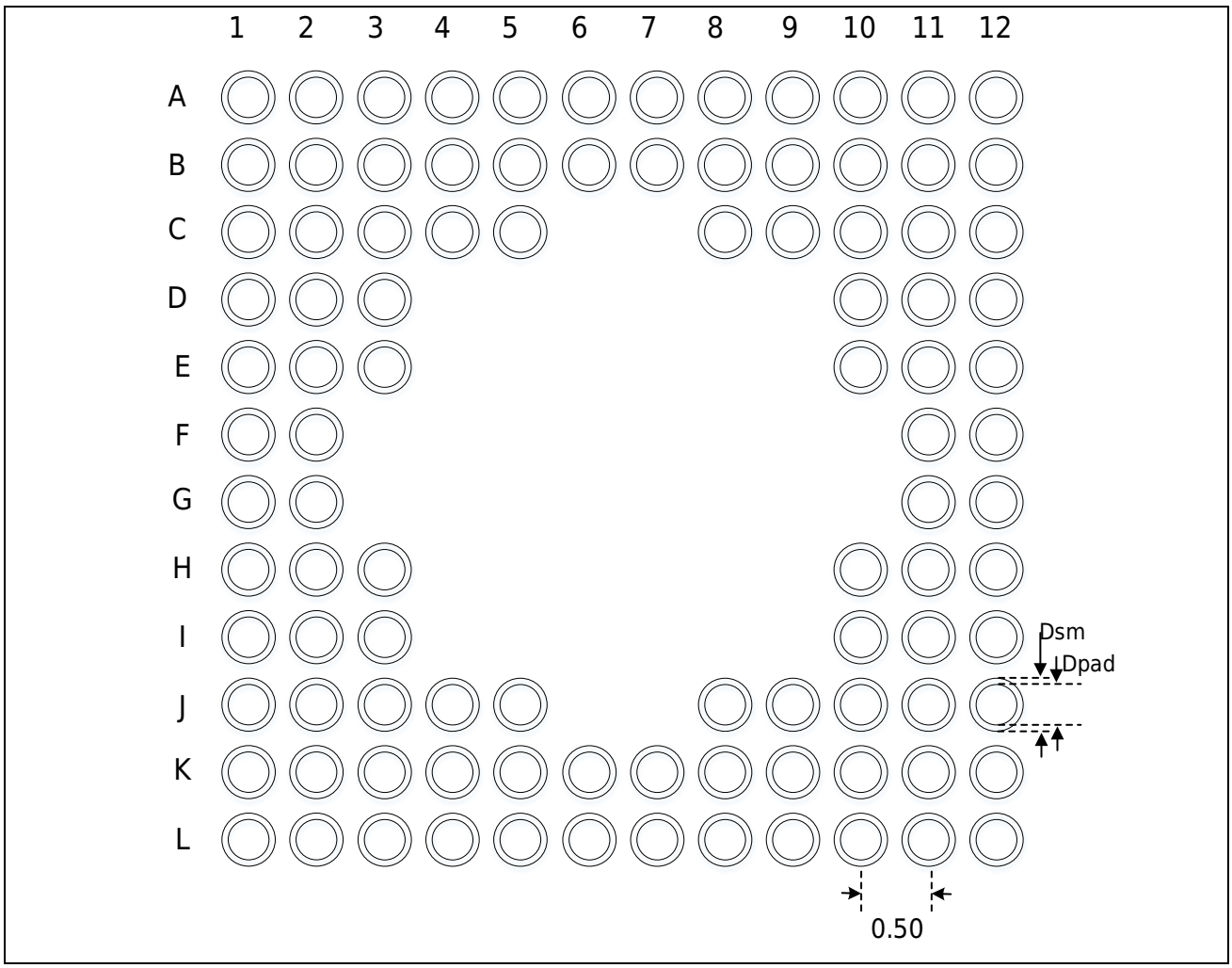
QFN60 Packaging (7mm x 7mm)



NOTE:

- *Dimensions are expressed in millimeters.*
- *Dimensions are for reference only.*

VFBGA100 Packaging (7mm x 7mm)



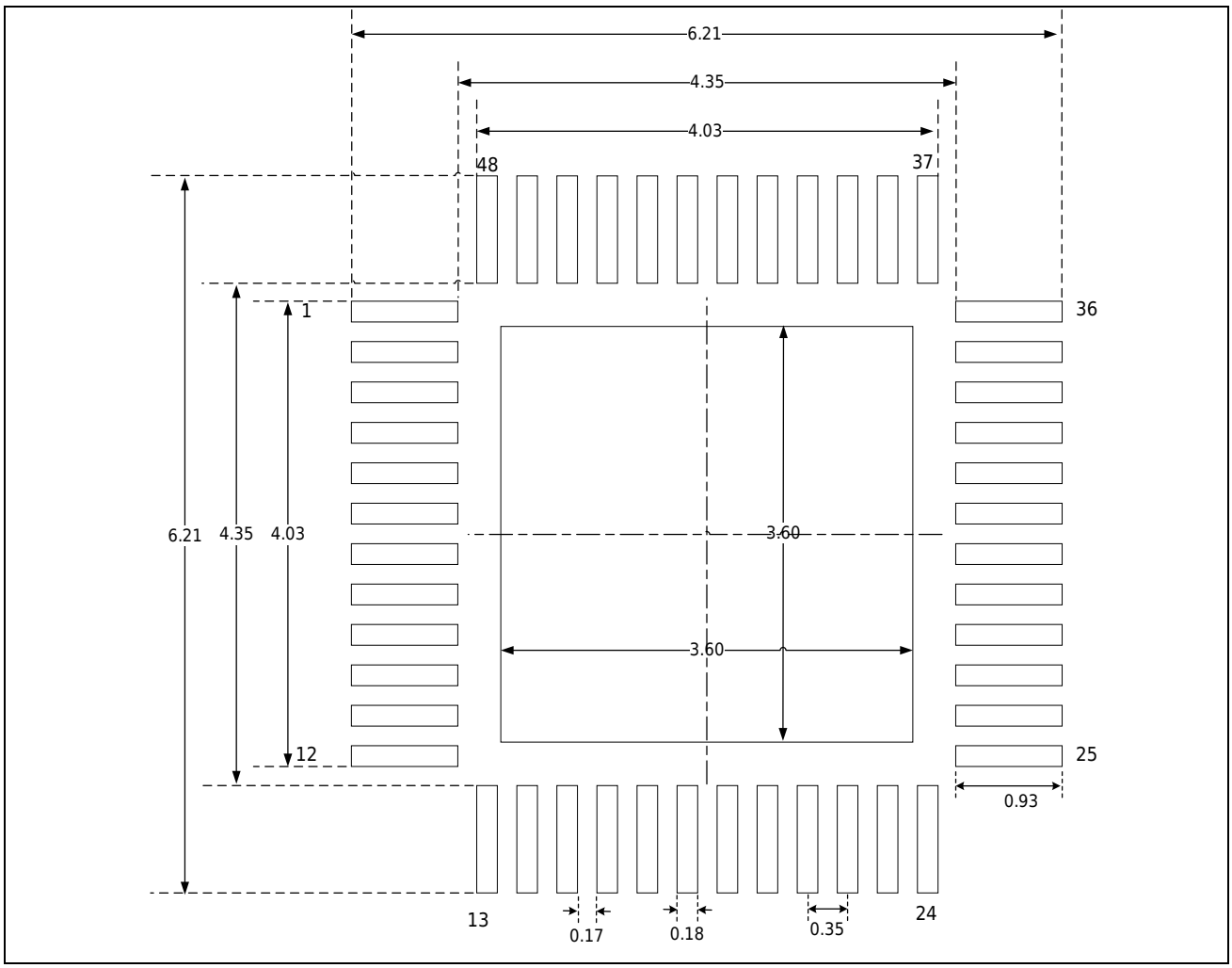
NOTE:

- *Dimensions are expressed in millimeters.*
- *Dimensions are for reference only.*

VBGA100 recommended PCB design rules (0.5mm pitch)

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.240 mm
Dsm	0.340 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.240 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

QFN48 Packaging (5mm x 5mm)



NOTE:

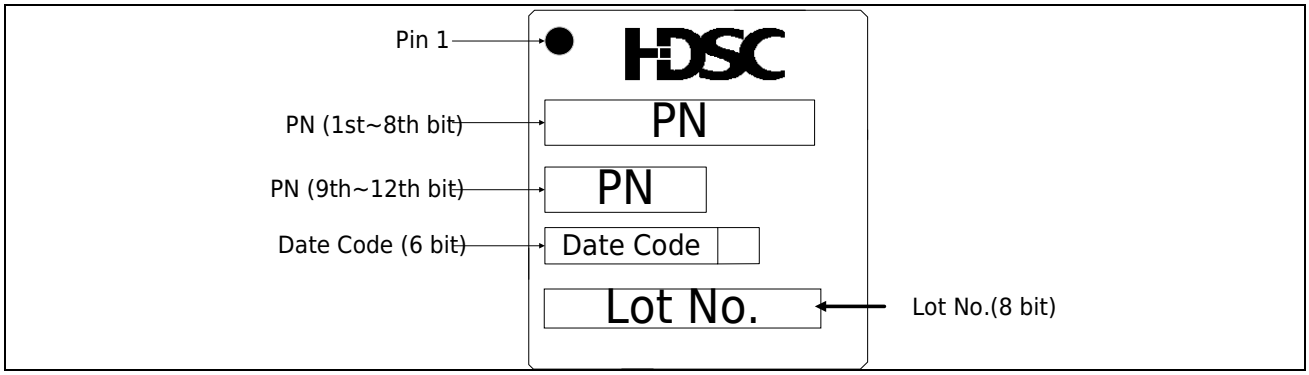
- *Dimensions are expressed in millimeters.*
- *Dimensions are for reference only.*

4.3 Silkscreen Instructions

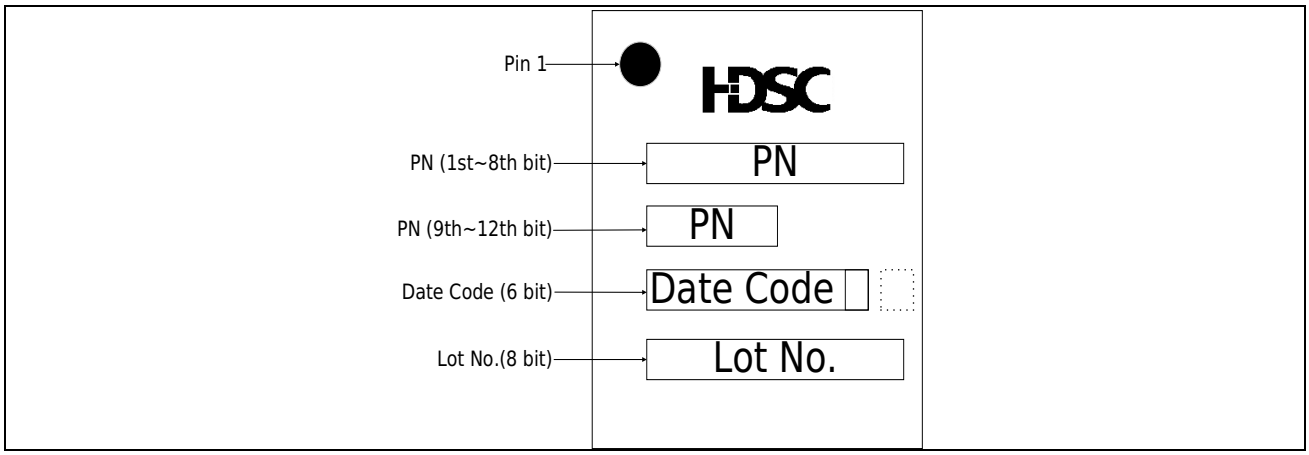
The position and information of Pin 1 printed on the front of each package are given below.

LQFP100 packaging (14mmx14mm) / LQFP64 packaging (10mmx10mm)

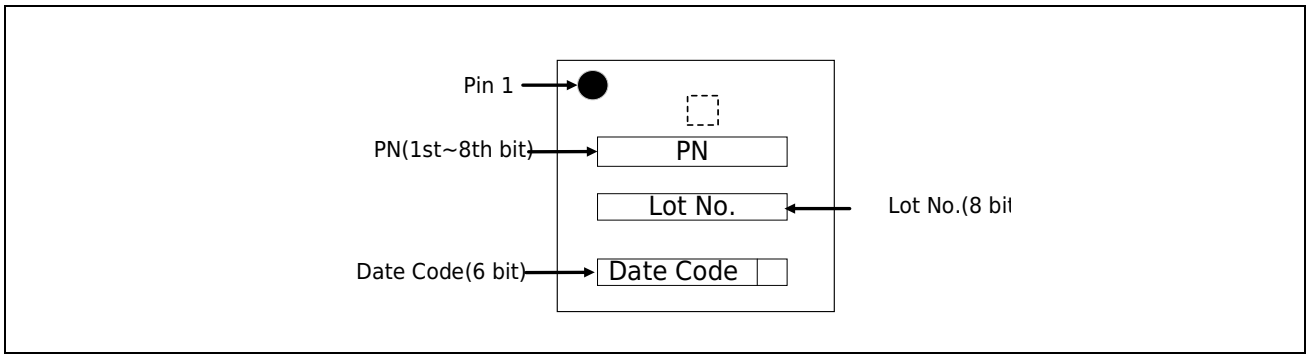
LQFP48 packaging (7mmx7mm)



QFN60 packaging (7mmx7mm) / VFBGA100 packaging (7mm x 7mm)



QFN48 packaging (5mmx5mm)



Note:

– The blank boxes in the above figure indicate optional marks related to production, which are not explained in this section.

4.4 Packaging Thermal Resistance Coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature T_j (℃) of the chip surface can be calculated according to the following formula:

$$T_j = T_A + (P_D \times \theta_{JA})$$

- T_A refers to the working environment temperature when the packaged chip is working, the unit is ℃;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is ℃/W;
- P_D is equal to the sum of a chip's internal power consumption (P_{INT}) and the power consumption generated by its I/O pins during operation ($P_{I/O}$), with the unit of W.

  $P_{INT} = I_{CC} \times V_{CC}$

  $P_{I/O} = \Sigma(V_{OL} \times I_{OL}) + \Sigma((V_{CC} - V_{OH}) \times I_{OH})$

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_J of the chip.

Table 4-1 Thermal resistance coefficient table for each package

Package Type and Size	Thermal Resistance Junction-ambient Value (θJA)	Unit
LQFP100 14mm x 14mm / 0.5mm pitch	50 +/- 10 %	℃/W
LQFP64 10mm x 10mm / 0.5mm pitch	65 +/- 10 %	℃/W
LQFP48 7mm x 7mm / 0.5mm pitch	75 +/- 10 %	℃/W
QFN60 7mm x 7mm / 0.4mm pitch	30 +/- 10 %	℃/W
QFN48 5mm x 5mm / 0.35mm pitch	42 +/- 10 %	℃/W

5 Ordering Information

Product	HC32F460JEUA-QFN48TR	HC32F460JETA-LQFP48	HC32F460KEUA-QFN60TR	HC32F460KETA-LQFP64	HC32F460PETB-LQFP100	HC32F460PEHB-VFBGA100	HC32F460JCTA-LQFP48	HC32F460KCTA-LQFP64	HC32F460PCTB-LQFP100
Main frequency (MHz)	200	200	200	200	200	200	200	200	200
Kernel	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4
Flash (KB)	512	512	512	512	512	512	256	256	256
RAM (KB)	192	192	192	192	192	192	192	192	192
OTP (B)	960	960	960	960	960	960	960	960	960
Package (mm*mm)	QFN48 (5*5) e=0.35	LQFP48 (7*7) e=0.5	QFN60 (7*7) e=0.4	LQFP64 (10*10) e=0.5	LQFP100 (14*14) e=0.5	VFBGA100 (7*7) e=0.5	LQFP48 (7*7) e=0.5	LQFP64 (10*10) e=0.5	LQFP100 (14*14) e=0.5
GPIO	38	38	50	52	83	83	38	52	83
Minimum Operating Voltage	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8
Maximum Operating Voltage	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6
16-bit Timer	11	11	11	11	11	11	11	11	11
Motor Control Timer	3	3	3	3	3	3	3	3	3
12-bit ADC Conversion Unit	2	2	2	2	2	2	2	2	2
Number of 12-bit ADC Channels	10	10	15	16	16	16	10	16	16
Comparator	3	3	3	3	3	3	3	3	3
Programmable Gain Amplifier (PGA)	1	1	1	1	1	1	1	1	1
SPI	4	4	4	4	4	4	4	4	4
QUADSPI	1	1	1	1	1	1	1	1	1
I^2S	4	4	4	4	4	4	4	4	4
I^2C	3	3	3	3	3	3	3	3	3
U(S)ART	4	4	4	4	4	4	4	4	4
CAN	1	1	1	1	1	1	1	1	1
SDIO	2	2	2	2	2	2	2	2	2
全速USB OTG	1	1	1	1	1	1	1	1	1
DMA	8	8	8	8	8	8	8	8	8
DCU	4	4	4	4	4	4	4	4	4
PVD	√	√	√	√	√	√	√	√	√
AES128	√	√	√	√	√	√	√	√	√
SHA256	√	√	√	√	√	√	√	√	√
TRNG	√	√	√	√	√	√	√	√	√
CRC	√	√	√	√	√	√	√	√	√
KEYSCAN	√	√	√	√	√	√	√	√	√
RTC	√	√	√	√	√	√	√	√	√
FLASH Physical Encryption	√	√	√	√	√	√	√	√	√
Shipment Configuration	Tape and Reel	Tray	Tape and Reel	Tray	Tray	Tray	Tray	Tray	Tray

Before ordering, please contact the sales window for the latest mass production information.

Version Revision History

Version Number	Revision Date	Modify the content
Rev1.00	2019/11/12	First edition release.
Rev1.10	2020/01/10	1) Added a description of the 256KB product throughout the document. 2) Added a description of the VFBGA package throughout the document. 3) Revised the maximum current value for Power-down mode at 105 °C in the Electrical Characteristics section. 4) Updated the silk screen drawing description.
Rev1.20	2020/08/26	1) Added description of the Ultra-High-Speed operating mode; updated CoreMark/DMIPS scores; added description of the Ultra-High-Speed mode. Updated the functional block diagram. 2) Added the 256KB product variant to the pin configuration diagram(s). 3) Added the bond pad diagram and package thermal resistance values. 4) Added BOR/PVD characteristics and current consumption characteristics in Ultra-High-Speed mode. 5) Updated the JTAG/SWJ debug port pin descriptions.
Rev1.30	2021/12/10	1) Updated the declaration: Add QFN48/60 A2/c1/c2 dimensions under package dimensions, and revise the data retention period for flash memory. 2) External main clock crystal: Changed (4-24MHz) to (4-25MHz). 3) Modified the functional block diagram: Change USB_DMA to USBFS_DMA; Change I2S_1 to I2S_2; add AOS. 4) 1.4.6 addresses: changed 0x00000400H~0x0000041FH to 0x0000_0400~0x0000_041F changed 0x00000408~0x0000041F to 0x0000_0408~0x0000_041F 5) Added an introduction description for "Automatic Operation System (AOS)"; update the description for "Keyboard Scan (KEYSCAN)." 6) Terminology corrections and description optimizations. 7) Modified the recommended bypass capacitor configuration for analog power pins in the power supply schematic: removed the 10nF capacitor, and changed the 10μF capacitor to 1 μF. 8) Added parameter entries in the reset and power control module characteristics table: TIPVD1/ TIPVD2/ TINRST/ TRSTBOR; changed TRSTTAO to TRSTPOR. 9) 3.3.12: Added CAN2.0B interface characteristics description.

Version Number	Revision Date	Modify the content
		10) In PLL characteristics, changed the maximum value of f_{PLL_IN} from 24 MHz to 25 MHz, and added Jitter characteristics. 11) 3.3.16.1: Changed the maximum value of f_{XTAL_EXT} to 25MHz. 12) 3.3.16.2: Added accuracy specifications for the external high-speed oscillator XTAL; revised descriptions related to C_{L1} and C_{L2}. 13) 3.3.16.3: Added accuracy specifications for the external low-speed oscillator XTAL32; revised descriptions related to C_{L1} and C_{L2}.
Rev1.40	2022/03/09	Company Logo Updated.
Rev1.41	2022/03/29	1) 3.3.13 USB Interface Characteristics: Removed the MAX and MIN values for R_{PD} and added a TYP value of 15kΩ; 3.3.16 $t_{SU\ (XTAL)}$ Startup Time: Removed the MAX value and added a TYP value. 2) 4.1 LQFP100/LQFP64/LQFP48: Modified the MAX value for `b` to 0.27.
Rev1.42	2022/09/14	1) In the pin configuration diagrams for all packages: Changed "PH0/ XTAL_IN" to "PH0/ XTAL_EXT/ XTAL_OUT"; Changed "PH1/ XTAL_OUT" to "PH1/ XTAL_IN"; Modified the style of the QFN60 pin configuration diagram; Added a new pin configuration diagram for QFN48. 2.2 Changed "PH0/ XTAL_IN" to "PH0/ XTAL_EXT/ XTAL_OUT" and "PH1/ XTAL_OUT" to "PH1/ XTAL_IN". 2.3 Changed "XTAL_OUT" to "XTAL_EXT/ XTAL_OUT" and added the note: "XTAL_EXT: External clock input". 2) 3.3.16.1 Changed "XTAL_IN" to "XTAL_EXT"; 3.3.16.2 In Figure 3-17, swap the pin names "XTAL_IN" and "XTAL_OUT"; 3.3.18 In Figure 3-21, changed the 10 μF capacitor value to 1 μF.
Rev1.50	2023/09/27	1) Product Characteristics: Corrected the ADC speed. 2) 1 Introduction: Corrected the ADC speed. 3) 1.4.16: Corrected the ADC speed. 4) 2.4 Table 2-6: Supplement the pin descriptions. 5) 3.2: Corrected the temperature in the thermal characteristics. 6) 3.3.7 Corrected the parameters in Table 3-19 I/O Static Characteristics. 7) 3.3.10 Corrected the parameters in Table 3-24 I2C Electrical Characteristics. 8) 3.3.11 Corrected the connection diagram in Table 3-25 SPI Electrical Characteristics and add an SPI timing diagram.

Version Number	Revision Date	Modify the content
		9) 4.4 Corrected the description of the package thermal resistance coefficient.
Rev1.60	2025/01/17	1) Product Characteristics: Corrected the frequency of the internal low-speed RC oscillator. 2) Table 2-6: Modified the pin description. 3) 3.2: Revised the description in Table 3-3 (Current Characteristics), changed "Maximum Injection Current " to " Maximum ". 4) 3.3.1: Added a note to Table 3-5. 5) 3.3.10.2: Removed the version information from the condition column in Table 3-31. 6) 3.3.24: Updated Figure 3-31 and its accompanying description. 7) Modified the package dimensions section.
Rev1.61	2026/02/12	1) Features: Optimized the crystal oscillator name, changing "main" and "auxiliary" to "high speed" and "low speed". 2) Pin configuration diagram and 2.2 Pin function table: Corrected the names of XTAL32_IN/OUT. 3) Pin function description: Optimized the crystal oscillator name, changing "main" and "auxiliary" to "high speed" and "low speed". 4) 3.3.1 General operating conditions: Optimized the description of precautions. 5) 3.3.23 Optimized the flash memory erase/write cycles and data storage period in Table 3-56.