InnoSwitch4-Pro Family

Digitally Controllable Off-Line CV/CC ZVS Flyback Switcher IC with 750 V PowiGaN, Active Clamp Drive and Synchronous Rectification

Product Highlights

Highly Integrated, Compact Footprint

- Quasi-Resonant (QR) or zero voltage switching (ZVS) flyback controller when paired with ClampZero™ (active clamp IC)
- Unique control algorithm to enable ZVS in both DCM and CCM
- Robust 750 V PowiGaN™ primary switch
- Steady-state switching frequency up to 140 kHz minimizes transformer size
- Synchronous rectification driver and secondary-side sensing
- Integrated FluxLink™, HIPOT-isolated, feedback link
- Drives low-cost N-channel FET series load switch
- Integrated 3.6 V supply for external MCU

Digitally Controlled via I²C Interface

- Precise CV, CC, CP Control
- Dynamic adjustment of power supply voltage and current
- Selectable DCM-only operation to reduce SR FET voltage stress
- Optimized command set to reduce I²C traffic
- Telemetry for power supply status and fault monitoring

EcoSmart™ – Energy Efficient

- Efficiency up to 95%
- Less than 30 mW no-load including line sense and MCU

Advanced Protection / Safety Features

- Series load switch short-circuit protection
- Disable output fault response
- Fast input line UV/OV protection
- Programmable Output OV/UV fault detection and response
- Open SR FET gate detection
- Hysteretic thermal shutdown
- Programmable watchdog timer for system faults

Full Safety and Regulatory Compliance

- Reinforced isolation >4000 VAC
- 100% production HIPOT testing
- UL1577 isolation voltage 4000 VAC (max) and TUV (EN62368) and CQC (G4943.1) safety approved

Green Package

- Halogen free and RoHS compliant

Applications

- High density power adapters
- Multiprotocol adapters including USB PD + PPS, QC, VOOC, VFC, SCP
- Direct-charge mobile device chargers
- Multi-chemistry tool and general purpose battery chargers
- Adjustable CV and CC LED ballast

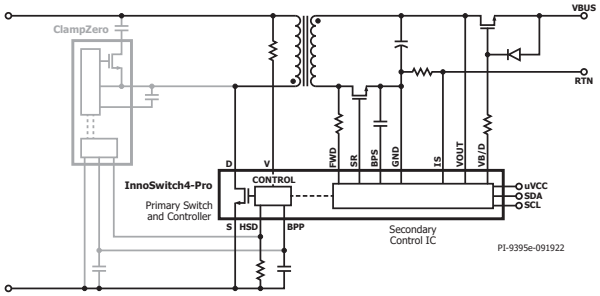


Figure 1a. Typical Application – Active Clamp Flyback. (With ClampZero)

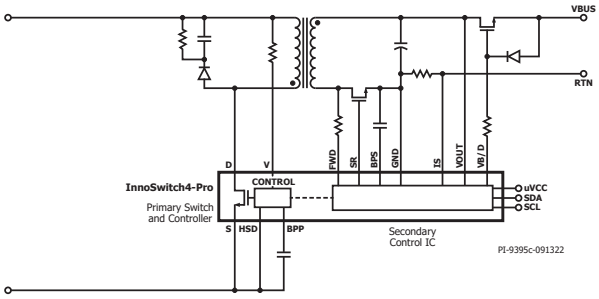


Figure 1b. Typical Application – QR Flyback.

Output Power Table[1] – ACF Mode

Product[4,5]	230 VAC ± 15%		85-265 VAC	
	Adapter[2]	Open Frame[3]	Adapter[2]	Open Frame[3]
INN4373F	70 W	75 W	60 W	70 W
INN4374F	85 W	90 W	75 W	85 W
INN4375F	90 W	100 W	80 W	90 W
INN4376F	115 W	125 W	100 W	115 W
INN4377F	135 W	145 W	115 W	135 W
Product[4,5]	385 VDC (PFC Input)			
	Adapter[2]		**Open Frame[3]**	
INN4474F	155 W		170 W	
INN4475F	160 W		180 W	
INN4476F	180 W		200 W	
INN4477F	200 W		220 W	

Output Power Table[1] – QR Mode

Product[4,5]	230 VAC ± 15%		85-265 VAC	
	Adapter[2]	Open Frame[3]	Adapter[2]	Open Frame[3]
INN4574F	80 W	90 W	65 W	85 W
INN4575F	90 W	100 W	75 W	90 W
INN4576F	105 W	125 W	80 W	115 W
INN4577F	125 W	145 W	90 W	135 W
Product[4,5]	385 VDC (PFC Input)			
	Adapter[2]		**Open Frame[3]**	
INN4674F	145 W		170 W	
INN4675F	155 W		180 W	
INN4676F	170 W		200 W	
INN4677F	185 W		220 W	

Table 1. Output Power Table. (See Table 1 Notes on page 2)

Description

The InnoSwitch™4-Pro family of ICs substantially reduces the size of power adapters. Switching frequency of up to 140 kHz and a very high level of integration combine to reduce the component volume and PCB board area required by a typical adapter implementation.

InnoSwitch4-Pro interfaces seamlessly with the ClampZero family of active clamp ICs to achieve zero voltage switching in both continuous and discontinuous conduction modes. Alternatively, InnoSwich4-Pro can operate in QR mode using an RCD clamp with the appropriated part number choice. Overall system efficiency exceeds 95%, allowing designers to eliminate heat sinks, spreaders and potting materials for thermal management, further reducing size, component cost and manufacturing complexity. The integration of PowiGaN primary switch and controller, isolated feedback and secondary controller with an I²C interface simplifies the development and manufacturing of fully programmable, highly efficient power supplies.

Figure 2a. High Creepage, Safety-Compliant InSOP-T28D Package.

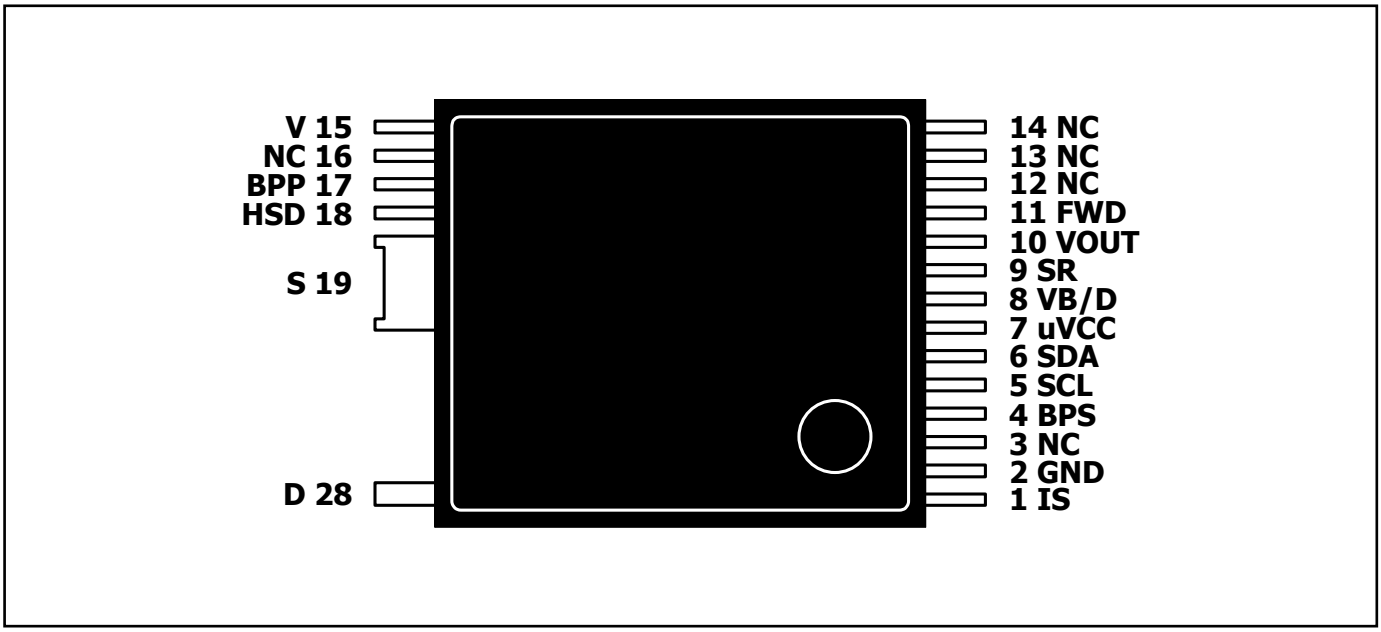


Figure 2b. Pin Configuration.

Output Power Table 1 Notes

1. Maximum output power is dependent on the design, with maximum IC package temperature kept <125 °C.
2. Minimum continuous power in a typical non-ventilated enclosed typical size adapter measured at 40 °C ambient.
3. Minimum peak power capability.
4. F Package: InSOP-T28D.
5. INN43xx/INN45xx series optimized for universal AC input designs.
   INN44xx/INN46xx series optimized for peak power designs with PFC input.

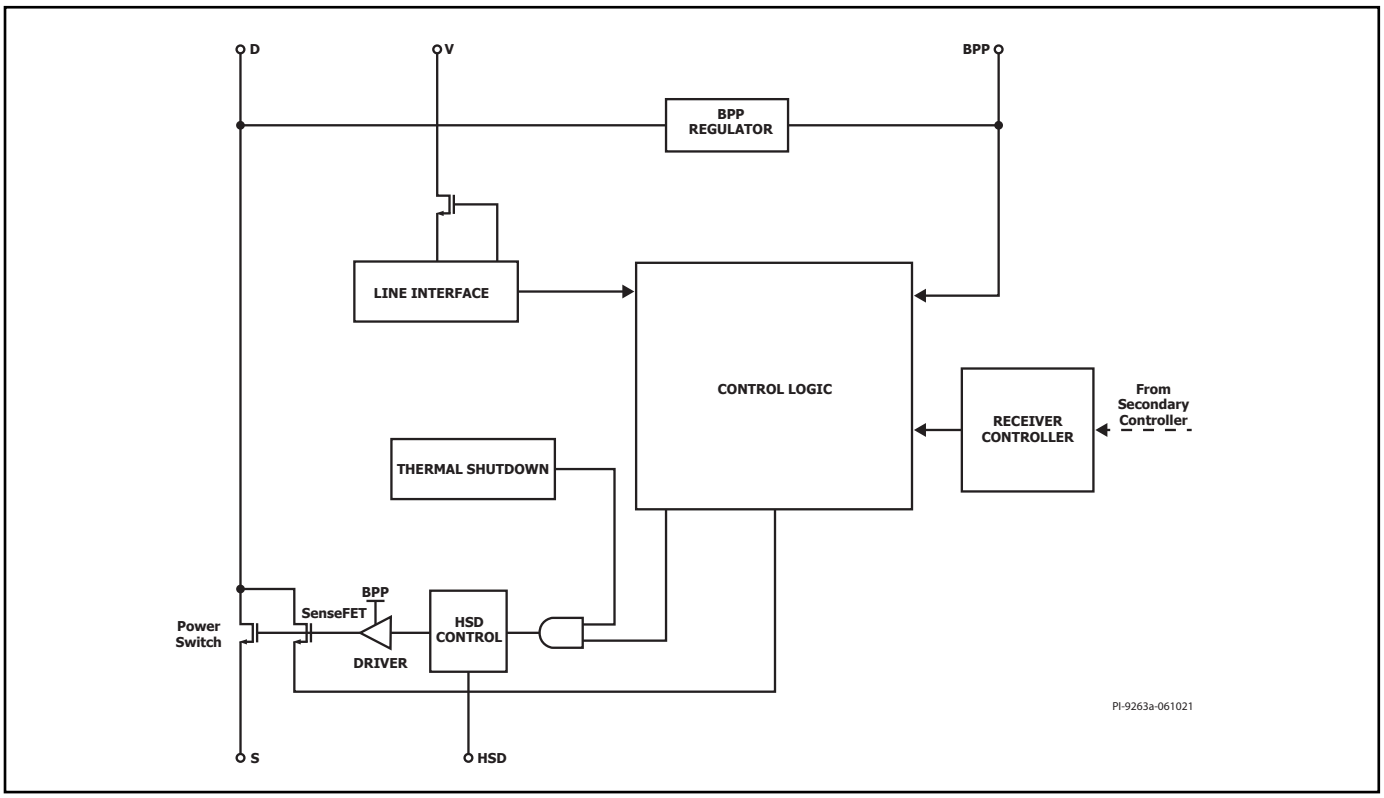


Figure 3. Primary Controller Block Diagram.

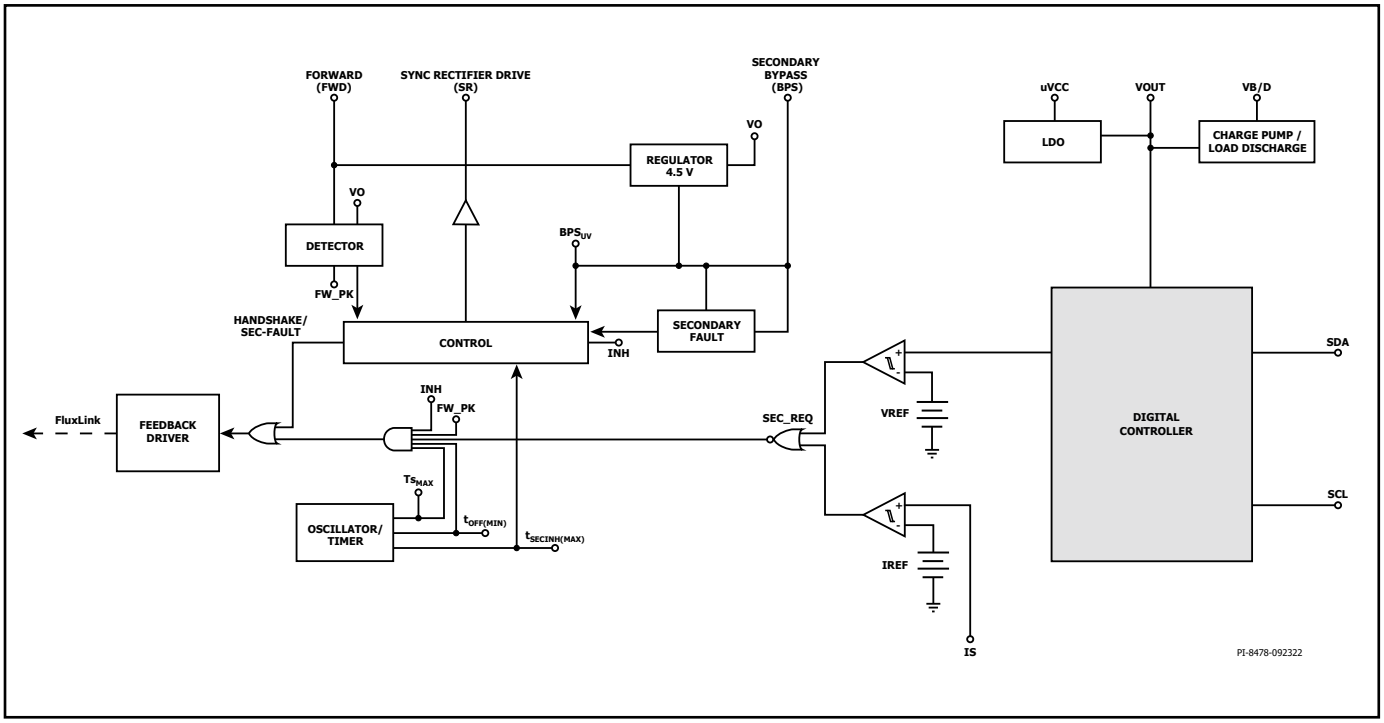


Figure 4. Secondary Controller Block Diagram.

Pin Functional Description

ISENSE (IS) Pin (Pin 1)
Connection to the power supply return output terminals. An external current sense resistor should be connected between this and the SECONDARY GROUND pin.

SECONDARY GROUND (GND) (Pin 2)
Ground reference for the secondary IC. Note this is not the power supply output ground due to the presence of the sense resistor between this and the ISENSE pin.

NC Pin (Pin 3)
Leave open. Should not be connected to any other pins.

SECONDARY BYPASS (BPS) Pin (Pin 4)
It is the connection point for an external bypass capacitor for the secondary IC supply.

I²C Clock (SCL) Pin (Pin 5)
I²C serial communication protocol clock line sourced by the Bus master.

I²C Serial Data (SDA) Pin (Pin 6)
I²C serial communication protocol data line sourced by the Bus master.

External VCC Supply (uVCC) Pin (Pin 7)
This is 3.6 V supply for an external controller.

VBUS Series Switch Drive and Load Discharge (VB/D) Pin (Pin 8)
VBUS enable and driver for NMOS gate for VOUT to VBUS series pass FET(s). This pin is also used to discharge output load voltage (VBUS).

SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 9)
Gate driver output and connection to external SR FET gate.

OUTPUT VOLTAGE (VOUT) Pin (Pin 10)
Connected directly to the output voltage providing current for the secondary IC and sense for output voltage regulation. This pin also has an active/programmable pull-down current source.

FORWARD (FWD) Pin (Pin 11)
The connection point to the switching node of the transformer output winding providing information on the primary switch timing plus providing power for the secondary IC when VOUT is below a threshold value.

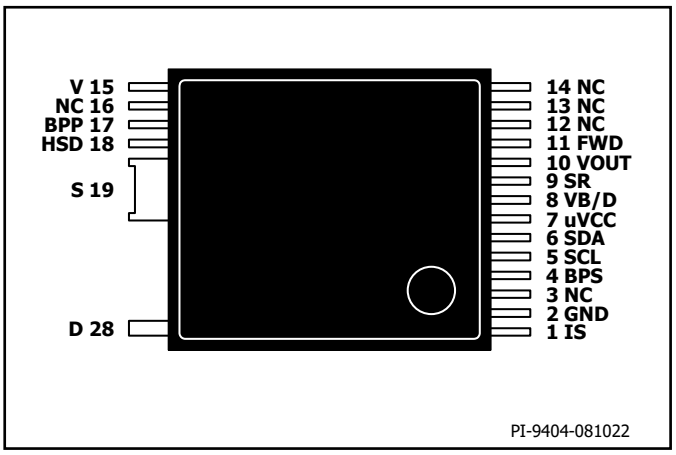


Figure 5. Pin Configuration.

NC Pin (Pin 12-14)
Leave open. Should not be connected to any other pins.

UNDER/OVER INPUT VOLTAGE (V) Pin (Pin 15)
A high-voltage pin connected to the AC or DC side of the input bridge for detecting under and overvoltage conditions at the power supply input. When connected to the AC side of the bridge, a high-voltage switch is opened when not sensing to reduce power consumption. This pin should be tied to GND to disable UV/OV protection.

NC Pin (Pin 16)
Leave open or connect to SOURCE pin or BPP pin.

PRIMARY BYPASS (BPP) Pin (Pin 17)
The connection point for an external bypass capacitor for the primary IC supply. This is also the ILIM selection pin for choosing standard ILIM or ILIM+1. Must be connected to BP1 pin of ClampZero.

HSD Pin (Pin 18)
High-side drive signal for active clamp. Must be connected to IN pin of ClampZero. In QR mode HSD pin is tied to ground.

SOURCE (S) Pin (Pin 19)
These pins are the power switch source connection. It is also ground reference for primary BYPASS pin.

DRAIN (D) Pin (Pin 28)
This pin is the power switch drain connection.

InnoSwitch4-Pro Functional Description

The InnoSwitch4-Pro combines a high-voltage power switch, along with both primary-side and secondary-side controllers in one device.

The architecture incorporates a novel inductive coupling feedback scheme (FluxLink) using the package lead frame and bond wires to provide a safe, reliable, and cost-effective means to transmit accurate, output voltage and current information from the secondary controller to the primary controller.

The InnoSwitch4-Pro secondary controller consists of a transmitter circuit that is magnetically coupled to the primary receiver, an I^2C interface to control power supply parameters and telemetry functions, a 4.5 V regulator on the SECONDARY BYPASS pin, synchronous rectifier FET driver, oscillator and timing functions, and a host of integrated protection features.

INN437xF and INN447xF
The primary controller on InnoSwitch4-Pro is a zero voltage switching (ZVS) flyback controller that has the ability to operate in continuous conduction mode (CCM), and discontinuous conduction mode (DCM) with virtually no switching loss. The controller uses both variable frequency and variable current limit control scheme. The primary controller consists of a frequency jitter oscillator, a receiver circuit magnetically coupled to the secondary controller, a current limit controller, 5 V regulator on the PRIMARY BYPASS pin, bypass overvoltage detection circuit, a lossless input line sensing circuit, current limit selection circuitry, over-temperature protection, leading edge blanking and power switch.

INN457xF and INN467xF
The primary controller on InnoSwitch4-Pro is a Quasi-Resonant (QR) flyback controller that has the ability to operate in continuous conduction mode (CCM). The controller uses both variable frequency and variable current control schemes. The primary controller consists of a frequency jitter oscillator; a receiver circuit magnetically coupled to the secondary controller, a current limit controller, 5 V regulator on the PRIMARY BYPASS pin, bypass overvoltage detection circuit, a lossless input line sensing circuit, current limit selection circuitry, over-temperature protection and leading edge blanking.

Figure 3 and Figure 4 show the functional block diagrams of the primary and secondary controller with the most important features.

Primary Controller

InnoSwitch4-Pro is a variable frequency controller allowing CCM/CrM/DCM operation for enhanced efficiency and extended output power capability.

PRIMARY BYPASS Pin Regulator
The PRIMARY BYPASS pin has an internal regulator that charges the PRIMARY BYPASS pin capacitor to V_{BPP} by drawing current from the DRAIN pin whenever the power switch is off. The PRIMARY BYPASS pin is the internal supply voltage node. When the power switch is on, the device operates from the energy stored in the PRIMARY BYPASS pin capacitor.

In addition, a shunt regulator clamps the PRIMARY BYPASS pin voltage to V_{SHUNT} when current is provided to the PRIMARY BYPASS pin through an external resistor. This allows the InnoSwitch4-Pro to be powered externally through a bias winding, decreasing the no-load consumption to less than 30 mW in a 5 V output design.

Primary Bypass ILIM Programming
InnoSwitch4-Pro ICs allows the user to adjust current limit (ILIM) settings through the selection of the PRIMARY BYPASS pin capacitor value. A ceramic capacitor can be used.

There are 2 selectable capacitor sizes – 0.47 μF and 4.7 μF for setting standard and increased ILIM settings respectively.

Primary Bypass Undervoltage Threshold
The PRIMARY BYPASS pin undervoltage circuitry disables the power switch when the PRIMARY BYPASS pin voltage drops below ~4.5 V ($V_{BPP} – V_{BP(H)}$) in steady-state operation. Once the PRIMARY BYPASS pin voltage falls below this threshold, it must rise to V_{SHUNT} to re-enable turn-on of the power switch.

Primary BYPASS Pin Overvoltage Function
The PRIMARY BYPASS pin has an optional latching OV protection feature. A Zener diode in parallel with the resistor in series with the PRIMARY BYPASS pin capacitor is typically used to detect an overvoltage on the primary bias winding and activate the protection mechanism. In the event that the current into the PRIMARY BYPASS pin exceeds I_{SD}, the device will latch-off or disable the power switch switching for a time $t_{AR(OFF)}$, after which time the controller will restart and attempt to return to regulation.

VOUT OV protection is also included as an integrated feature on the secondary controller (see Output Voltage Protection).

Over-Temperature Protection
The thermal shutdown circuitry senses the primary switch die temperature. The threshold is set to T_{SD} with either a hysteretic or latch-off response.

Hysteretic response: If the die temperature rises above the threshold, the power switch is disabled and remains disabled until the die temperature falls by $T_{SD(H)}$ at which point switching is re-enabled. A large amount of hysteresis is provided to prevent over-heating of the PCB due to a continuous fault condition.

Latch-off response: If the die temperature rises above the threshold the power switch is disabled. The latching condition is reset by bringing the PRIMARY BYPASS pin below $V_{BPP(RESET)}$ or by going below the UNDER/OVER INPUT VOLTAGE pin UV (I_{UV-}) threshold.

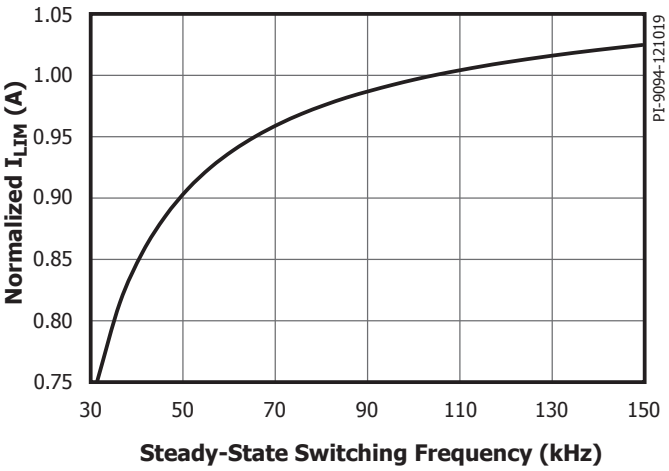


Figure 6. Normalized Primary Current vs. Frequency.

Current Limit Operation
The primary-side controller has a current limit threshold ramp that is inversely proportional to the time from the end of the previous primary switching cycle (i.e. from the time the primary switch turns off at the end of a switching cycle).

This characteristic produces a primary current limit that increases as the switching frequency (load) increases (Figure 6).

This algorithm enables the most efficient use of the primary switch with the benefit that this algorithm responds to digital feedback information immediately when a feedback switching cycle request is received.

At full load, switching cycles have a maximum current approaching 100% I_{LIMIT}. This gradually reduces to 30% of the full current limit as load decreases. Once 30% current limit is reached, there is no further reduction in current limit (since this is low enough to avoid audible noise). The time between switching cycles will continue to increase as load reduces.

Jitter

The normalized current limit is modulated between 100% and 95% at a modulation frequency of f_M this results in a frequency jitter of ~7 kHz with average frequency of ~100 kHz.

Auto-Restart

In the event a fault condition occurs (such as an output overload, output short-circuit, or external component/pin fault), the InnoSwitch4-Pro enters auto-restart (AR) or latches off. The latching condition is reset by bringing the PRIMARY BYPASS pin below $V_{BPP(RESET)}$ or by going below the UNDER/OVER INPUT VOLTAGE pin UV (I_{UV-}) threshold.

In auto-restart, switching of the power switch is disabled for $t_{AR(OFF)}$. There are 2 ways to enter auto-restart:

1. Continuous secondary requests at above the overload detection frequency f_{OVL} for longer than 82 ms (t_{AR}).
2. No requests for switching cycles from the secondary for > $t_{AR(SK)}$.

The second is included to ensure that if communication is lost, the primary tries to restart. Although this should never be the case in normal operation, it can be useful when system ESD events (for example) causes a loss of communication due to noise disturbing the secondary controller. The issue is resolved when the primary restarts after an auto-restart off-time.

The auto-restart is reset as soon as an AC reset occurs.

SOA Protection

In the event that there are two consecutive cycles where 110% I_{LIMIT} is reached within ~500 ns (the blanking time + current limit delay time), the controller will skip 2.5 cycles or ~25 µs. This provides sufficient time for the transformer to reset with large capacitive loads without extending the start-up time.

Input Line Voltage Monitoring

The UNDER/OVER INPUT VOLTAGE pin is used for input undervoltage and overvoltage sensing and protection.

A sense resistor is tied between the high-voltage DC bulk capacitor after the bridge (or to the AC side of the bridge rectifier for fast AC reset) and the UNDER/OVER INPUT VOLTAGE pin to enable this functionality. This function can be disabled by shorting the UNDER/OVER INPUT VOLTAGE pin to primary GND.

At power-up, after the primary bypass capacitor is charged and the ILIM state is latched, and prior to switching, the state of the UNDER/OVER INPUT VOLTAGE pin is checked to confirm that it is above the brown-in and below the overvoltage shutdown thresholds.

In normal operation, if the UNDER/OVER INPUT VOLTAGE pin current falls below the brown-out threshold and remains below brown-out for longer than t_{UV-}, the controller enters auto-restart. Switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current is above the brown-in threshold.

In the event that the UNDER/OVER INPUT VOLTAGE pin current is above the overvoltage threshold, the controller will also enter auto-restart. Again, switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current has returned to within its normal operating range.

The input line UV/OV function makes use of a internal high-voltage MOSFET on the UNDER/OVER INPUT VOLTAGE pin to reduce power consumption. If the cycle off-time t_{OFF} is greater than 50 µs, the internal high-voltage MOSFET will disconnect the external sense resistor from the internal IC to eliminate current drawn through the sense resistor. The line sensing function will activate again at the beginning of the next switching cycle.

HSD Operation (INN437xF and INN447xF)

When the primary controller receives a request from the secondary to begin a conduction cycle the InnoSwitch4-Pro first sends a signal through the HSD pin to turn on the high-side switch in the ClampZero for a fixed time of t_{HSD}. The amount of time required to build up energy in transformer for ZVS is a function of clamp capacitor and transformer leakage inductance. After this on-time, the InnoSwitch4-Pro will wait for a programmed delay (see: HSD to ZVS Delay Programming) before turning on the main primary switch to begin a flyback conduction cycle.

HSD to ZVS Delay Programming (INN437xF and INN447xF)

In order to successfully achieve zero voltage switching (ZVS), some delay is necessary between turn-off of the ClampZero switch and conduction of the InnoSwitch4-Pro. At low input line/full load in CCM operation, the required delay time is a function of the drain node capacitance and the leakage inductance of the transformer. To tune this delay t_{LLDL}, a resistor must be placed between the HSD pin and the SOURCE pin. This resistor can program one of four delays. Centering this delay at the lowest point of the Drain voltage is critical for optimizing ZVS operation.

HSD Resistor	Programmed Delay (t_{LLDL})
130 kΩ	80 ns
60 kΩ	100 ns
30 kΩ	120 ns
15 kΩ	140 ns

At high input line/full load in DCM operation, the required delay time is a function of the drain node capacitance and the sum of magnetizing and leakage inductance of the transformer. The delay is pre-programmed to t_{HLDL} ~450 ns.

This delay switches between t_{LLDL} and t_{HLDL} based on input line voltage information. When the UNDER/OVER VOLTAGE pin current rises above 53.75 µA, the delay becomes t_{HLDL} and remains t_{HLDL} until the current falls by 7.5 µA at which point t_{LLDL} is enabled. Hysteresis is provided to ensure longer delay for high-line ZVS.

Primary-Secondary Handshake

At start-up, the primary-side initially switches without any feedback information (this is very similar to the operation of a standard TOPSwitch™, TinySwitch™ or LinkSwitch™ controllers).

If no feedback signals are received during the auto-restart on-time (t_{AR}), the primary goes into auto-restart mode. Under normal conditions, the secondary controller will power-up via the FORWARD pin or from the OUTPUT VOLTAGE pin and take over control. From this point onwards the secondary controls switching.

If the primary controller stops switching or does not respond to cycle requests from the secondary during normal operation (when the secondary has control), the handshake protocol is initiated to ensure that the secondary is ready to assume control once the primary

begins to switch again. An additional handshake is also triggered if the secondary detects that the primary is providing more cycles than were requested.

The most likely event that could require an additional handshake is when the primary stops switching as the result of a momentary line brown-out event. When the primary resumes operation, it will default to a start-up condition and attempt to detect handshake pulses from the secondary.

If secondary does not detect that the primary responds to switching requests for 8 consecutive cycles, or if the secondary detects that the primary is switching without cycle requests for 4 or more consecutive cycles, the secondary controller will initiate a second handshake sequence. This provides additional protection against cross-conduction of the SR FET while the primary is switching. This protection mode also prevents an output overvoltage condition in the event that the primary is reset while the secondary is still in control.

Wait and Listen

When the primary resumes switching after initial power-up recovery from an input line voltage fault (UV or OV) or an auto-restart event, it will assume control and require a successful handshake to relinquish control to the secondary controller.

As an additional safety measure the primary will pause for an auto-restart on-time period, t_{AR} (~82 ms), before switching. During this "wait" time, the primary will "listen" for secondary requests. If it sees two consecutive secondary requests, separated by ~30 µs, the primary will infer secondary control and begin switching in slave mode. If no pulses occurs during the t_{AR} "wait" period, the primary will begin switching under primary control until handshake pulses are received.

Secondary Controller

As shown in the block diagram in Figure 4, the IC is powered by a 4.5 V (V_{BPS}) regulator which is supplied by either VOUT or FWD. The SECONDARY BYPASS pin is connected to an external decoupling capacitor and fed internally from the regulator block.

The FORWARD pin also connects to the negative edge detection block used for both handshaking and timing to turn on the SR FET connected to the SYNCHRONOUS RECTIFIER DRIVE pin. The FORWARD pin voltage is used to determine when to turn off the SR FET in discontinuous mode operation. This is when the voltage across the $R_{DS(ON)}$ of the SR FET drops below zero volts.

In continuous conduction mode (CCM) the SR FET is turned off before the pulse request is sent to the primary to demand the next switching cycle, providing excellent synchronous operation, free of any overlap for the FET turn-off.

The output voltage is regulated on the VOUT pin and defaults to 5 V at start-up.

The external current sense resistor connected between ISENSE and SECONDARY GROUND pins is used to regulate the output current in constant current regulation mode.

Programmable Voltage and Current

The operating voltage and current set points are set fully programmable through I²C interface. The output voltage is fully user programmable with a range from 3 V to 24 V. The fast response feedback loop of the IC features 10 mV (ΔVOUT) voltage change resolution. The programmable current set point features 15% to 100% operating range, with a programming step size of 0.52% of full scale current. Below 5 V and for load current less than 50 mA, voltage command step size of 10 mV may result in non-montonicity since operating frequency is very low.

Minimum Off-Time

The secondary controller initiates a cycle request using the FluxLink connection to the primary. The maximum frequency of secondary-cycle requests is limited by a minimum cycle off-time of $t_{OFF(MIN)}$. This is in order to ensure that there is sufficient reset time after primary conduction to deliver energy to the load.

Maximum Switching Frequency

The maximum switch-request frequency of the secondary controller is f_{SREQ}.

Internal uVCC Generation, Bus Switch Driver and Discharge

The internal LDO generates 3.6 V uVCC for MCU which simplifies the system design. InnoSwitch4-Pro also has an internal driver that guarantees turn-on of an n-channel FET series bus switch with source voltage as high as 24 V. The VB/D pin which enables the bus switch is also configurable as the discharge path for the load.

Programmable Protections

User programmable protection features include output undervoltage (UV) and overvoltage (OV) protection and over-temperature protection.

The UV/OV thresholds are dynamically programmable. Users can program four responses to these protections, including auto-restart, latch-off, disable output, and no-response. An auto-restart (AR) or latch-off (LO) response does not inherently open the series bus switch. The I²C master must send a command to open it if this is the desired behavior.

The secondary controller also features generation of an interrupt signal if one or more of the faults is detected. The SCL pin is pulled down for ~55 µs to generate an interrupt for MCU.

In the case when the MCU loses communication with the secondary controller, a watchdog timer triggers a reset to reassert a safe 5 V condition and opens the series bus switch.

Telemetry Feature

The controller communicates to the MCU to report back the status of the power supply. Output voltage and current is measured by internal ADC and available to MCU through I²C. The telemetry features also covers CV, CC and constant power set points, OV/UV thresholds, all protection settings, interrupt status, and complete fault status.

Frequency Soft-Start

At start-up the primary controller is limited to a maximum switching frequency of f_{SW} and 75% of the maximum programmed current limit at the switch-request frequency of 100 kHz.

After hand-shake is completed the secondary controller linearly ramps up the switching frequency from f_{SW} to f_{SREQ} over the ~10 ms time period.

In the event of a short-circuit or overload at start-up, the device will move directly into CC (constant-current) mode. The device will go into auto-restart (AR), if the output voltage does not rise above the 3.6 V before the expiration of the soft-start timer after handshake has occurred.

If the output voltage reaches regulation within the soft-start time period, the frequency ramp is immediately aborted and the secondary controller is permitted to go full frequency. This will allow the controller to maintain regulation in the event of a sudden transient loading soon after regulation is achieved. The frequency ramp will only be aborted if quasi-resonant-detection programming has already occurred.

Maximum Secondary Inhibit Period
Secondary requests to initiate primary switching are inhibited to maintain operation below maximum frequency and ensure minimum off-time. Besides these constraints, secondary-cycle requests are also inhibited during the "ON" time cycle of the primary switch (time between the cycle request and detection of FORWARD pin falling edge). The maximum time-out in the event that a FORWARD pin falling edge is not detected after a cycle requested is ~30 µs.

SECONDARY BYPASS Pin Overvoltage Protection
The InnoSwitch4-Pro secondary controller features SECONDARY BYPASS pin OV feature similar to PRIMARY BYPASS pin OV feature. When the secondary is in control: in the event the SECONDARY BYPASS pin current exceeds $I_{BPS(SD)}$ the secondary will initiate a fault response dictated by sec-fault response.

SR Disable Protection
In each cycle SR is only engaged if a set cycle was requested by the secondary controller and the negative edge is detected on the FORWARD pin. In the event that the voltage on the ISENSE pin exceeds approximately 3 times the CC threshold, the SR FET drive is disabled until the surge current has diminished to nominal levels.

SR Static Pull-Down
To ensure that the SR gate is held low when the secondary is not in control, the SYNCHRONOUS RECTIFIER DRIVE pin has internal nominally "ON" device to pull the pin low and reduce any voltage on the SR gate due to capacitive coupling from the FORWARD pin.

Open SR Protection
In order to protect against an open SYNCHRONOUS RECTIFIER DRIVE pin system fault the secondary controller has a protection mode to ensure the SYNCHRONOUS RECTIFIER DRIVE pin is connected to an external FET. If the external capacitance on the SYNCHRONOUS RECTIFIER DRIVE pin is below ~200 pF, the device will assume the SYNCHRONOUS RECTIFIER DRIVE pin is "open" and there is no FET to drive. If the pin capacitance detected is above ~200 pF, the controller will assume an SR FET is connected.

In the event the SYNCHRONOUS RECTIFIER DRIVE pin is detected to be open, the secondary controller will stop requesting pulses from the primary to initiate auto-restart.

If the SYNCHRONOUS RECTIFIER DRIVE pin is tied to ground at start-up, the SR drive function is disabled and the open SYNCHRONOUS RECTIFIER DRIVE pin protection mode is also disabled.

ZVS Operation in DCM and CCM Operating Modes (INN437xF and INN447xF)
In order to improve conversion efficiency and eliminate switching losses, the InnoSwitch4-Pro features a drive signal to the companion ClampZero device as means to force the voltage across the primary power switch to zero before every conduction cycle. This mode of operation is automatically engaged in both DCM and CCM, dramatically simplifying system design. In DCM, stress across the high-side clamp switch is minimized to control the timing of the clamp-switch turn-on. By restricting conduction cycles to the peak of the drain voltage ring, switching loss across the ClampZero switch is minimized. See Figure 7a.

Rather than detecting the magnetizing ring peak on the primary-side, the valley voltage of the FORWARD pin voltage as it falls below the output voltage level is used to gate secondary requests to initiate the switch "ON" cycle in the primary controller.

The secondary controller detects when the controller enters in discontinuous-mode and opens secondary cycle request windows corresponding to maximum switching voltage across the primary power switch.

Secondary valley switching is enabled for 20 µs after DCM is detected or when (FORWARD Pin) ring amplitude (pk-pk) >2 V. Afterwards, valley switching is disabled, at which point switching of the active clamp switch may occur at any time a secondary request is initiated.

The secondary controller includes blanking of ~1200 ns to prevent false detection of the primary "ON" cycle when the FORWARD pin rings below ground.

Unlike in InnoSwitch3 devices, the valley switching mode does not play a direct role in initiating the turn-on of the primary-side power switch, instead the active clamp circuit creates the low VDS condition on the primary power switch necessary for it to operate with ZVS.

Intelligent Quasi-Resonant Mode Switching (INN457xF and INN467xF)
In order to improve conversion efficiency and reduce switching losses, the lnnoSwitch4-Pro features a means to force switching when the voltage across the primary switch is near its minimum voltage when the converter operates in discontinuous conduction mode (DCM). This mode of operation is automatically engaged in DCM and disabled once the converter moves to continuous conduction mode (CCM). See Figure 7b.

Rather than detecting the magnetizing ring valley on the primary-side, the peak voltage of the FORWARD pin voltage as it rises above the output voltage level is used to gate secondary requests to initiate the switch "ON" cycle in the primary controller.

The secondary controller detects when the controller enters in discontinuous-mode and opens secondary cycle request windows corresponding to minimum switching voltage across the primary power switch.

Quasi-Resonant (QR) mode is enabled for 20 µsec after DCM is detected. QR switching is disabled after 20 µsec, at which point switching may occur at any time a secondary request is initiated. The secondary controller includes blanking of ~1 µsec to prevent false detection of primary "ON" cycle when the FORWARD pin rings below ground.

ZVS and QR Switching Window Optimization
InnoSwitch4-Pro allows for optimization of switching to achieve QR/ Valley switching as close to the peak/minimum FORWARD voltage respectively. Command register 0x02 = 0x1F is recommended for optimal switching.

Default value is 0x01.

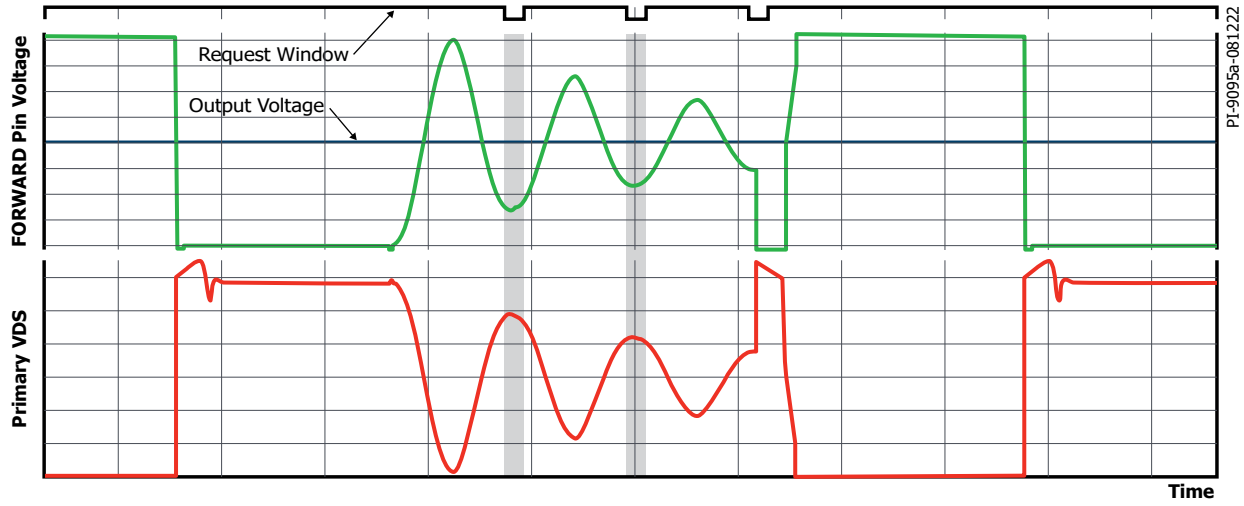


Figure 7a. Intelligent Zero Voltage Mode Switching.

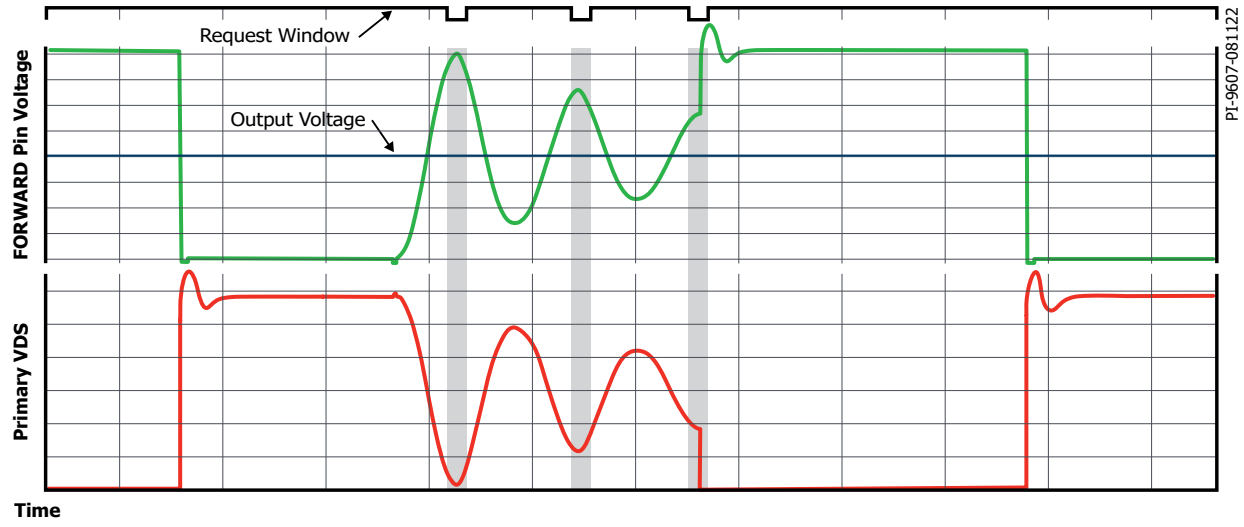


Figure 7b. Intelligent Quasi-Resonant Mode Switching.

Register Definition

I²C Slave Address

The InnoSwitch4-Pro 7-bit slave address is 0x18 (7'b001 1000).

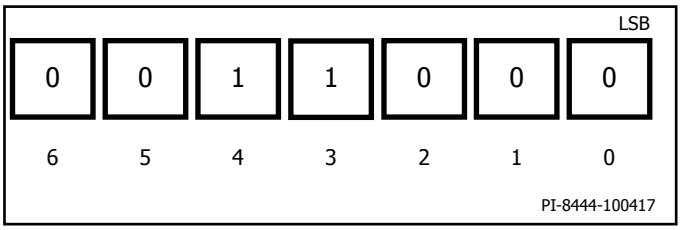


Figure 8. PI Slave Address.

I²C Protocol Format is 3-Byte Write Command

Write commands:
[PI_SLAVE_ADDRESS][W][A][PI_COMMAND][A][Byte][A] or
[PI_SLAVE_ADDRESS][W][A][PI_COMMAND][A][Low Byte][A][High Byte][A]

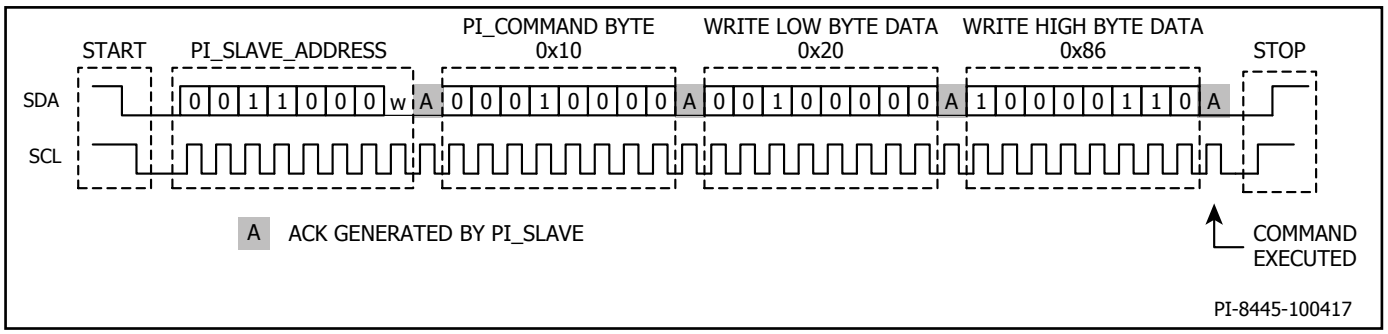


Figure 9. Example Register Write Command Sequence (CV set to 8 V).

I²C Protocol Format is 2-Byte Read Command

Word Read transaction:
[PI_SLAVE_ADDRESS][W][A][PI_COMMAND][A][START_TELEMETRY_REGISTER_ADDRESS]
[A][END_TELEMETRY_REGISTER_ADDRESS [A]
[PI_SLAVE_ADDRESS] [r][A]{PI Slave responds Low Byte}[a]{PI Slave responds High Byte}[na]

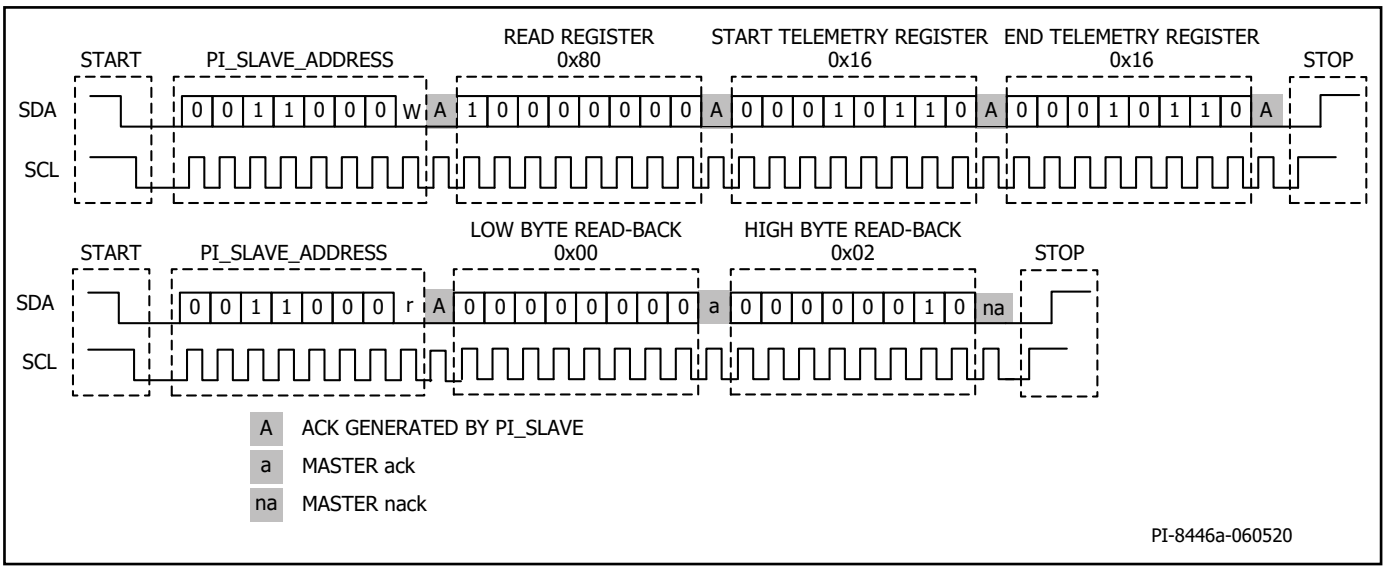


Figure 10. Example Read Register Sequence (Read Fault Register READ11). Note: START and END TELEMETRY Register Addresses Does Not Have to Point to Same Register to Read multiple Registers in Single Command.

Write and Read Command I²C Protocol

[A] denotes a Slave Acknowledgement
[a] denotes a Master Acknowledgement
[na] denotes a Master nack
[W] denotes Write (1'b0)
[r] denotes Read (1'b1)
[PI_SLAVE_ADDRESS] = 0x18 (7'b001 1000)
[PI_COMMAND] (see PI COMMAND Register Address Assignments, Description and Control Range Section)
[TELEMETRY_REGISTER_ADDRESS] (see Telemetry (Read-Back) Registers Address Assignment and Description Section)

Every I²C transaction should have a minimum of 150 μsec delay between commands. If this delay is not provided commands may be ignored. The InnoSwitch4-Pro does not support clock stretching.

PI COMMAND Register Address Assignments, Description and Control Range

All command register addresses in InnoSwitch4-Pro are odd-parity addressing. Some select registers (some highlighted below) also employ odd parity error bit to the high and low bytes of data.

Name	Function	Adjustment Range	Register Address		Type	Default	Description	
			Address	Address with Odd Parity				
VBEN[D]	Series Bus Switch Control	Enable or Disabled?	0x04		W_Byte	0x0	bit[7]	Parity
							bit[1:0]	{11} Enable VBEN/Disable VDIS {01} Disable VBEN/No Reset {00} Disable VBEN/Reset
BLEEDER[E]	Activate Bleeder (V_{OUT}) Function	Enable or Disabled?	0x06	0x86	W_Byte	0xD0	bit[1:0]	{00}: Disabled {01}: Enabled {11}: Enabled with auto disable OTP clears this register
VDIS[A]	Load (VBUS) Discharge	Enable or Disabled?	0x08		W_Byte	0x0	bit[7]	Parity
							bit[1:0]	{11} Enable Discharge/Disable VBEN/Reset {10} Enable Discharge/No Reset
							bit[3:2]	{11} Disable Discharge
Turn-Off PSU	Latch-off Device	Enable or Disabled?	0x0A	0x8A	W_Byte	0x0	bit[0]	{0}: Disabled {1}: Enabled
Fast VI Command	Speed of CV/CC Update	10 ms Update Limit or No Speed Limit?	0x0C	0x8C	W_Byte	0x0	bit[0]	{1}: Disable 10 msec update limit
CVO	Constant-Voltage Only	Only CV Mode	0x0E		W_Byte	0x04	bit[4:3]	{11}: 64 ms {10}: 32 ms {01}: 16 ms {00}: 8 ms
							bit[2:1]	{11}: Disable-Output[C] {10}: Auto-Restart {01}: Latch-Off {00}: No Response
							bit[0]	{1}: CV Only Mode/No CC Regulation
CV[B]	Output Voltage	3 V to 24 V (10 mV/step)	0x10		W_Word	500 (5 V)	bit[15]	High Byte Parity
							bit[13]	Enable auto set UVA, OVA in CVO mode
							bit[12:8]	Output voltage
							bit[7]	Low Byte Parity
							bit[6:0]	Output Voltage

Range {300 to 2400} 10 mV/LSB

Table 2. Command Register Assignments.

Name	Function	Adjustment Range	Register Address		Type	Default	Description		
			Address	Address with Odd Parity					
OVA	Overvoltage Programming	3.3 V to 25 V (100 mV/step)	0x12	0x92	W_Word	Auto-Restart 62 (6.2 V)	bit[15]	High Byte Parity	Range {33 to 250} 100 mV/LSB
							bit[10:9]	{11}: Disable-Output[C] {10}: Auto-Restart {01}: Latch-Off {00}: No Response	
							bit[8]	Threshold	
							bit[7]	Low Byte Parity	
							bit[6:0]	Threshold	
UVA	Undervoltage Threshold	2.7 V to 24 V (100 mV/step)	0x14	0x94	W_Word	64ms Auto-Restart 36 (3.6 V)	bit[15]	High Byte Parity	Range {27 to 240} 100 mV/LSB
							bit[12:11]	{11}: 64ms {10}: 32ms {01}: 16ms {00}: 8ms	
							bit[10:9]	{11}: Disable-Output[C] {10}: Auto-Restart {01}: Latch-Off {00}: No Response	
							bit[8]	Threshold	
							bit[7]	Low Byte Parity	
							bit[6:0]	Threshold	
CDC	Cable Drop Compensation	0 mV to 600 mV (50 mV/step)	0x16		W_Word	0 (0 V)	bit[3:0]	Range {0 to 12} 50 mV/LSB	
CC	Constant Current Regulation	15% to 100% of CC, (0.17 mV/step/Rs)	0x18	0x98	W_Word	192 (100%)	bit[15]	High Byte Parity	Range {29 (15%) to 192 (100%)}
							bit[8]		
							bit[7]	Low Byte Parity	
							bit[6:0]		
V_{KP}	Constant Output Power Knee Voltage	5.3 V to 24 V (100 mV/step)	0x1A		W_Word	240 (24V)	bit[15]	High Byte Parity	Range {53 to 240} 100 mV/LSB
							bit[8]		
							bit[7]	Low Byte Parity	
							bit[6:0]		
CCSC	Output Short-Circuit Fault Detection	Disable Output, AR, Latch-off or No Response	0x20		W_Byte	0x02	bit[1:0]	{11}: Disable-Output[C] {10}: Auto-Restart {01}: Latch-Off {00}: No Response	

Table 2. Command Register Assignments (cont).

Name	Function	Adjustment Range	Register Address		Type	Default	Description	
			Address	Address with Odd Parity				
ISSC	IS-pin Short Fault Response and Detection Frequency/ Threshold	Disable Output, AR, Latch-off or No Response	0x22	0xA2	W_Byte	0x32	bit[1:0]	{11}: Disable-Output[C] {10}: Auto-Restart {01}: Latch-Off {00}: No Response
		Frequency? (30k Hz/60k Hz/ 90 kHz/120 kHz)					bit[3:2]	Frequency Detection Threshold {00}: 60 kHz {01}: 30 kHz {10}: 90 kHz {11}: 120 kHz
		Threshold for Current Limit					bit[6:4]	{001}: d'16 {010}: d'32 {011}: d'48 {100}: d'64 {101}: d'80 {110}: d'96 {111}: d'112
Watchdog Time	Communication Rate Monitor	Disable/0.5 s/1 s/2 s	0x26		W_Byte	0x01 (0.5 sec)	bit[1:0]	{00}: No Watch-Dog {01}: 0.5 sec {10}: 1 sec {11}: 2 sec
Interrupt	Interrupt Mask	Writing a non-zero value enables interrupt	0x2C		WR_Byte	0x00	bit[8]	Operating Mode Flag (OMF)
							bit[7]	Series Bus Switch Short
							bit[6]	Control Secondary
		Interrupt is automatically disabled after one interrupt pulse sent out					bit[5]	BPS Current Latch-off
							bit[4]	CVO Mode Peak load timer
							bit[3]	IS pin Short
							bit[2]	Output Short-Circuit
							bit[1]	Vout(UV)
							bit[0]	Vout(OV)
OTP	Secondary Over-Temperature Fault Hysteresis	40 °C / 60 °C	0x2E	0xAE	W_Byte	0x00	bit[0]	{0}: 40°C {1}: 60°C
VBUSSC	Series BUS Switch Short-Circuit Fault	Threshold for Current Sense	0x36	0xB6	W_Byte	0x02	bit[5:4]	{11}: d'72 {10}: d'64 {01}: d'32 {00}: d'48
		Number of Current Sense Samples					bit[3:2]	{11}: 4 samples {10}: 3 samples {01}: 2 samples {00}: 1 sample
		AR, Latch-off or No Response					bit[1:0]	{10}: Auto-Restart {01}: Latch-Off {00}: No Response
DCM-only	Discontinuous Conduction Mode Only	Enable or Disabled?	0x3A	0xBA	W_Byte	0x00	bit[2]	{0}: Disable {1}: Enable

Table 2. Command Register Assignments (cont).

Notes:
A. Send VBEN=Disable/No Reset after sending VDIS command with No Reset option.
B. At lower output voltage and light load below 50 mA, CV command with auto set OVA, UVA may trigger AR during decrement CV transitions.
C. Disable Output Fault Response Disables VBEN with Reset at fault. Reset may trigger AR depending on the operating conditions.
D. Output voltage before the series bus switch must be less than 16 V to issue the {EnabledVBEN/Disable VDIS} command.
E. Disable the weak bleeder by writing 0x0x into 0x86 at power-on to reduce no-load power.

Telemetry (Read-Back) Registers Address Assignment and Description

	Name	Register Name	Register Address	Type	Register Bit Assignments		
Command Register Read-Back	READ1	Output Voltage Set-Point	0x02	R_Word	bit[15]	High Byte Parity	{Reg_CV}
					bit[12:8]		
					bit[7]	Low Byte Parity	
					bit[6:0]		
	READ2	Output Current Set-Point	0x04	R_Word	bit[15]	High Byte Parity	{Reg_CC}
					bit[8]		
					bit[7]	Low Byte Parity	
					bit[6:0]		
	READ3	Overvoltage Threshold	0x06	R_Word	bit[15]	High Byte Parity	{Reg_OVA}
					bit[12:8]		
					bit[7]	Low Byte Parity	
					bit[6:0]		
	READ4	Undervoltage Threshold	0x08	R_Word	bit[15]	High Byte Parity	{Reg_UVA}
					bit[12:8]		
					bit[7]	Low Byte Parity	
					bit[6:0]		
	READ5	Constant Current Set-Point	0x0A	R_Word	bit[15:8]	{Reg_CC}	
		Constant Power Threshold			bit[7:0]	{Reg_VKP}	
	READ6	Overvoltage Fault	0x0C	R_Word	bit[15:14]	{Reg_OVA_Response}	
		Undervoltage Fault			bit[13:12]	{Reg_UVA_Response}	
		Output Short-Circuit			bit[11:10]	{Reg_CCSC_Response}	
		IS pin Short			bit[9:8]	{Reg_ISSC_Response}	
		Undervoltage Time Out			bit[7:6]	{Reg_UVA_TIMER}	
		Watchdog Time Out			bit[5:4]	{Reg_WD_TIMER}	
		CV Mode			bit[3:2]	{Reg_CVO_Response}	
		CV Mode Timer			bit[1:0]	{Reg_CVO_TIMER}	
	READ7	VBUS Switch Enable	0x0E	R_Word	bit[14]	{Reg_VBEN}	
		Minimum Load			bit[13]	{Reg_BLEEDER}	
		Turn PSU Off			bit[12]	{Reg_PSUOFF}	
		Fast VI Commands			bit[11]	{Reg_FSTVIC}	
		Constant-Voltage Mode Only			bit[10]	{Reg_CVO}	
		Over-Temperature Fault Hysteresis			bit[9]	{Reg_OTP_HYS}	
		Cable Drop Compensation			bit[3:0]	{Reg_CDC}	
Measurement	READ8	Measured Output Current	0x10	R_Word	bit[15]	High Byte Parity	{Reg_ MEASURED_I}
					bit[8]		
					bit[7]	Low Byte Parity	
					bit[6:0]		
	READ9	Measured Output Voltage	0x12	R_Word	bit[15:12]	4'b0	
					bit[11:0]	{Reg_MEASURED_V}	
						Vout Range	Report-back resolution
						3 - 7.2 V	20 mV
						7.2 - 10 V	50 mV
						10 - 20 V	100 mV

Table 3. Telemetry (Read-Back) Register Assignments.

Name	Description	Register Address	Type	Register Name	
READ10 (Instanta-neous)	Interrupt Enable	0x14	R_Word	bit[15]	{Reg_INTERRUPT_EN}
	System Ready Signal			bit[14]	{Reg_CONTROL_S}
	Output Discharge			bit[13]	{Reg_VDIS}
	Switching Frequency High?			bit[12]	{Reg_HIGH_FSW}
	Write Auto CV Enabled?			bit[10]	{Reg_CV_EN}
	Over-Temperature Protection Fault?			bit[9]	{Reg_OTP}
	Weak Bleeder Enabled			bit[5]	{Reg_VOUTWK}
	VOUTADC > 1.1*Vout			bit[4]	{Reg_VOUT10PCT}
	IS-pin Short-Circuit Detected			bit[3]	{Reg_ISSC}
	Output Short-Circuit Detected			bit[2]	{Reg_CCSC}
	Output Voltage UV Fault Comparator			bit[1]	{Reg_VOUT_UV}
	Output Voltage OV Fault Comparator			bit[0]	{Reg_VOUT_OV}
READ11	Operating Mode Flag (OMF)	0x16	R_Word	bit[2]	CC Mode
				bit[1]	CP Mode
				bit[0]	CV Mode
READ12	Average Output Current	0x18	R_Word	bit[15:8]	8b'0
				bit[7:0]	16 sample average of READ 8
READ13	Average Output Voltage	0x1A	R_Word	bit[15:12]	4b'0
				bit[11:0]	16 sample average of READ 9
READ14	Voltage DAC	0x1C	R_Word	bit[15:8]	DAC_100 mV
				bit[7:0]	DAC_10 mV
READ16	CVO Mode AR	0x20		bit[15]	{Reg_ar_CVO}
	IS pin Short-Circuit AR			bit[12]	{Reg_ar_ISSC}
	Output Short-Circuit AR			bit[11]	{Reg_ar_CCSC}
	Output Voltage OV AR			bit[10]	{Reg_ar_VOUT_OV}
	Output Voltage UV AR			bit[9]	{Reg_ar_VOUT_UV}
	Latch-Off (LO) Occurred			bit[7]	{Reg_LO}
	CVO Mode LO			bit[6]	{Reg_Lo_CVO}
	PSU Turn-Off CMD Received			bit[5]	{Reg_PSUOFF}
	IS-pin Short-Circuit LO			bit[4]	{Reg_Lo_ISSC}
	Output Voltage OV LO			bit[2]	{Reg_Lo_VOUT_OV}
	Output Voltage UV LO			bit[1]	{Reg_Lo_VOUT_UV}
	BPS pin LO			bit[0]	{Reg_BPS_OV}
READ17	Interrupts	0x22	R_Word	Mask	Status
					bit[8] {Reg_OMF}
					bit[7] {Reg_VBUSSC}
				bit[15]	bit[6] {Reg_~CONTROL_S}
				bit[14]	bit[5] {Reg_LO_Fault}
				bit[13]	bit[4] {Reg_CVO_AR}
				bit[12]	bit[3] {Reg_ISSC}
				bit[11]	bit[2] {Reg_CCSC}
				bit[10]	bit[1] {Reg_VOUT_UV}
				bit[9]	bit[0] {Reg_VOUT_OV}

Table 3. Telemetry (Read-Back) Register Assignments (cont.)

Command Registers

System Ready Status Register

The system ready bit {Reg_control_s} must be read prior to the start of any I²C transactions and after the InnoSwitch4-Pro has entered into a reset state resulting from auto-restart (AR), latch-off (LO), Disable Output (DO) or initial power-up.

When the {Reg_control_s} bit is set to "1", it means InnoSwitch4-Pro is ready to receive I²C commands.

To read the {Reg_control_s} bit, write the READ10 sub address 0x14 into the 0x80 address. Then read High Byte data back from address 0x80. The bit 14 is {Reg_control_s}.

Constant current regulation is based on the average current measurement register (READ12).

For a 5 A CC threshold, the current sense resistor is 6.4 mΩ. The current limit step size for this example is ~26 mA/step.

Example: For a power supply with maximum CC of 5 A (Rs = 6.4 mΩ), the following demonstrates changing the CC set point from 5 A to 2.5 A. This corresponds to change in CC from 100% (0xC0) to 50% (0x60) – with odd parity this becomes 0x80E0::

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	CC Register (0x98)
Low Byte:	0xE0 (8'b0100 0000)
High Byte:	0x80 (8'b1000 0000)

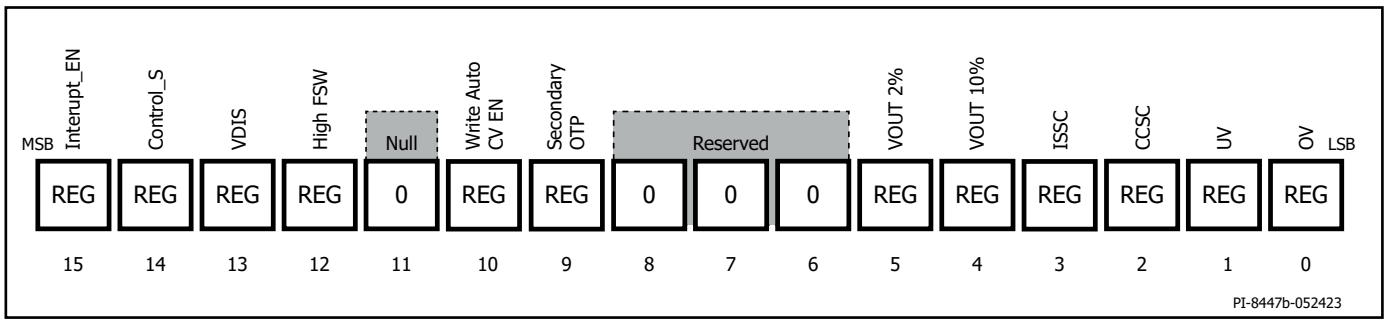


Figure 11. {Reg_Control_s} Telemetry Register (READ 10).

Example: Reading the {Reg_control_s} bit:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
Read Register:	0x80
PI_Command:	READ10 (0x14), READ10 (0x14)
PI_SLAVE_ADDRESS [r]:	0x31 (8'b0011 0001)

Programming Output Voltage (CV), Output Constant Current (CC), Constant Power Mode (CP), Cable Drop Compensation (CDC) and Constant Voltage Only Mode (CVO)

CV Register (0x10)

The output voltage of the power supply is regulated on the VOUT pin. The valid programming range is from 3 V to 24 V with 10 mV / lsb. The default CV register value is 5 V. Below 5 V and at light load below 50 mA, output monotonicity may not be visible with 10 mV / steps.

Example: to change CV from 5 V to 8 V
Convert 8 V to lsb representation: 8/(10mV/lsb) = 800
Convert to hex format (800 = 0x0320)
With odd parity bits added the hex data is 0x8620)
The bit I²C command for this is shown below:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	CV Register (0x10)
Low Byte:	0x20 (8'b0010 0000)
High Byte:	0x86 (8'b1000 0110)

This sequence of commands is shown in Figure 9 and Figure 20.

CC Register (0x98)

The constant current regulation register address is 0x18 and with odd parity it is 0x98. The constant current regulation threshold is adjustable from 15% (d'29) CC up to 100% (d'192) of the full scale. The full-scale constant-current threshold is set with the sense resistor between the IS and GND pins. The typical value for the full-scale current voltage drop is 32 mV ($_{ISV(TH)}$). The resolution step size is (0.52%/step):

32 mV/192 = 0.167 mV/step/Rs

Constant Output Power Voltage Threshold V_{KP} (0x1A)

A constant output power characteristic is programmed via the "knee power voltage" in conjunction with the 100% constant current regulation threshold (full-scale current setting). If the full-scale CC is 2.5 A and the knee power voltage is set to 8 V, the constant power is 20 W. If the VKP register were set to 12 V, the resultant constant power characteristic above the VKP threshold would be 30 W.

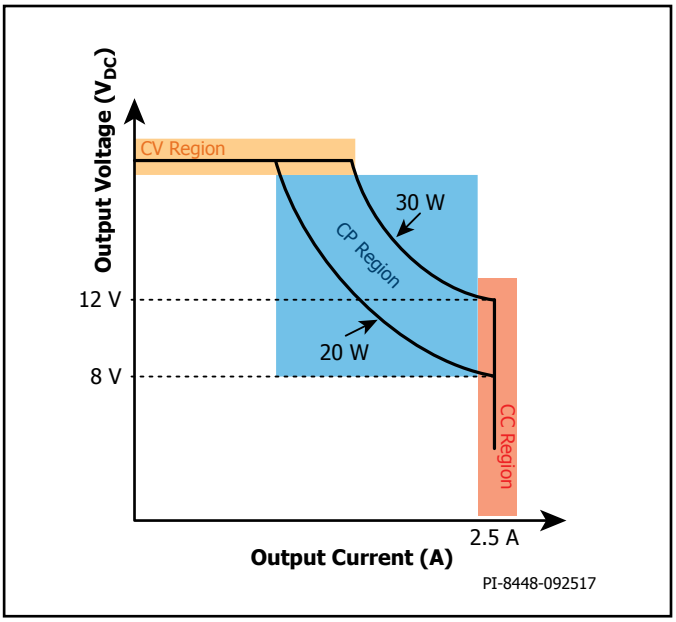


Figure 12. Constant Output Power Profile.

From no-load to heavy loading conditions, InnoSwitch4-Pro will operate in CV then transition into CP then into CC region below the V_{KP} threshold. Setting V_{KP} to maximum value (24 V) results in no Constant Output Power regulation region.

Example: To change V_{KP} from 24 V (d'240) (0xF0 = 0x0170 with odd parity) to 8 V (0x50 = 0x80D0):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	VKP Register (0x1A)
Low Byte:	0xD0 (8'b1101 0000)
High Byte:	0x80 (8'b1000 0000)

Reducing the constant current regulation threshold does not modify the maximum programmed output power with a given V_{KP} setting. From the example shown above, setting CC regulation to 2 A (full-scale CC is still 2.5 A), with V_{KP} = 8 V, would result in output profile shown below with CP characteristic intercept of 10 V for the same 20 W constant power characteristic.

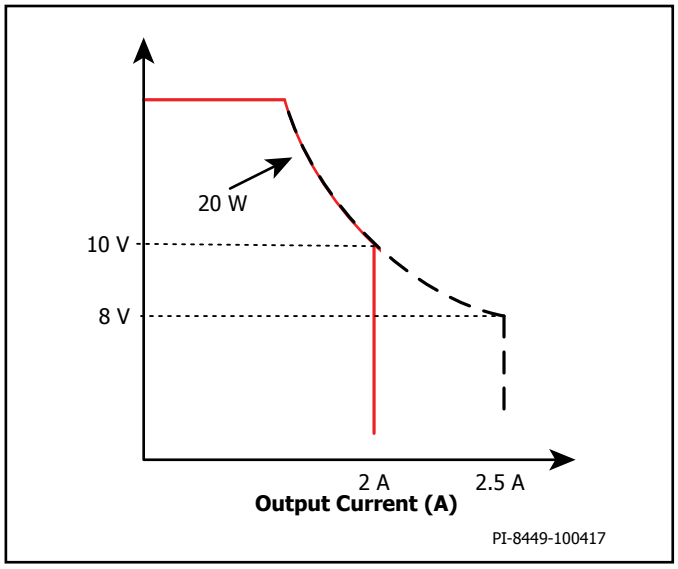


Figure 13. Constant Output Power Profile with Reduced CC Regulation Threshold.

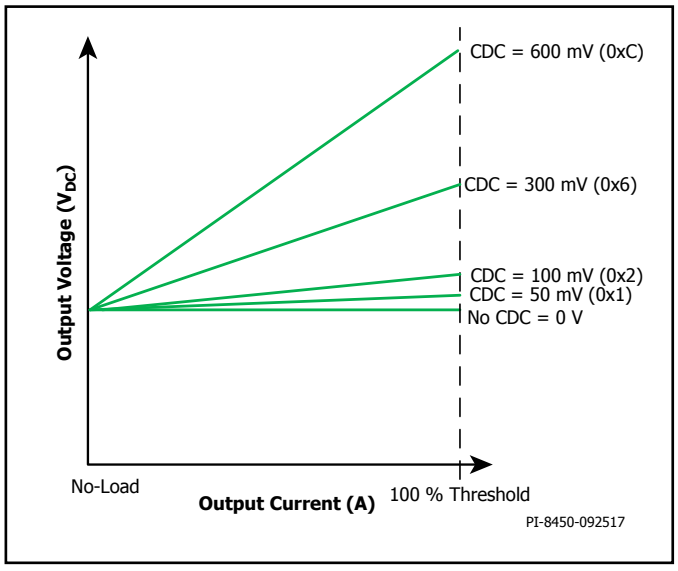


Figure 14. CDC as Function of Load Current.

Cable Drop Compensation (CDC) (0x16)

The amount of cable drop compensation has a controllable range of 0 V to 600 mV in 50 mV/steps. CDC is applied as a function of the current through the sense resistor (resistor between IS and GND pins) used to program the constant current regulation threshold. At no-load there is no CDC and the compensation is increased linearly as load increases and reaches the maximum programmed value at the onset of the 100% constant-current regulation threshold (full-scale voltage across the current sense resistor).

The table below shows the register values to program the desired CDC:

CDC (mV)	Hex Value	Binary
0	0x00	4'b0000
100	0x02	4'b0010
150	0x03	4'b0011
200	0x04	4'b0100
250	0x05	4'b0101
300	0x06	4'b0110
350	0x07	4'b0111
400	0x08	4'b1000
450	0x09	4'b1001
500	0x0A	4'b1010
550	0x0B	4'b1011
600	0x0C	4'b1100

Table 4. Cable Drop Compensation.

If the current sense resistor between IS pin to GND pin is shorted, there will be neither any cable drop compensation nor any constant current regulation.

Example: To change CDC from 0 V to 300 mV (0x06):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b1011 0000)
PI_Command:	CDC Register (0x16)
Byte:	0x06 (4'b0110)

Constant Voltage Only Mode (0x0E)

The InnoSwitch4-Pro can be programmed to operate with constant-voltage only and have no constant current regulation mode. The set output current register (0x98) sets the overload threshold instead of regulating the constant current when the CVO mode is enabled. Once the load current exceeds the programmed current a peak load timer (t_{PLT}) is started. The options for the peak load timer (CVO timer bit [4:3] of Register 0x0E) are 8 ms, 16 ms, 32 ms or 64 ms. If the peak load exceeds the programmed timer, the InnoSwitch4-Pro can be programmed to respond to this fault as disable output, auto-restart, latch-off or no-response through the CVO Register 0x0E bit [2:1]. The default response for peak overload is auto-restart with 8 ms timer.

In case of Disable – Output (DO) response, InnoSwitch4-Pro will open the series bus switch and reset to default configuration when the fault occurs. After reset, InnoSwitch4-Pro might annunciate other faults – example VOUT OV AR depending on the operating condition of the power supply.

Auto CV Mode

In CVO mode only, InnoSwitch4-Pro includes auto set OVA and UVA feature for any output voltage programmed in the CV register (0x10). OVA and UVA thresholds are set ~12.5% higher and lower than programmed CV.

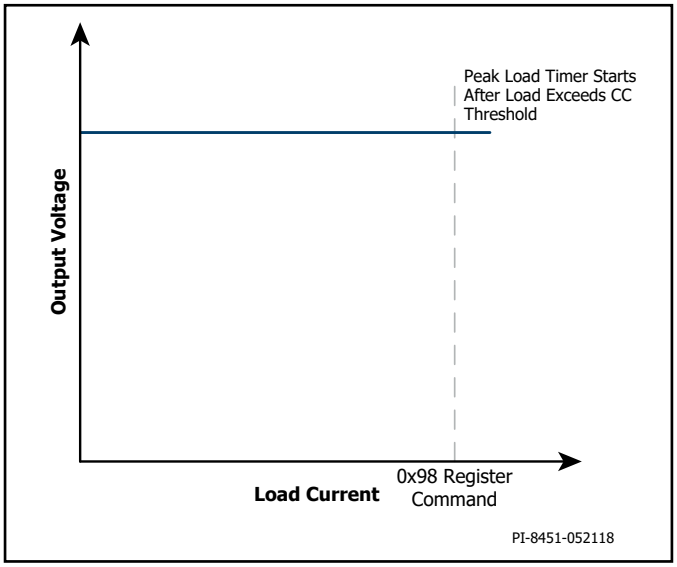


Figure 15. Constant Voltage Only (CVO) Mode.

In case of output voltage decrement, the BLEEDER is automatically enabled and disabled when VOUT10PCT flag is cleared. The fault responses will remain the same as programmed in OVA and UVA registers, only the thresholds will be adjusted. At light loads below 50 mA, the OVA fault might trigger due to output voltage rise after BLEEDER turns off. This can be mitigated by setting OVA fault response to No-Response before using the auto set OVA and UVA feature for voltage decrement command.

Example: Enable CVO Mode, set t_{PLT} to 16 ms and fault response to Disable - Output (DO): (0x0F)

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	CVO Register (0x0E)
Byte:	0x0F (8'b0000 1111)

Example: Set CV =10 V (1000 = 0x3E8) with auto set OVA and UVA (bit [13] = 1'b1 of CV register 0x10):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	CV Register (0x10)
Low Byte:	0xA7 (8'b1010 0111)
High Byte:	0x68 (8'b0110 1000)
Byte:	0x02 (2'b10)

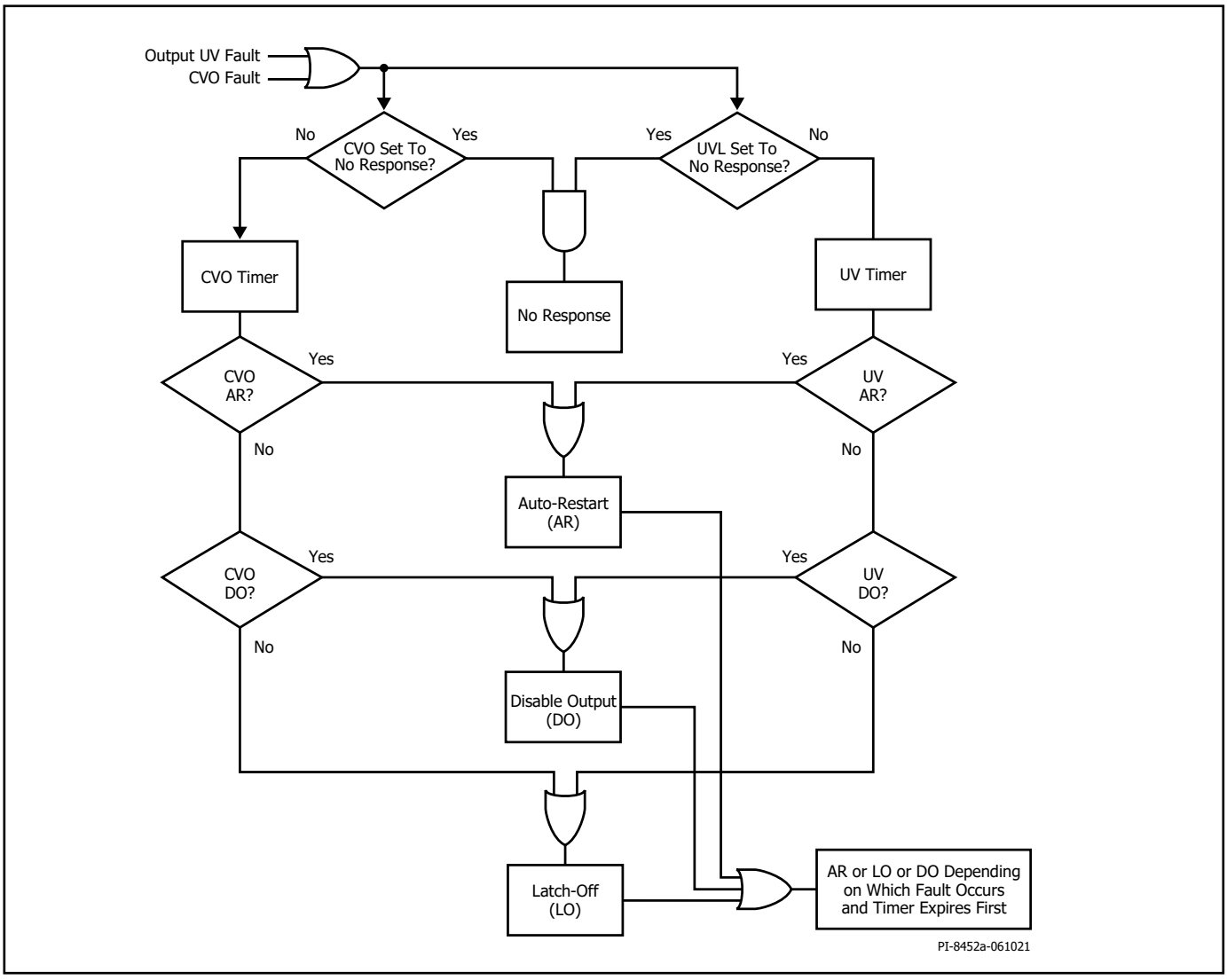


Figure 16. CVO and Output UV Control.

The output undervoltage protection mode discussed in Output Overvoltage and Undervoltage Protection Thresholds/Fault Behavior section is still active in the CVO mode of operation even if the individual UV fault response is set to 'No response'. The Figure 16 control flow-chart shows the expected behavior of the device under the different potential programming scenarios.

Programmable Protection Mechanisms

Output Overvoltage and Undervoltage Protection Thresholds/Fault Behavior

Besides the ability of programing the OV/UV thresholds on the fly as a function of the set CV, the behavior of the power supply once a fault occurs (a. No-Response which just sets the fault register, b. Latch-off (LO), c. Auto-restart (AR) or d. Disable Output (DO)) and timing for the UV fault detection (8 ms, 16 ms, 32 ms or 64 ms) is programmable as well. The output overvoltage delay is fixed at ~80 µs. All faults that are programmed to have no-response will be logged into the telemetry read-back fault register.

In case of Disable – Output (DO) response, InnoSwitch4-Pro will open the series bus switch and reset to default configuration when the fault occurs. After reset, InnoSwitch4-Pro might annunciate other faults – example VOUT OV AR depending on the operating condition of the power supply.

OVA(0x92) : write to this address to specify the overvoltage threshold and fault response to OV fault
UVA(0x94) : write to this address to specify the undervoltage threshold, UV timer and fault response to UV fault

Example: To change the absolute output undervoltage threshold 3 V (d'30), fault response to Disable-Output (DO) and configure fault timer to 64ms: (0x9E9E with odd parity)

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	UVA Register (0x94)
Low Byte:	0x9E (8'b1001 1110)
High Byte:	0x9E (8'b1001 1110)

IS Pin and Output Short-Circuit Fault Protection

The InnoSwitch4-Pro can be configured to monitor whether a short-circuit fault occurs across the output current sense resistor or a short-circuit fault across the IS to GND pins.

A fault is annunciated in the event the sensed current through IS pin does not exceed the programmed current limit threshold (bit [6:4] of ISSC register 0xA2) and switching frequency exceeding the programmed threshold (bit [3:2] of ISSC register 0xA2). The switching frequency can be selected in a range from 30 to 120 kHz. This must be carefully selected to suit the expected operating conditions of the design.

An IS pin short (ISSC) can be programmed to have a response to be a. No-Response, b. Latch-off (LO), c. Auto-restart (AR) or d. Disable Output (DO). In the event the behavior is a No-Response, the Telemetry Read-Back Fault Register is logged.

ISSC (0xA2): write to this address to specify the behavior for an IS-GND short.

Example: To set the behavior of an IS pin short to AR for switching frequency exceeding 30 kHz and current limit threshold of d'48: (0x36):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	ISSC register (0xA2)
Byte:	0x36 (8'b0011 0110)

The InnoSwitch4-Pro sets the CCSC fault register (READ 10 bit 2) once the voltage across the IS pin resistor exceeds more than ~3 times the $I_{SV(TH)}$. The CCSC register can be programmed to have response of a. No-Response, b. Latch-off (LO), c. Auto-restart (AR) or d. Disable Output (DO). In applications where the output capacitance after the series bus-switch exceeds 100 µF, the response for CCSC should be set to No-Response for proper start-up and may be programmed back to other fault response during normal operation after the series bus-switch is closed.

CCSC (0xA0): write to this address to specify the behavior for an output short-circuit.

Example: Set behavior of output short-circuit to No-response.

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	CCSC Register (0x20)
Byte:	0x00 (2'b00)

Setting CCSC register to No-Response and creating a short-circuit condition at output will result in Auto-Restart if switching frequency is $>f_{OVL}$ parameter for longer than t_{AR}.

Note: In operating conditions where InnoSwitch4-Pro primary tap or ClampZero tap turns on due to insufficient bias, resulting in undesired ringing on the FWD signal, the AR behavior may get affected and it is recommended to use Under Voltage AR in conjunction with CCSC when configured to AR response.

Series Bus Switch Short-Circuit Fault Protection

Series bus switch short-circuit fault is set in the event when sensed current through IS pin exceeds the programmed threshold (bit [5:4] of VBUSSC register 0xB6) and VBEN is disabled. There is option to program the number of current samples (1, 2, 3 or 4 consecutive samples) exceeding the set threshold before annunciating the fault.

A VBUS switch short (VBUSSC) can be programmed to have a response to be a. No-Response, b. Latch-off (LO) or c. Auto-restart (AR). In the event the behavior is a No-Response, the Telemetry Read-Back Fault Register is logged.

Watchdog Timer (0x26)

The Watchdog timer supervises the communication on the I^2C command lines and has an adjustable time-out. InnoSwitch4-Pro will go into a reset state if I^2C commands are not received within the programmable time interval. The watchdog timer does not engage until the master issues the first I^2C command (Read or Write). In the reset state the following occurs:

1. VBUS switch is Disabled (Series switch is open).
2. VOUT pin voltage regulates at the default 5 V threshold.
3. All command registers are cleared.

By writing 0x00 into register 0x26, the Watchdog timer is disabled. Disabling this feature can be useful in initial software debugging or checking functionality of the device on the bench.

Example: To disable the Watchdog timer:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	Watchdog Timer Register (0x26)
Byte:	0x00 (2'b00)

Opening and Closing the Series VBUS Switch (0x04)

Enabling VBEN (closing the VBUS series switch) speeds up the ADC sampling frequency in order to achieve high control accuracy. Write commands to CV register (0x10) and CC register (0x98) cannot be accepted faster than 80 ms when the VBEN is disabled (Series VBUS switch open).

Write 0x03 (with odd parity this becomes 0x83) into the VBEN register (0x04) to close the series VBUS switch and write 0x00 (with odd parity this becomes 0x80) to this register to open the switch. When the VBUS switch is open (VBEN disabled), the system is reset to the default output voltage set point of 5 V. Disabling the series VBUS switch also resets all the programmable command registers to their default values. The InnoSwitch4-Pro controller is in a state of reset when VBEN is disabled or the VDIS register is enabled.

For both these commands, since the controller is in reset, an ACK or Nack at the end of the command should not be expected.

InnoSwitch4-Pro also includes the option of bus switch open and no system reset. Write 0x01 (with odd parity 0x01) into the VBEN register (0x04) to open the switch without system reset. In this case, series bus switch is opened and the output voltage before the switch remains as configured previously in the CV register. All the programmable command registers do not reset to default values, instead retain the previous programmed configuration.

Enabling the VBEN register automatically disables the VDIS register (0x08) described in Active VOUT Pin Bleeder and Output Load Discharge Functions section.

Example: Enabling (Closing) the Series VBUS switch (0x83):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	VBEN Register (0x04)
Byte:	0x83 (8'b1000 0011)

Prior to sending command to open the series bus switch with system reset (0x00), a command to set the output voltage (CV register 0x10) to 5 V is recommended. In the event of an auto-restart or latch-off, the bus switch is not disabled. In the event of disable-output, the bus switch is disabled and system is reset to default configuration. The VBEN command must be sent to enable the series bus switch (close the switch) prior to increasing the output voltage above 16 V.

Turn-Off the Power Supply (0x8A)

The I²C master has the ability to turn-off the power supply (through an I²C command), which will require AC power cycling to restart the power supply.

Example: Turn-off the power supply:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	Turn-Off PSU Register (0x8A)
Byte:	0x01 (1'b1)

Fast VI Command

By default, the maximum speed in which CV (0x10) and CC (0x98) commands can be sent to program output voltage/current respectively is 10 msec. However, the speed limit can be removed by setting 0x1 to the Fast VI Command Register (0x8C).

Example: To disable speed limit for V/I commands:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	Fast VI Speed Register (0x8C)
Byte:	0x01 (1'b1)

Active VOUT Pin Bleeder and Output Load Discharge Functions

There may be circumstances where the VOUT pin strong bleeder function must be activated to discharge the output voltage from a high to low regulation set point. The VOUT bleeder can be activated by writing 0x01 into BLEEDER Register (0x86).

The BLEEDER register must not be enabled for extended period of time to prevent excessive power dissipation in the controller. When the BLEEDER function is being used to bleed the output voltage from high to low set point, the status of the VOUT10PCT register (bit 4 in the READ10 0x14 read register) should be used to disable the function.

The VOUT10PCT register is set once the output voltage is above 10% of the target regulation voltage.

The InnoSwitch4-Pro automatically disables SR pin when strong bleeder is enabled to save power.

The InnoSwitch4-Pro can also discharge the VBUS output voltage by bringing the VB/D pin to ground. The discharge circuit is a series diode + resistor tied from the VBUS output to the VB/D pin shown in the typical application schematic. The resistor selected should limit the current into VB/D pin within the max current limit specified in the electrical specifications.

Load discharge function can be activated by writing 0x03 (0x83 with odd parity) into VDIS register (0x08). Enabling the VDIS register will automatically disable the VBEN register (0x04) and reset the device to the default state.

The I²C master can use telemetry to monitor the VOUT pin voltage or a fixed timer to help determine when to disable both these functions.

In circumstances where device reset is not desirable, load discharge function can be activated without reset by writing 0x02 into VDIS register (0x08). This command will enable load discharge without device reset but doesn't disable the VBEN register – a separate command 0x01 must be written into VBEN register to disable bus switch without reset.

Example: Activate the Vout Bleeder:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	BLEEDER Register (0x86)
Byte:	0x01 (8'b0000 0001)

Example: Discharge the VBUS Output:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	VDIS Register (0x08)
Byte:	0x83 (8'b1000 0011)

Auto Bleeder Control for Reducing I²C Traffic

InnoSwitch4-Pro includes an option of Enable BLEEDER with Auto Disable feature. Writing 0x03 into the BLEEDER register (0x86) will enable the bleeder function which is automatically disabled when VOUT10PCT register is cleared.

Secondary Over-Temperature Protection (0xAE)

As the secondary controller die temperature increases beyond ~125 °C, the active VOUT pin bleeder function described above will be turned off. The bleeder will not be permitted to be re-enabled until the controller temperature falls below the programmable hysteresis value.

Example: Set Secondary OTP Hysteresis to 60 °C:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	OTP Register (0xAE)
Byte:	0x01 (1'b1)

Transient Response

If faster transient response is required in the application the InnoSwitch4-Pro includes command registers to reduce the time for low to high output voltage transitions. The command register addresses and recommended settings are shown in the table below:

Command Register Address	Default		Recommended for Speed Up	
	MSB	LSB	MSB	LSB
0x32	0x28	0x1E	0x14	0x0A
0x34	0x18	0xC8	0x1F	0x84

Using values other than the default or recommended settings about could lead to oscillatory behavior.

Constant Voltage Load

The constant current regulation mode in the InnoSwitch4-Pro can be optimized for constant voltage (CV) type load if this is required by the end application. Enabling this command register reduces the output current ripple for CV load only. The command register and setting below should only be used if CV load must be supported.

Command Register		Default		Recommended for CV Load	
Address	Address with Odd Parity	MSB	LSB	MSB	LSB
0x30	0xB0	0x00	0x1F	0x0A	0x20

DCM-Only

InnoSwitch4-Pro includes a feature to limit the switching cycle requests from secondary to primary such that converter always operates in the Discontinuous Conduction Mode (DCM).

At high-line, when a step load occurs, it would normally introduce one or more CCM cycles and raise the peak FW pin voltage. Enabling the DCM-only feature will limit this peak voltage and thereby reduce the stress on SR-FET.

DCM-only feature can be enabled/disabled through I²C command. Writing 0x04 into DCM-only register (0xBA) will enable this feature.

Example: Enable DCM-only mode:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	DCM-only Register (0xBA)
Byte:	0x04 (8'b0000 0100)

Telemetry (Read-back) Registers

Telemetry read registers (READ1 to READ7) show the content of all the command registers in Table 3. Telemetry read register addresses are grouped to allow optimal polling to get the power supply status in single I²C read back command with start and end telemetry addresses of interest.

Fault Registers

All the command registers including set voltage, set current, constant-power knee voltage, control (Series VBUS switch, VOUT pin Bleeder, Load discharge etc.) and all fault status can be read-back using the Telemetry functionality of the InnoSwitch4-Pro through I²C.

The READ10 telemetry registers are instantaneous and are cleared whenever the condition is no longer valid.

The READ16 (0x20) Register contains fault register data for auto-restart and latch-off. This register is only cleared when the BPS pin falls below its undervoltage threshold or the series VBUS switch is opened.

Example: Read the Fault Telemetry Register to determine an auto-restart occurred due to an output undervoltage (UV) Fault:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
Read Register:	0x80
Telemetry Register:	0x20
PI_SLAVE_ADDRESS [r]:	0x31 (8'b0011 0001)
PI_Slave Response:	Low Byte 8'b0000 0000 (0x00) High Byte 8'b0000 0010 (0x02)

Operating Mode Flag (OMF)

InnoSwitch4-Pro reports the mode of operation in telemetry register READ11 (0x16). It reports if InnoSwitch4-Pro is operating in CV, CP or CC mode. If interrupt mask is enabled, interrupt is raised whenever operating mode changes between CV, CP and CC modes. The OMF status of the supply should be read when in steady-state operation.

Main Regulation DAC Input

The READ14 telemetry register is the input into the main regulation loop that controls constant voltage, constant current and constant output power regulation. If this register is the same as the Set CV Register (0x10) the converter is operating in constant-voltage mode. If the READ14 is less than the Set CV Register (0x10) the converter is operating in constant-current (CC) or constant-power (CP) mode depending on the value of the Constant Power Knee Voltage Register (0x1A).

The output voltage from the READ14 register is computed as V_{OUT} = 5 V + (MSB × 100 mV) – (LSB x 10 mV).

Example: READ14 (0x1C): MSB = 0x00, LSB = 0x0E
LSB is d'14 so the computed V_{OUT} = 5 – (14 × 10 mV) = 4.86 V

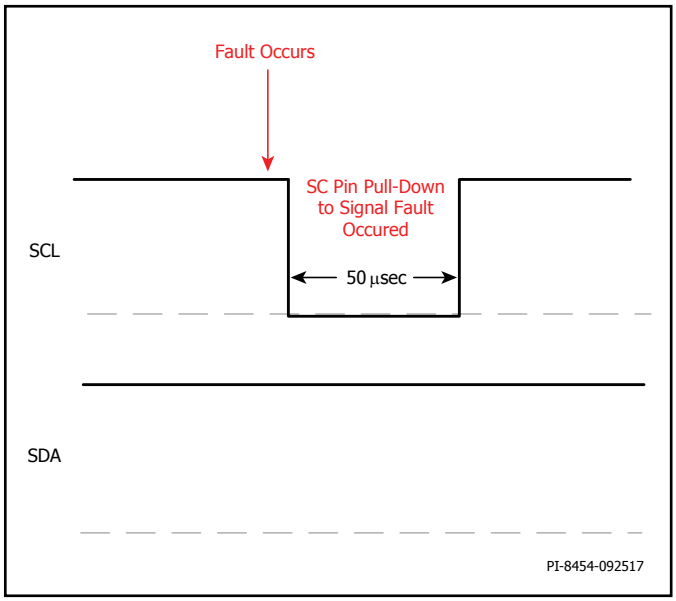


Figure 17. Interrupt Mask During Idle I²C.

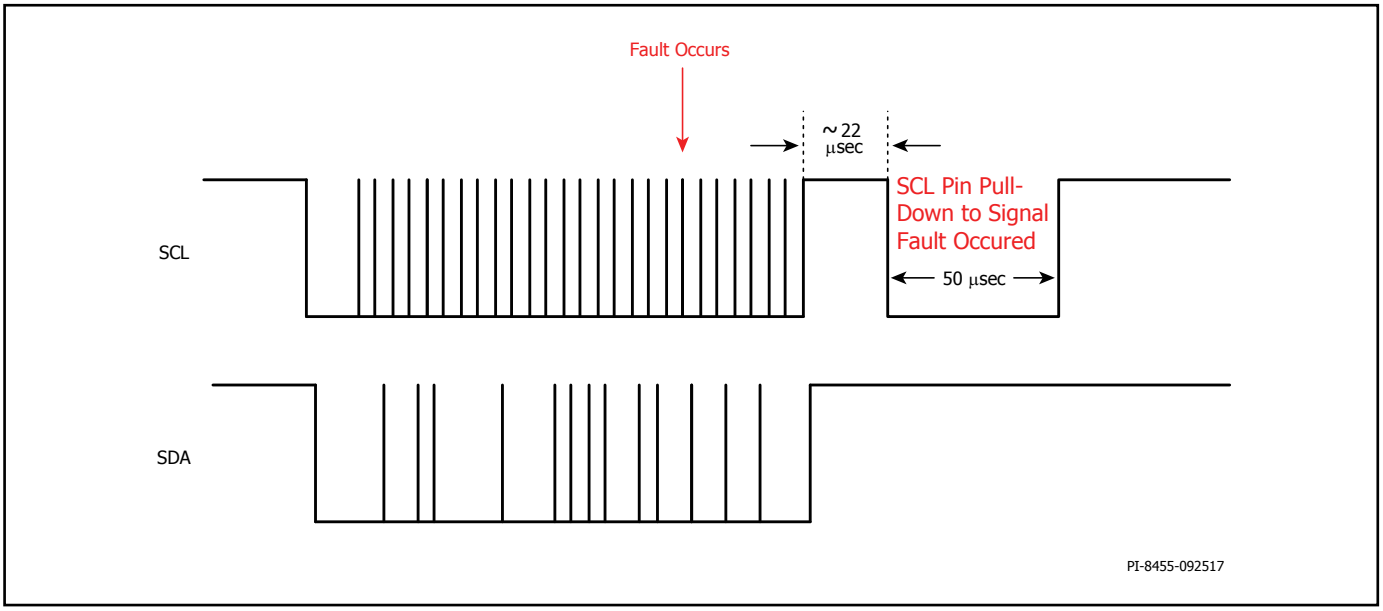


Figure 18. Interrupt Mask During Active I²C Transaction.

Fault Signaling Interrupt Through SCL Pin

In order to improve the fault reporting, an active interrupt reporting scheme is featured on the SCL pin during I²C idle state (when both SDA and SCL pins are pulled high).

When a fault occurs, the SCL pin will behave in one of the following two conditions:

1. When the SCL pin is in idle mode (see Figure 17), the fault interrupt will happen as soon as the fault is detected. The interrupt pulls down the SCL pin for 50 µsec then releases it back to HI State.
2. When the SCL pin is busy (active I²C transaction) (see Figure 16), the fault interrupt will wait for the I²C transaction to be completed, wait ~22 µsec and then pull down the SCL line for 50 µsec (minimum) then releases it back to HI State.

The Interrupt Mask Write Register (0x2C) must be enabled for each of the individual fault conditions. See Figure 19. In order to activate this feature. Once a fault occurs, the Interrupt is reset and the particular faults of interest must be re-enabled to activate the SCL reporting scheme.

The Interrupt Mask read register (0x22) will not be auto cleared when the interrupt triggers and will only reset when the Interrupt Mask write register is re-enabled. The Control Secondary Interrupt bit [6] is an indication that the secondary controller is waiting to handshake with primary. Several system faults could trigger this event such as primary-side thermal shutdown or an input line under or overvoltage condition.

Note 1: Any fault response configured as a No Response and Interrupt Mask enabled will result in an interrupt signal on the SCL pin.

Note 2: Any fault response configured as a Disabled Output and Interrupt Mask enabled results in a system reset when the fault is annunciated and the status of Interrupt signal on the SCL pin is ambivalent. It is recommended not to enable the Interrupt Mask for the faults that are configured to Disable Output response.

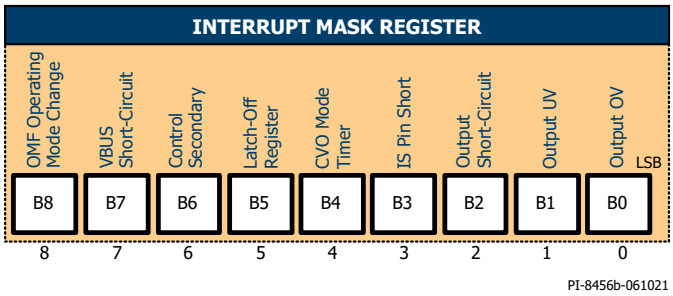


Figure 19. Interrupt Mask Register.

Example: Set the Interrupt Write Register to flag SCL pin fault for output OV, UV or short-circuit only:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	INTM Register (0x2C)
Byte:	0x07 (8'b0000 0111)

Output Voltage Measurement

The voltage on the VOUT pin is available on the Telemetry Register READ 9 (0x12). The tolerance of this telemetry register is ±3% over the entire regulation range of 3 to 24 V. When the output voltage is below 5 V at loads below ~50 mA, the voltage may fluctuate due to very low switching frequency of the converter but within the specified tolerance. This is normal and expected behavior.

The output voltage report back is in 12-bit format but the resolution depends on the output voltage range as shown in Table 5. This telemetry register is for indication only, in steady-state operation the VOUT pin is very tightly regulated per the CV Write Register (0x10) discussed in CV Register (0x10) section.

The report back resolution step size depending on output voltage is tabulated below:

Output Voltage Range (V)		Resolution Step Size
3	7.2	20 mV
7.2	10	50 mV
10	24	100 mV

Table 5. Output Voltage Report Back Resolution.

If the actual output voltage is 5.11 V (CV Write Register 0x10 set to 0x837F.)

The READ9 register will be at 5.10 V or 5.12 V since the resolution step size is 20 mV in this range

Example: If the READ 9 read-back register value is 0xA801 recalling that low byte precedes the high byte, the proper hex to decimal conversion would be from 0x01A8 = 424 in decimal.

The full output voltage range the report back should be divided by 10 mV to convert into actual output voltage, which in this example results in an output voltage of 4.24 V.

Read-back of the output voltage set-point READ1 (0x02) as with all the read registers is formatted with low-byte preceding the high-byte.

Output Current Measurement

The load output current is also available on the Telemetry Register.

Telemetry Register READ8 (0x10) contains the instantaneous measured relative output load current data. The load current is available on a relative basis with respect to the full-scale constant current regulation threshold programmed by the sense resistor tied between the IS and GND pin of the InnoSwitch4-Pro.

The ADC full range is 192, which denotes 100% threshold across the current sense resistor.

Example: If a 10 mΩ sense resistor is used and the read-back register is 0x8040.

Removing the odd parity bit from high byte results in 0x40 = 64 in decimal.

Sense current value = N(Decimal) x $0.167/R_{SENSE}$
64 x 0.167/10 = 1.068A. This is the measured output current value:

(0.167 mV = 32 mV/192, where 32 mV = $IS_{V(TH)}$ and 192 is ADC full range).

The READ12 and READ13 are 16 sample rolling averages of the measured output current and output voltage respectively. The value of these average registers is more stable than the instantaneous registers (READ8 and READ9) but take slightly longer to stabilize.

When the series BUS switch is opened these registers are cleared and values are reset to zero until the measurement start to accumulate. The resolution of READ 12 and READ 13 is the same as the READ8 and READ 9 respectively.

The output voltage and current measurement registers are updated every 100 µs.

I²C Connection

uVCC External Power Supply

The uVCC pin provides an accurately regulated 3.6 V supply to an external controller. The maximum load current capability of this supply is 40 mA for 0.5 seconds when the VOUT pin is greater than or equal to 5 V. For steady-state operation, it is expected the current drawn from uVCC is less than 10 mA. The uVCC pin should be decoupled to the GND pin with at least a 2.2 µF ceramic capacitor. When the VOUT pin voltage is less than 3.9 V, the internal LDO will droop and follow VOUT pin voltage. Under these conditions, the uVCC pin voltage is dependent on load current and internal series impedance. At VOUT pin = 3 V and 6 mA load current on uVCC, the expected output on uVCC will be 3 V – R_{UVCC} (Ω) × 6 mA.

If the VOUT pin voltage falls sufficiently to cause the uVCC pin to go below the $uVCC_{RST}$ threshold, communication through I²C is no longer available.

SCL/SDA Pull-up Requirements

The SCL and SDA-pins should be pulled-up to the uVCC pin with a resistor. The maximum pull-up resistance is dependent on the capacitance of the SCL/SDA pins and I²C Master. The resultant voltage fall-time to the VIL threshold assuming a total capacitance of 20 pF is tabulated as function of SCL clock frequency in the table below.

The InnoSwitch4-Pro part can be used with I²C frequency above 535 kHz, however there are specific timing requirements that need to be met as described in the data sheet parameter table and associated notes below the table.

Max Frequency (kHz)	Max Pull-Up Resistance (kΩ)	t_F (ns)
400	13	300
500	10	240
600	8	200
700	7	178

Table 6. I²C Pull-Up Resistor Values.

Meeting these requirements at frequencies above 535 kHz may require the interface IC to have the ability to produce asymmetrical 1²C CLK signals. If such ability is not available in the interface IC (or micro-controller connected to the InnoSwitch4-Pro through the I²C bus), it is recommended that I²C frequency of 535 kHz or lower is used.

I²C Example Waveforms

Setting The Output Voltage To 8 V

Same as Example shown in Figure 9.

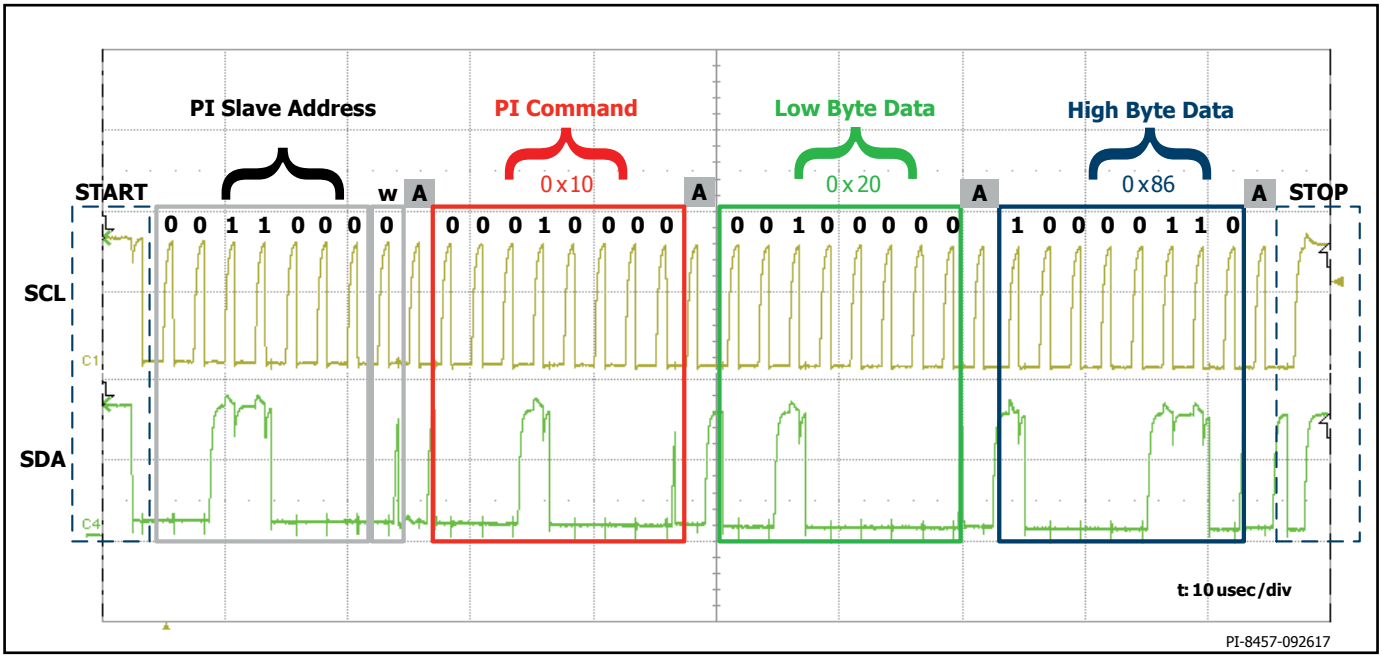


Figure 20. I²C Waveforms for Setting Output Voltage to 8 V.

Reading Telemetry Fault Register After AR Event Caused by Undervoltage

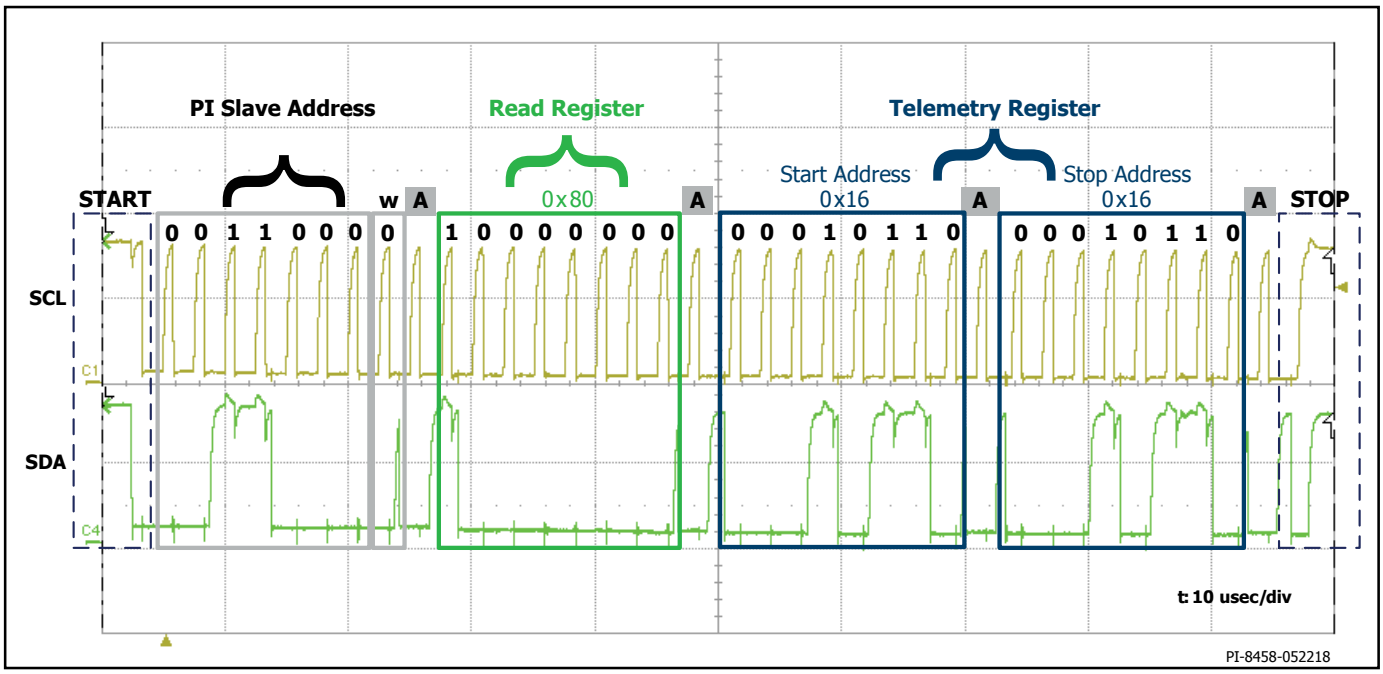


Figure 21. I²C Waveforms for Writing Address of Fault Register READ11 in Read Register (READ0) in Order to Read Back READ11.

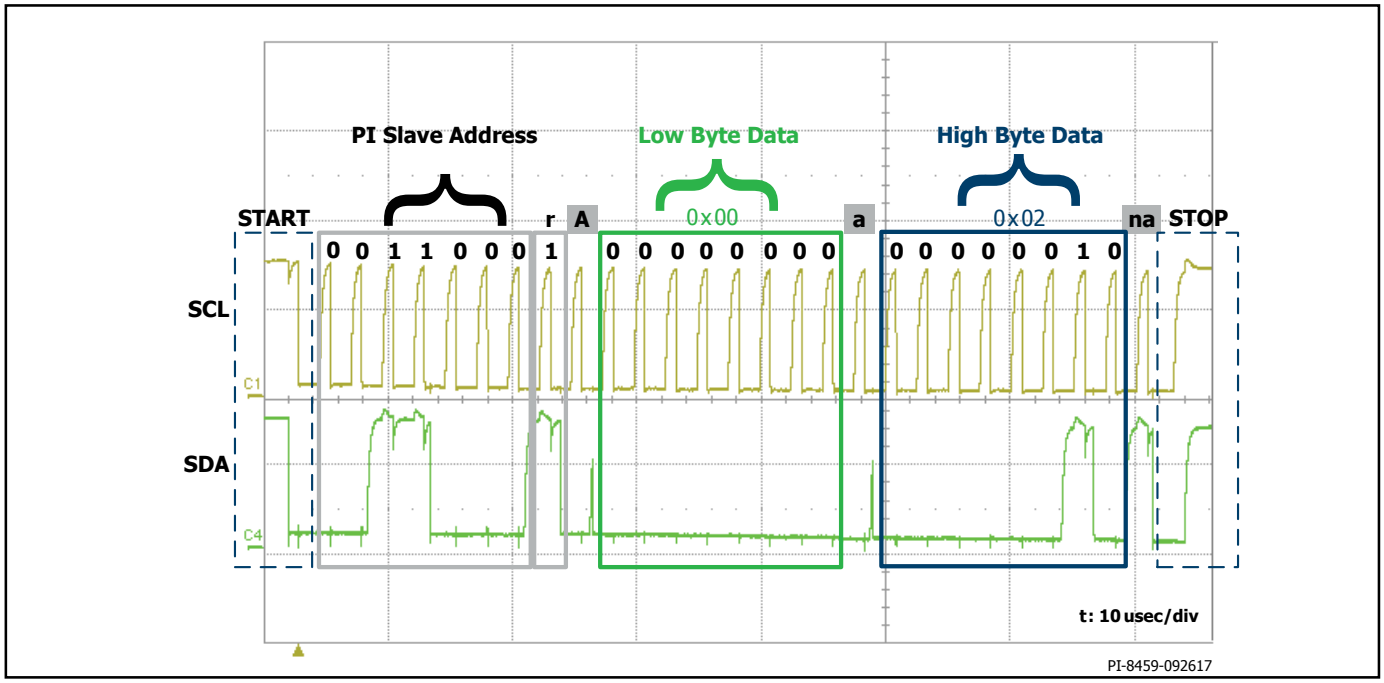


Figure 22. I²C Waveforms for Read Value From READ11 Register.

Applications Example

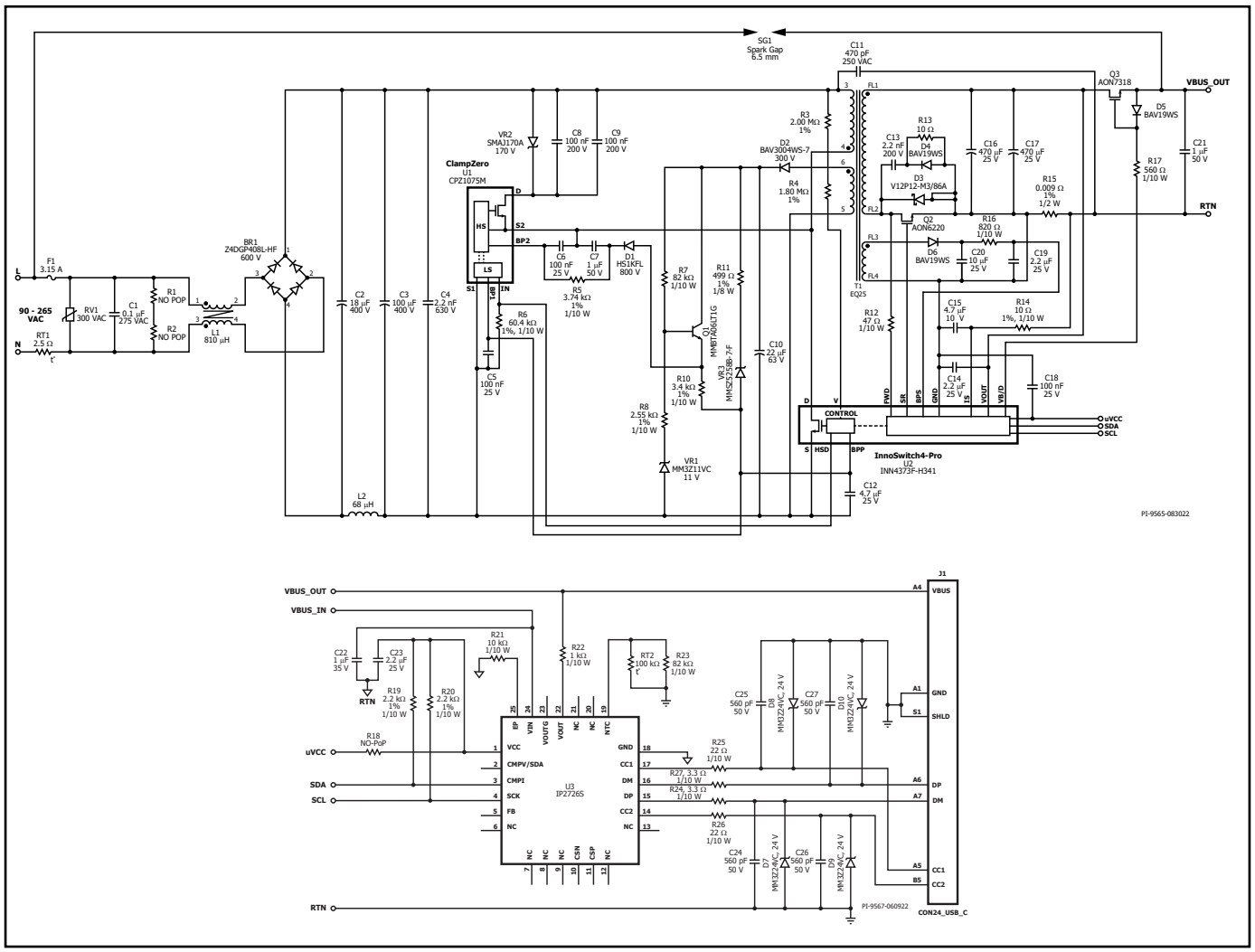


Figure 23. Schematic of 65 W USB PD Power Supply using INN4373F-H341 InnoSwitch4-Pro.

The circuit shown in Figure 23 is a 5 V, 3 A; 9 V, 3 A; 15 V, 3 A and 20 V, 3.25 A 65 W programmable power supply using the INN4373F-H341 IC. The power stage is controlled by Injoinic's IP2726S IC. This USB PD power supply is DOE level 6 and EC CoC v5 compliant.

Input fuse F1 isolates the circuit and provides protection from component failure. Common mode choke L1 along with Y capacitor C11 provides common mode noise filtering while inductor L2 forms a pi filter with capacitors C2 and C3 for differential mode EMI filtering along with C1. Inrush thermistor RT1 limits the inrush current when the power supply is connected to the AC input. MOV RV1 is used for surge protection. Bridge rectifier BR1 rectifies AC line voltage and provides full-wave rectified DC.

One end of the transformer primary is connected to the rectified DC bus; the other is connected to the drain terminal of the InnoSwitch4-Pro IC. Resistors R3 and R4 provide input voltage sense protection for under-voltage and overvoltage conditions.

The primary clamp formed by the body diode of the ClampZero IC and capacitors C8 and C9 limits the peak drain voltage of U2 at the instant of turn-off of the switch inside U2. The energy stored in the leakage inductance of the transformer will be transferred to capacitors C8 and C9. Part of the magnetizing energy will also get transferred to C8 and C9 depending on the capacitance value used. VR2 is used to protect the InnoSwitch4-Pro from excessive drain voltages during abnormal conditions. High-voltage ceramic capacitor C4 is used to decouple the bulk voltage, reducing the loop area of high frequency switching currents.

The InnoSwitch4-Pro generates an HSD (High-Side Drive) signal to turn on the ClampZero device when it is instructed to do so by the secondary-side through the internal FluxLink. When ClampZero IC (U1) turns on to achieve soft switching of InnoSwitch4-Pro primary switch, clamp capacitors C8 and C9 charges the leakage inductance of the transformer (CCM operation) or both the leakage and magnetizing inductance of the transformer (DCM operation).

A small delay is provided between the ClampZero switch (U1) turn-off and the turn-on of InnoSwitch4-Pro primary to achieve zero-voltage switching. This delay is either programmable by resistor R6 value at low-line input voltage (refer to page 5), or a fixed 500 ns delay at high-line input voltage. The transition between programmable delay and fixed delay is based on input line voltage information at the V pin of InnoSwitch4-Pro.

The IC U2 is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C12 when AC is first applied. During normal operation, the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C10. Linear regulator circuit comprises of BJT Q1, R7, R8, and Zener diode VR1 ensures sufficient current flows through R10 into the BPP pin of the InnoSwitch4-Pro and the BP1 pin of the ClampZero ICs. By injecting sufficient current into BPP and BP1 pins, the internal current source of U2 is not required to charge C12, and power consumption is minimized during no-load condition and at normal operation.

Capacitor C5 is used to provide local decoupling at the BP1 pin of IC U1. Capacitor C6 provides the decoupling for BP2 pin. Diode D1 and capacitor C7 form a bootstrap circuit to provide the bias for the high-side BP2 pin. Resistor R5 limits the current flowing into the BP2 pin. Providing an external bias prevents high-side internal tap turn-on and minimizes excess energy loss.

Zener diode VR3 offers primary sensed output overvoltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at the output of the converter, the auxiliary winding voltage increases and causes breakdown of VR3 which then causes excess current to flow into the BPP pin of InnoSwitch4-Pro IC. If the current flowing into the BPP pin increases above the I_{SD} threshold, the InnoSwitch4-Pro controller will latch off and prevent any further increase in output voltage. Resistor R11 limits the current injected to BPP pin when the output overvoltage protection is triggered.

Output regulation is achieved using modulation control where the frequency and I_{LIM} of switching cycles are adjusted based on output load. At high load, most switching cycles are enabled for a high value of I_{LIM} in the selected I_{LIM} range while at light load or no-load, most cycles are disabled and the ones enabled have a low value of I_{LIM} in the selected I_{LIM} range. Once a cycle is enabled, the switch remains ON until the primary current ramps to the device current limit for the specific operating state.

The secondary-side of the InnoSwitch4-Pro IC provides output voltage and current sensing and a gate drive to a FET for synchronous rectification. The voltage across the transformer secondary winding is rectified by the secondary-side synchronous rectifier FET (SR FET) Q2 and filtered by capacitors C16 and C17. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via an RCD snubber, R13, C13, and D4. Diode D4 minimizes the dissipation in resistor R13. Schottky diode D3 minimizes the losses that happen during the ClampZero switch conduction period.

The gate of Q2 is turned on by secondary-side controller inside IC U2, based on the secondary winding voltage sensed via resistor R12 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR FET is turned off just prior to the secondary-side commanding through FluxLink a new switching cycle from the primary. In discontinuous mode of operation, the SR FET is turned off when the magnitude of the voltage drop across the SR FET falls below a threshold of approximately $V_{SR(TH)}$. Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switches and provides extremely reliable synchronous rectifier operation.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. For this design, a secondary bias winding circuit is used to further improve the system efficiency. Bias winding voltage is rectified by diode D6 and filtered by capacitor C20. Resistor R16 limits the current flowing to the BPS pin of U2. Capacitor C19 connected to the BPS pin of InnoSwitch4-Pro IC provides decoupling for the internal circuitry.

The output current is sensed by monitoring the voltage drop across resistor R15. The current measurement is filtered with resistor R14 and capacitor C15, and then monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold of up to approximately 32 mV configured by the USB PD controller via I^2C interface is used to reduce the losses. Once the output current threshold is exceeded, the InnoSwitch4-Pro responds depending on its configuration to either maintain a fixed output current by using variable frequency and variable primary switch peak current control schemes or to shut down the power supply.

For constant current (CC) operation, when the output voltage falls below 5 V, the secondary-side controller inside InnoSwitch4-Pro IC will power itself from the secondary winding directly. During the on-time of the primary-side power switch, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C19 via resistor R12 and an internal regulator. This allows output current regulation to be maintained down to the minimum UV threshold. Below this level the unit enters auto-restart until the output load is reduced.

When the output current is below the CC threshold, the converter operates in constant voltage mode. The output voltage is monitored by the VOUT pin of the InnoSwitch4-Pro IC. Similar with current regulation, the output voltage is also compared to an internal voltage threshold that is set via the integrated secondary controller of the InnoSwitch4-Pro IC and the USB-PD controller IC, and output voltage regulation is achieved by variable frequency and variable primary switch peak current limit control schemes. Capacitor C14 is used as decoupling capacitor for the VOUT pin.

N-channel MOSFET Q3 functions as the bus switch which connects or disconnects the output of the flyback converter from the USB Type-C receptacle. MOSFET Q3 is controlled by the VB/D pin on the InnoSwitch4-Pro IC. Diode D5 is connected across the Source and Gate terminals of Q3 and resistor R17 is connected from the Gate terminal of Q3 to the VB/D pin to provide a discharge path for the bus voltage when Q3 is turned off. Capacitor C21 is used at the output for ESD protection and output voltage ripple reduction.

The Injoinic IP2726S (U3) is the USB Type-C and PD controller. Output of the InnoSwitch4-Pro IC U2 powers the IP2726S device directly from the flyback output voltage VBUS_IN. USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which type-C plug is connected.

The IP2726S IC communicates with InnoSwitch4-Pro IC through the I^2C interface using the SCL and SDA lines in which it sets several command registers, such as the CV, CC, VKP, OVA and UVA parameters. These parameters correspond to the output voltage, constant output current, constant output power voltage threshold, output overvoltage threshold, and output undervoltage threshold registers of the InnoSwitch4-Pro IC, respectively. The status of the InnoSwitch4-Pro IC is read by the IP2726S IC from the telemetry registers also using the I^2C interface.

Capacitor C18 is used as decoupling capacitor on uVCC pin of U2. Resistors R19 and R20 are used as pull-up resistors for SDA and SCL respectively.

Capacitor C22 is used as decoupling capacitor on VIN pin of U3 and capacitor C23 is used as decoupling capacitor on VCC pin of U3. Resistor R25, R26, C25, C26, D8 and D9 are used to protect the CC1 and CC2 lines from ESD surge events.

Key Application Considerations

Output Power Table
The data sheet output power table (Table 1) represents the maximum practical continuous output power level that can be obtained under the following conditions:

1. The minimum DC input voltage is 90 V or higher for 85 VAC input, 220 V or higher for 230 VAC input or 115 VAC with a voltage doubler. Input capacitor voltage should be sized to meet these criteria for AC input designs.
2. Efficiency assumptions depend on power level. Smallest device power level assumes efficiency >87% increasing to >92% for the largest device.
3. Transformer primary inductance tolerance of ±5%.
4. Reflected output voltage (VOR) is set to maintain K_p = 0.7 at minimum input voltage for universal line and K_p = 1 for high input line designs (for thermally constrained environment efficiency should be >92% with larger devices).
5. Maximum conduction losses for adapters are limited to 0.6 W, 0.8 W for open frame designs.
6. Increased current limit is selected for peak and open frame power columns and standard current limit for adapter columns.
7. The part is board mounted with SOURCE pins soldered to a sufficient area of copper and/or a heat sink to keep the SOURCE pin temperature at or below 110 °C.
8. Ambient temperature of 50 °C for open frame designs and 40 °C for sealed adapters.
9. Below a value of 1, K_p is the ratio of ripple to peak primary current. To prevent reduced power delivery, due to premature termination of switching cycles, a transient K_p limit of ≥0.25 is recommended. This prevents the initial current limit (I_{INT}) from being exceeded at switch turn-on.

Primary-Side Overvoltage Protection
Primary-side output overvoltage protection provided by the InnoSwitch4-Pro IC uses internal protection that is triggered by a threshold current of I_{SD} into the PRIMARY BYPASS pin. The protection response is dependent on the feature code of the device, either Latch-off or Auto-Restart. In addition to an internal filter, the PRIMARY BYPASS pin capacitor forms an external filter helping noise immunity. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the SOURCE and PRIMARY BYPASS pins of the device.

The primary sensed OVP function can be realized by connecting a series combination of a Zener diode and a resistor from the rectified and filtered bias winding voltage supply to the PRIMARY BYPASS pin. The rectified and filtered bias winding output voltage may be higher than expected (up to 1.5X or 2X the desired value) due to poor coupling of the bias winding with the output winding and the resulting ringing on the bias winding voltage waveform. It is therefore recommended that the rectified bias winding voltage be measured. This measurement should be ideally done at the lowest input voltage and with the highest load on the output. This measured voltage should be used to select the components required to achieve primary sensed OVP.

The Zener diode and resistor must be chosen such that the current drawn by BPP at the target OVP level exceeds the BPP shutdown threshold current I_{SD}. The Zener diode must not conduct during normal operation steady state and transient conditions so the clamping voltage must be higher than the difference of the bias capacitor voltage and BPP voltage during those conditions. For a more reliable design, the resistor value must also be chosen such that if the OVP Zener ever fails short, the current supplied to the BPP pin is below the absolute maximum rating of 100 mA.

Reducing No-Load Consumption
The InnoSwitch-4 Pro IC can start in self-powered mode, drawing energy from the BYPASS pin capacitor charged through an internal current source. Additionally, the internal current source also charges the BP1 pin decoupling capacitor of the ClampZero device at start-up. Use of a bias winding, however, is required to provide supply current to the PRIMARY BYPASS pin, once the InnoSwitch4-Pro IC has started switching. An auxiliary (bias) winding provided on the transformer serves this purpose. A bias winding driver supply to the PRIMARY BYPASS pin enables the design of power supplies with low no-load power consumption less than 30 mW. The high-side BP2 pin decoupling capacitor of the ClampZero device draws energy from the internal current source of ClampZero device, once the power supply starts switching. Resistor R8 shown in Figure 23 should be adjusted to achieve the lowest no-load input power.

Secondary-Side Overvoltage Protection
The secondary-side output overvoltage protection provided by the InnoSwitch4-Pro IC uses an internal protection circuit triggered by an input current exceeding a threshold of $I_{BPS(SD)}$ into the SECONDARY BYPASS pin. The protection response, either Latch-off or Auto-Restart is dependent on the feature code of the device. The direct output sensed OVP function can be realized by connecting a Zener diode from the output to the SECONDARY BYPASS pin. The Zener diode voltage needs to be the difference between 1.25 × V_{OUT} and 4.5 V (the SECONDARY BYPASS pin voltage). It is necessary to add a low value resistor in series with the OVP Zener diode to limit the maximum current into the SECONDARY BYPASS pin.

Selection of Components

Components for InnoSwitch4-Pro Primary-Side Circuit

BPP Capacitor
A capacitor connected from the PRIMARY BYPASS pin of the InnoSwitch4-Pro IC to GND provides decoupling for the primary-side controller and also selects current limit. A 0.47 µF or 4.7 µF capacitor may be used. Though electrolytic capacitors can be used, often surface mount multi-layer ceramic capacitors are preferred for use on double sided boards as they enable placement of capacitors close to the IC. Their small size also makes it ideal for compact power supplies. Capacitors rated for at least 10 V, 0805 or larger sizes with X5R or X7R dielectric are recommended to ensure that minimum capacitance requirement is met. The ceramic capacitor type designations, such as X7R, X5R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 5 V. Do not use Y5U or Z5U / 0603 rated MLCC due to this type of SMD ceramic capacitor has very poor voltage and temperature coefficient characteristics.

Bias Winding and External Bias Circuit
The internal regulated current source connected from the DRAIN pin of the switch to the PRIMARY BYPASS pin of the InnoSwitch4-Pro primary-side controller charges the capacitor connected to the PRIMARY BYPASS pin to achieve start-up. A bias winding should be provided on the transformer with a suitable rectifier and filter capacitor to create a bias supply that can be used to supply the required current for BP1 and BP2, determined by the I_{S1} and I_{S2} parameters of both InnoSwitch4-Pro and ClampZero. The turns ratio for the bias winding should be selected such that 7 V to 8 V minimum is developed across the bias winding at the lowest rated output voltage of the power supply at no-load condition. If the voltage is lower than this, no-load input power will increase.

In USB PD applications, the output voltage range is very wide. For example, a 45 W adapter would need to support 5 V, 9 V and 15 V and a 100 W adapter would have output voltages selectable from 5 V to 20 V. Such a wide output voltage variation results in a large change in bias winding output voltage as well.

A linear regulator circuit is generally required to limit the current injected into the PRIMARY BYPASS pin of the InnoSwitch4-Pro.

The bias current from the external circuit should be set to max of I_{S1} for InnoSwitch4-Pro + max of $I_{S1(1)}$ for ClampZero to achieve lowest no-load power consumption when operating the power supply at 230 VAC input, (V_{BPP} > 5 V). A glass passivated standard recovery rectifier diode with low junction capacitance is recommended to avoid the snappy recovery typically seen with fast or ultrafast diodes that can lead to higher radiated EMI.

An aluminum capacitor of at least 22 µF with a voltage rating 1.2 times greater than the highest voltage developed across the capacitor is recommended. Highest voltage is typically developed across this capacitor when the supply is operated at the highest rated output voltage and load with the lowest input AC supply voltage.

Line UV and OV Protection

Resistors connected from the UNDER/OVER INPUT VOLTAGE pin to the DC bus enable sensing of input voltage to provide line under voltage and overvoltage protection. For a typical universal input application, a resistor value of 4 MΩ is recommended.

InnoSwitch4-Pro features a primary sensed OV protection feature that can be used to latch-off the power supply. Once the power supply is latched off, it can be reset if the UNDER/OVER INPUT VOLTAGE pin current is reduced to zero. Once the power supply is latched off, even after the input supply is turned off, it can take considerable amount of time to reset the InnoSwitch4-Pro controller as the energy stored in the DC bus will continue to provide current to the controller. A fast AC reset can be achieved using the modified circuit configuration shown in Figure 24. The voltage across capacitor CS reduces rapidly after input supply is disconnected reducing current into the INPUT VOLTAGE MONITOR pin of the InnoSwitch4-Pro IC and resetting the InnoSwitch4-Pro controller.

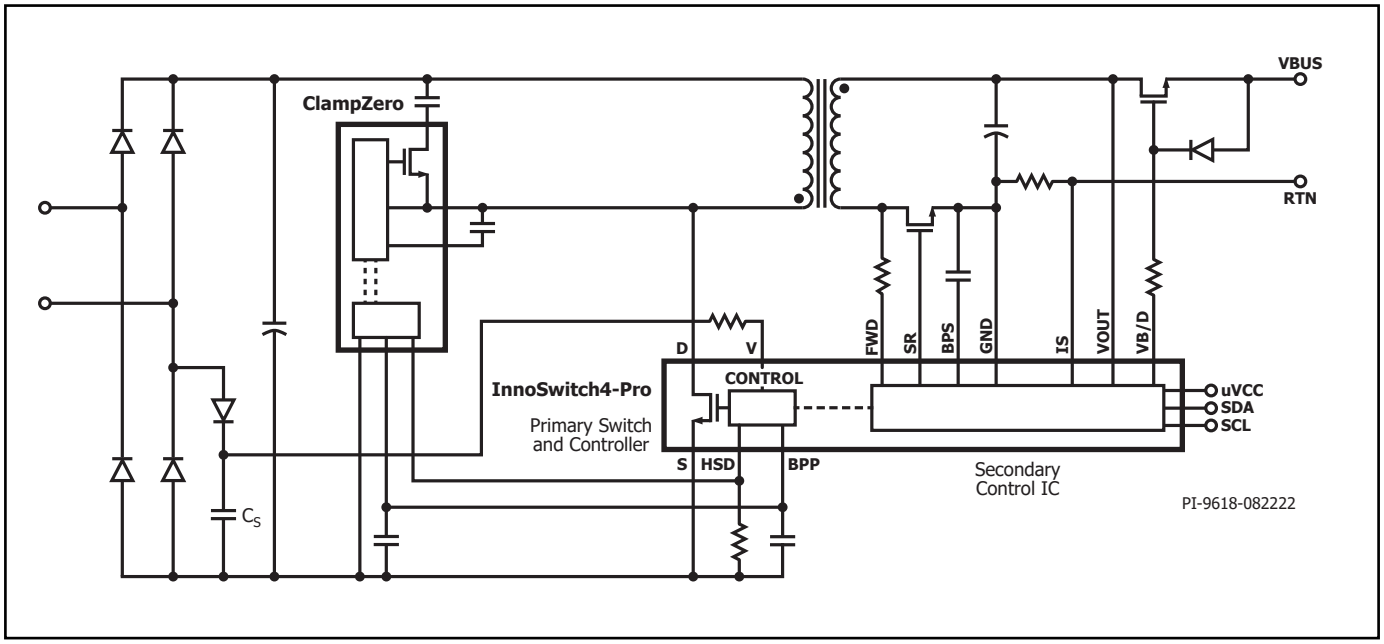


Figure 24. Fast AC Reset Configuration.

Primary-Side Clamp
ClampZero IC is used to provide soft switching at the turn-on of the InnoSwitch4-Pro primary switch as shown in Figure 23. Clamp capacitors C8 and C9 store the leakage energy when the primary switch is turned off and delivers the stored leakage energy to the secondary when the ClampZero device turns on while simultaneously charging up the leakage inductance in the reverse direction in CCM operation and charges both leakage and magnetizing inductance in the reverse direction during DCM operation. This prevents the excess voltage spike at the drain during the primary switch turn-off on a cycle-by-cycle basis. VR2 is used across the clamp capacitor just to provide backup protection in case ClampZero IC stops switching due to any circuit fault condition.

It is recommended to choose the value of the clamp capacitor such that ~0.25 times the resonant period of the C_{CLAMP} and L_{LKG} equals the HSD pulse width. Capacitance in the range of 10 nF to 200 nF may be used depending on the design. At least 200 V, 1206 or larger size rated X7R dielectric capacitors are recommended.

$$\text{HSD Pulse Width} = \frac{\Pi}{2}\sqrt{L_{LKG}C_{CLAMP}}$$

Components for InnoSwitch4-Pro Secondary-Side Circuit

SECONDARY BYPASS Pin - Decoupling Capacitor
A 2.2 µF, 10 V / X7R or X5R / 0805 or larger size multi-layer ceramic capacitor should be used for decoupling the SECONDARY BYPASS pin of the InnoSwitch4-Pro IC. Since the SECONDARY BYPASS pin voltage needs to be 4.5 V before the output voltage reaches the regulation voltage level, a significantly higher BPS capacitor value could lead to output voltage overshoot during start-up. Values lower than 1.5 µF may not offer enough capacitance, and cause unpredictable operation. The capacitor must be located adjacent to the IC pins. At least 10 V is recommended voltage rating to give enough margin from BPS voltage, and 0805 size is necessary to guarantee the actual value in operation since the capacitance of ceramic capacitors drops significantly with applied DC voltage especially with small package SMD such as 0603. 6.3 V / 0603 / X5U or Z5U type of MLCC is not recommended for this reason. The ceramic capacitor type designations, such as X7R, X5R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 4.5 V.

Capacitors with X5R or X7R dielectrics should be used for best results.

When the output voltage of the power supply is 5 V or higher, the supply current for the secondary-side controller is provided by the OUTPUT VOLTAGE (VOUT) pin of the IC as the voltage at this pin is higher than the SECONDARY BYPASS pin voltage. During start-up and operating conditions where the output voltage of the power supply is below 5 V, the secondary-side controller is supplied by current from an internal current source connected to the FORWARD pin.

If the power supply will operate in the upper range of the output voltage rating, deriving the secondary bias supply from VOUT will incur significant losses since it will be using an internal linear regulator. A bias winding may be provided from the transformer with suitable rectifier and filter to supply the required current to the BPS pin at the highest output voltage. This bias supply may not be able to supply the current required at lower output voltages since it scales with the output and should be greater than V_{BPS} (4.5 V).

FORWARD Pin Resistor
A 47 Ω, 5% resistor is recommended to ensure sufficient IC supply current. A lower resistor value should not be used as it can affect device operation such as the timing of the synchronous rectifier drive. A higher resistance value up to 300 Ω can be used to adjust synchronous rectifier gate drive duty and to limit negative current injection. It is recommended to add a parallel fast recovery diode in parallel with the resistor to allow enough current to charge BPP capacitor during start-up and also when output voltage regulated below 5 V. Diode anode is connected to the transformer winding while the cathode is connected to the FORWARD pin. Figure 25, 26, 27 and 28 show examples of unacceptable and acceptable FORWARD pin voltage waveforms. VD is forward voltage drop across the SR.

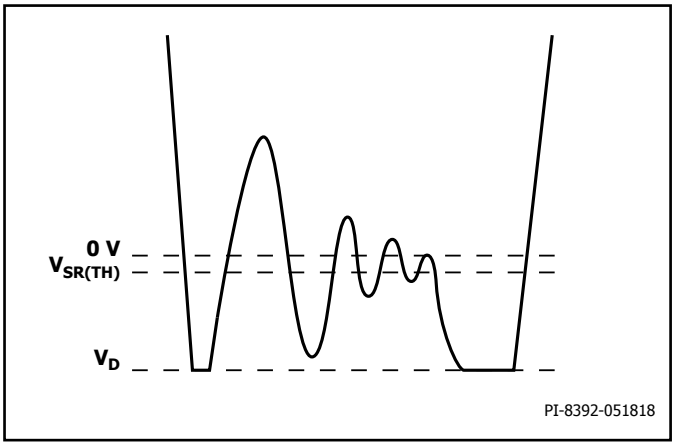


Figure 25. Unacceptable FORWARD Pin Waveform After Handshake with SR Switch Conduction During Flyback Cycle.

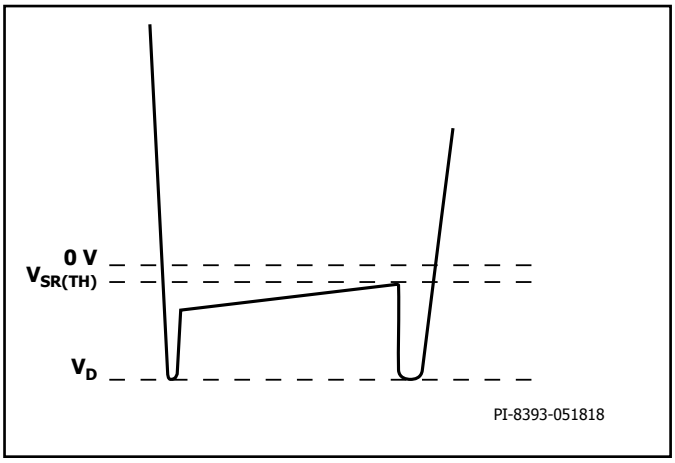


Figure 26. Acceptable FORWARD Pin Waveform After Handshake with SR Switch Conduction During Flyback Cycle.

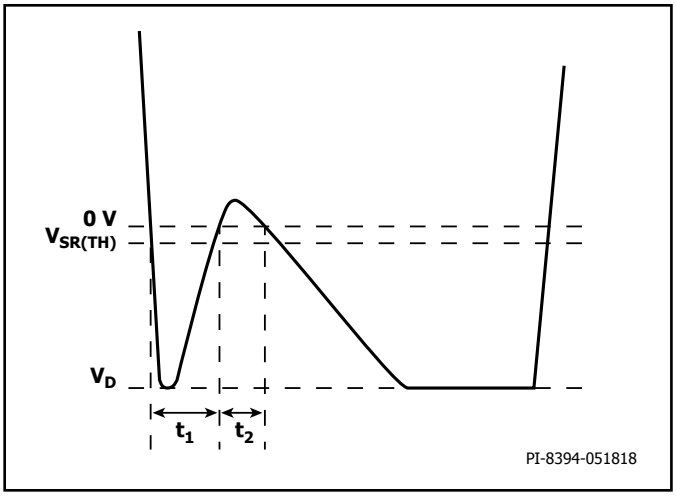


Figure 27. Unacceptable FORWARD Pin Waveform Before Handshake with Body Diode Conduction During Flyback Cycle.

Note:
If $t_1 + t_2 = 1.5\ \mu s \pm 50$ ns, the controller may fail the handshake and trigger a primary bias winding OVP latch-off/auto-restart.

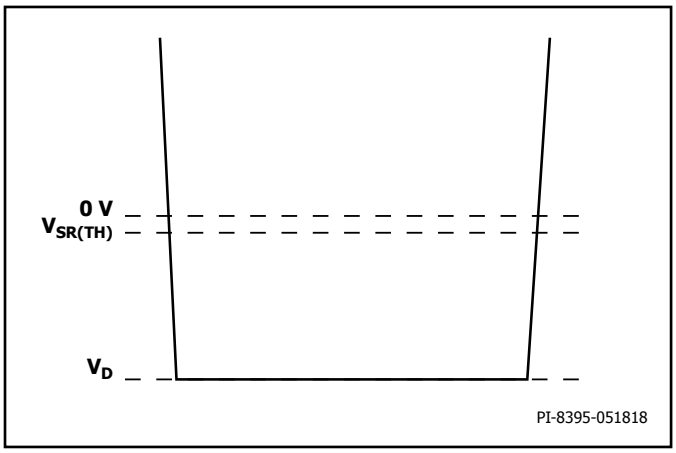


Figure 28. Acceptable FORWARD Pin Waveform Before Handshake with Body Diode Conduction During Flyback Cycle.

Synchronous Rectifier FET

Although a simple diode rectifier and filter works for the output, the use of an SR FET enables the significant improvement in operating efficiency often necessary to meet the European CoC and the U.S. DoE energy efficiency requirements. The secondary-side controller turns on the SR FET once the flyback cycle begins. The SR FET gate should be tied directly to the SYNCHRONOUS RECTIFIER DRIVE pin of the InnoSwitch4-Pro IC (no additional resistors should be connected in the gate circuit of the SR FET). The SR FET is turned off once the VDS of the SR FET reaches the turn off threshold.

The following table provides a recommendation for the SR FET $R_{DS(ON)}$ selection for different designs.

Output	FET $R_{DS(ON)}$
20 V / 3 A	7 mΩ
20 V / 5 A	4.5 mΩ
20 V / 6.75 A	3 mΩ

Table 7. Recommended SR FET $R_{DS(ON)}$ for Different Designs.

The SR FET driver uses the SECONDARY BYPASS pin for its supply rail, and this voltage is typically 4.5 V. A FET with a high threshold voltage is therefore not suitable; FETs with a threshold voltage of 1.5 V to 2.5 V are ideal although switches with a threshold voltage (absolute maximum) as high as 4 V may be used provided their data sheets specify $R_{DS(ON)}$ across temperature for a gate voltage of 4.5 V.

A Schottky diode is recommended across the SR FET. Since the SR FET gate turns off during the ClampZero switch conduction period, there will be energy transfer to secondary during this period typically about 500 ns. In addition to this there is a slight delay between the commencement of the flyback cycle and the turn-on of the SR FET. During this time, the body diode of the SR FET conducts. If an external parallel Schottky diode is used, this current mostly flows through the Schottky diode. Once the InnoSwitch4-Pro IC detects end of the flyback cycle, voltage across SR FET $R_{DS(ON)}$ reaches 0 V, any remaining portion of the flyback cycle is completed with the current commutating to the body diode of the SR FET or the external parallel Schottky diode. The Schottky diode in parallel with the SR FET is required to reduce the stress on the SR FET during clamp-fet turn-off. An efficiency increase of 0.20% or higher is expected with the addition of Schottky diode for designing with an output current rating >2 A.

The voltage rating of the Schottky diode and the SR FET should be at least 1.4 times the expected peak inverse voltage (PIV) based on the turns ratio used for the transformer. 60 V rated FETs and diodes are suitable for most 5 V designs that use a V_{OR} < 60 V, and 120 V rated FETs and diodes are suitable for 20 V designs.

The interaction between the leakage reactance of the output windings and the SR FET capacitance (C_{OSS}) leads to ringing on the voltage waveform at the instance of voltage reversal at the winding due to the primary switch turn-on. This ringing can be suppressed using an RC snubber connected across the SR FET. A snubber resistor in the range of 10 Ω to 47 Ω may be used (higher resistance values lead to a noticeable drop in efficiency). A capacitance value of 220 pF to 2.2 nF is adequate for most designs. A switching diode can be paralleled with the snubber resistor to minimize its dissipation.

Output Capacitor

Low ESR aluminum electrolytic capacitors are suitable for use with most high frequency flyback switching power supplies though the use of aluminum-polymer solid capacitors has gained considerable popularity due to their compact size, stable temperature characteristics, extremely low ESR and high RMS ripple current rating. These capacitors enable the design of ultra-compact chargers and adapters.

Typically, 200 μF to 300 μF of aluminum-polymer capacitance per ampere of output current is adequate. The other factor that influences the choice of capacitance is the output ripple. Ensure that capacitors with a voltage rating higher than the highest output voltage plus sufficient margin is used.

Output Overload Protection

The maximum power which can be delivered by the power supply is obtained by the product of the programmed VKP and the full scale current limit. For output voltage below the programmed VKP threshold, the InnoSwitch4-Pro IC will limit the output current once the programmed current limit is reached. The full scale current limit is set by the resistor between the IS and GND pins. A lower value of the current limit can be programmed over I²C. For any output voltage above the programmed VKP threshold, InnoSwitch4-Pro IC will provide a constant power characteristic. An increase in load current within the programmed current limit will result in a drop in output voltage such that the product of output voltage and current equals the maximum power set by the product of VKP and the full scale current limit.

Decoupling Capacitor at µVCC Pin
It is recommended that at least a 2.2 µF ceramic capacitor be placed between the uVCC and GND pins.

Pull-Up Resistors for SDA and SCL Pins
A 4.7 kΩ pull-up resistor from each of the SDA and SCL pin to the uVCC pin is recommended for communication at a frequency of 400 kHz. The maximum value of the pull-up resistor is dependent on the capacitance presented by the SDA/SCL lines and the I²C master. The resultant voltage rises to the V_{IL} threshold assuming a total capacitance of 20 pF is tabulated as a function of SCL clock frequency in Table 7.

Decoupling Capacitor at VOUT Pin
It is recommended that a 1-2.2 µF ceramic capacitor be placed close to the VOUT pin.

IS to GND Pin Current Sense Resistor
This sense resistor is chosen such that the required full scale current produces a 32 mV drop across IS and GND pins. A 1% or lower tolerance resistor is recommended. This sense resistor needs to be placed as close to the InnoSwitch4-Pro IC pins as possible for accurate current measurement and CC regulation.

Output Decoupling Capacitor
A ceramic output decoupling capacitor up to 10 µF is required to pass 18 kV ESD air discharge. This capacitor must be placed as close as possible to output terminals or Type-C connector of the power supply.

Bus Switch
A low $R_{DS(ON)}$ N-channel FET bus switch is recommended to reduce impact of high load currents on efficiency. The FET need not be a logic level FET. VB/D can supply typically 7 V above VOUT so it can sufficiently enhance FETs with gate threshold of 4 V.

Bus Discharge
The resistor value for bus discharge is chosen as per the discharge time requirements for high-voltage to low-voltage transitions, also considering the VB/D pin internal current discharge limit $I_{B/D(DS)}$ of 50 mA. A 560 Ω resistor value is recommended for 20 V designs to meet the USB PD discharge time specification. A general purpose diode in series is recommended across the bus switch Source to Gate pins for unidirectional current flow.

External Controller
An external controller is needed to send the I²C commands to the InnoSwitch4-Pro IC over the SDA and SCL lines. For standalone applications, the external controller can get its supply from the uVCC pin of the InnoSwitch4-Pro IC. It should be able to sustain operation for a supply voltage as low as 2.8 V.

Recommendations for Circuit Board Layout

See Figure 29 for a recommended circuit board layout for an InnoSwitch4-Pro based power supply.

Single-Point Grounding
Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

Bypass Capacitors
The PRIMARY BYPASS and SECONDARY BYPASS pin capacitor must be located directly adjacent to the PRIMARY BYPASS-SOURCE and SECONDARY BYPASS-SECONDARY GROUND pins respectively and connections to these capacitors should be routed with short traces.

Primary Loop Area
The area of the primary loop that connects the input filter capacitor, transformer primary and IC should be kept as small as possible.

IS to GND Pin Capacitor
A 1 µF or higher ceramic capacitor is recommended to be used between the IS and GND pins of the InnoSwitch4-Pro IC for accurate constant current regulation.

Primary Clamp Circuit
Active clamp is used to achieve the ZVS turn-on on the primary switch and to limit the peak voltage on the drain pin at turn-off. ClampZero IC is used along with clamp capacitor to achieve this. To reduce EMI, minimize the loop from the clamp components to the transformer and InnoSwitch4-Pro.

Thermal Considerations
The SOURCE pin is internally connected to the IC lead frame and provides the main path to remove heat from the device. Therefore, the SOURCE pin should be connected to a copper area underneath the IC to act not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, it can be maximized for good heat sinking without compromising EMI performance. Similarly, for the output SR switch, maximize the PCB area connected to the pins on the package through which heat is dissipated from the SR switch.

Sufficient copper area should be provided on the board to keep the IC temperature safely below the absolute maximum limits. It is recommended that the copper area provided for the copper plane on which the SOURCE pin of the IC is soldered is sufficiently large to keep the IC temperature below 110 °C when operating the power supply at full rated load and at the lowest rated input AC supply voltage.

Y Capacitor
The Y capacitor should be placed directly between the primary input filter capacitor positive terminal and the output positive or return terminal of the transformer secondary. This routes high amplitude common-mode surge currents away from the IC. Note: if an input pi-filter (C, L, C) EMI filter is used then the inductor in the filter should be placed between the negative terminals of the input filter capacitors.

Output SR FET
For best performance, the area of the loop connecting the secondary winding, the output SR switch and the output filter capacitor, should be minimized.

IS-GND Pin, Sense Resistor Traces
It is recommended to have the traces from the current sense resistor to the IS-GND pins to be in a star connection at the respective two nodes of the current sense resistor in order to have an accurate CC set-point. The IS-GND sense traces should be at the innermost of the solder pads of the current sense resistor to avoid measuring any drop across the solder pads of the resistor or the load traces coming in and out of the sense resistor.

uVCC, SDA and SCL Pins
The traces to SDA and SCL pins should be kept away from any noisy node or trace. If possible a shield trace should be made in parallel to the SDA and SCL traces.

ESD
Sufficient clearance should be maintained (>8 mm) between the primary-side and secondary-side circuits to enable easy compliance with any ESD / HIPOT requirements. The spark gap is best placed directly between output positive rail and one of the AC inputs. In this configuration, a 6.2 mm spark gap is often sufficient to meet the creepage and clearance requirements of many applicable safety standards. This is less than the primary to secondary spacing because the voltage across spark gap does not exceed the peak of the AC input.

If there is a controller used for USB PD communication then the Ground of the controller should be connected to the GND pin of the InnoSwitch4-Pro IC and not the GND pin of the type C connector, this helps with better ESD performance. However, if there is a separate daughter board connected with the controller IC on it and the Ground path becomes long then the Ground of the controller IC can be connected closer to the USB connector GND pins to help in the eye diagram during USB PD compliance tests.

Drain Node
The drain switching node is the dominant noise generator. As such the components connected the drain node should be placed close to the IC and away from sensitive feedback circuits. The clamp circuit components should be located physically away from the PRIMARY BYPASS pin and trace lengths minimized.

The area of the loop comprising of the input rectifier filter capacitor, the primary winding and the IC primary-side switch should be kept as small as possible.

Layout Example

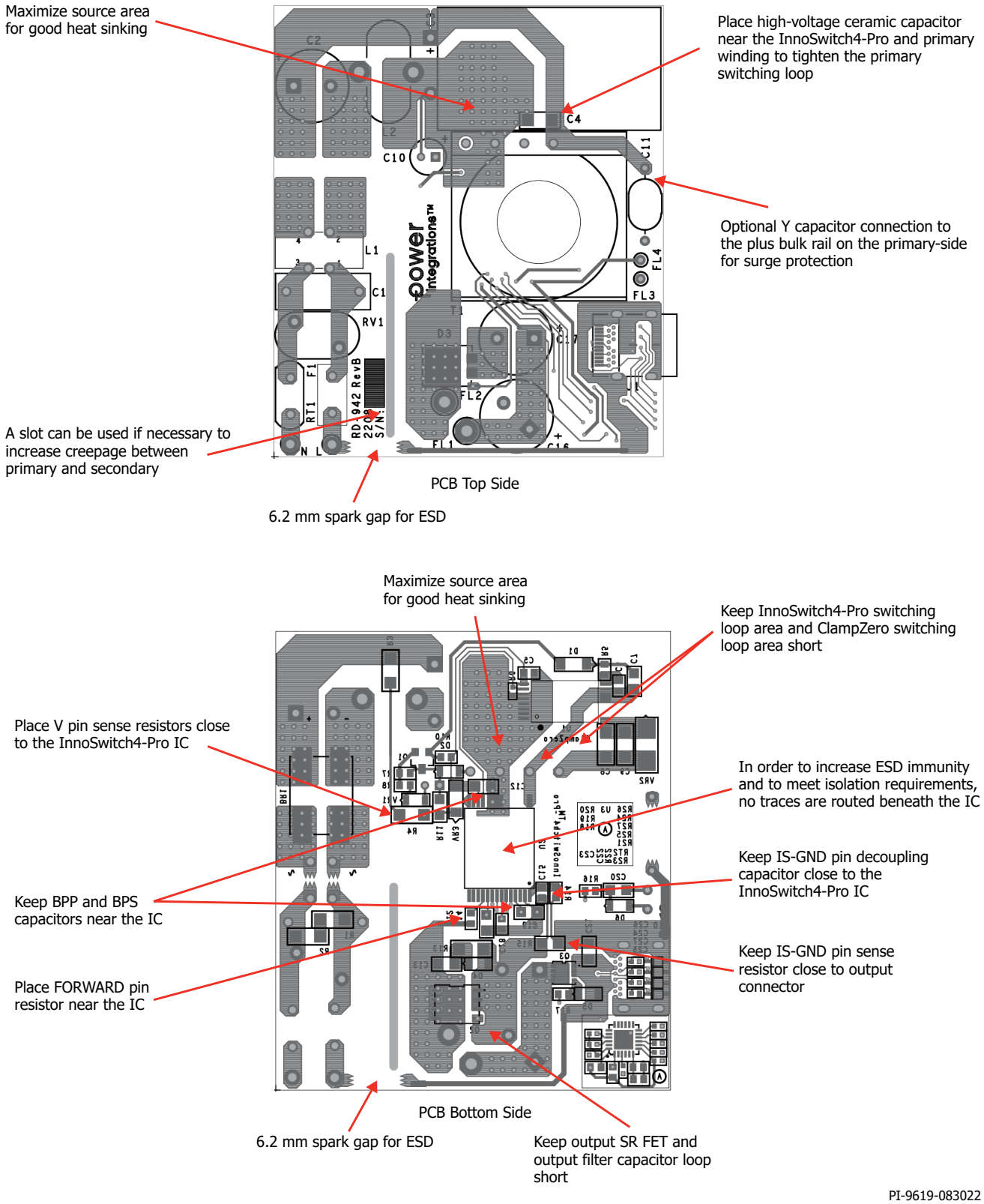


Figure 29. PCB Layout Recommendation.

Recommendations for EMI Reduction

1. Appropriate component placement and small loop areas of the primary and secondary power circuits help minimize radiated and conducted EMI. Care should be taken to achieve a compact loop area.
2. A resistor in series with the bias winding helps reduce radiated EMI.
3. Common mode chokes are typically required at the input of the power supply to sufficiently attenuate common mode noise. However, the same performance can be achieved by using shield windings on the transformer. Shield windings can also be used in conjunction with common mode filter inductors at input to improve conducted and radiated EMI margins.
4. Adjusting SR switch RC snubber component values can help reduce high frequency radiated and conducted EMI.
5. A pi-filter comprising differential inductors and capacitors can be used in the input rectifier circuit to reduce low frequency differential EMI.
6. A 1 µF ceramic capacitor connected at the output of the power supply helps to reduce radiated EMI.

Recommendations for Transformer Design

Transformer design must ensure that the power supply delivers the rated power at the lowest input voltage. The lowest voltage on the rectified DC bus depends on the capacitance of the filter capacitor used. At least 2 µF/W is recommended to always keep the DC bus voltage above 70 V, though 3 µF/W provides sufficient margin. The ripple on the DC bus should be measured to confirm the design calculations for transformer primary-winding inductance selection. PI Expert Online (https://piexpertonline.power.com/) can be used to easily create designs for InnoSwitch4-Pro.

Switching Frequency (f_{SW})

It is a unique feature in InnoSwitch4-Pro that for full load, the designer can set the switching frequency to between 50 kHz to 130 kHz. For a smaller transformer, the full load switching frequency could be set to 130 kHz. When setting the full load switching frequency it is important to consider primary inductance and peak current tolerances to ensure that average switching frequency does not exceed 140 kHz which may trigger auto-restart due to overload protection.

Table 8 provides a guide for switching frequency selection based on device size. This represents the best compromise between the overall device losses based on the internal high-voltage switch and transformer size.

Device	Recommended Full Load Switching Frequency
INN4373F	90-110 kHz
INN4375F	70-90 kHz
INN4377F	60-80 kHz

Table 8. Recommended Switching Frequency for Different Devices*.

*The higher size devices have lower $R_{DS(ON)}$ and higher I_{LIM} and are intended for use in higher power applications (>75 W). In accordance with IEC standards, these designs have to meet the harmonic current requirements and thus need a power factor correction front end. It is assumed for these designs that the input voltage to the DC-DC section is in the range of 380-400 VDC.

Reflected Output Voltage, V_{OR} (V)

This parameter describes the effect on the primary switch drain voltage of the secondary-winding voltage during diode/SR conduction which is reflected back to the primary through the turns ratio of the transformer. To make full use of ZVS capability and ensure flattest efficiency over line/load, set reflected output voltage (V_{OR}) to maintain K_P = 0.7 at minimum input voltage for universal input and K_P = 1 for high-line-only conditions.

Consider the following for design optimization:

1. Higher V_{OR} allows increased power delivery at V_{MIN}, which minimizes the value of the input capacitor and maximizes power delivery from a given InnoSwitch4-Pro device.
2. Higher V_{OR} reduces the voltage stress on the output diodes and SR switches.
3. Higher V_{OR} increases leakage inductance which reduces power supply efficiency.
4. Higher V_{OR} increases peak and RMS current on the secondary-side which may increase secondary-side copper and diode losses.

There are some exceptions to this. For very high output currents the V_{OR} should be reduced to get highest efficiency. For output voltages above 15 V, V_{OR} should be higher to maintain an acceptable PIV across the output synchronous rectifier.

Output Voltage	Optimal Range for V_{OR}
5 V	45-70
12 V	80-120
15 V	100-135
20 V	120-160
24 V	135-180

Table 9. Recommended V_{OR} for Optimal Performance.

Ripple to Peak Current Ratio, K_P

A K_P below 1 indicates continuous conduction mode, where K_P is the ratio of ripple-current to peak-primary-current (Figure 30).

$$K_P \equiv K_{RP} = I_R / I_P$$

A value of K_P higher than 1, indicates discontinuous conduction mode (Figure 31). In this case K_P is the ratio of primary switch off-time to the secondary rectifier conduction-time.

$$K_P \equiv K_{DP} = (1 - D) \times T/ t = V_{OR} \times (1 - D_{MAX}) / ((V_{MIN} - V_{DS}) \times D_{MAX})$$

It is recommended that a K_P close to 0.7 at the minimum expected DC bus voltage should be used for most InnoSwitch4-Pro designs. Since InnoSwitch4-Pro provides ZVS benefit a K_P value of <1 results in lower primary-side switch losses and higher transformer efficiency by lowering the primary RMS current.

For typical USB PD and rapid charge designs which require a wide output voltage range, K_P will change significantly as the output voltage changes. K_P will be high for high output voltage conditions and will drop as the output voltage is lowered. The PIXls spreadsheet can be used to effectively optimize selection of K_P, inductance of the primary winding, transformer turns ratio, and the operating frequency while ensuring appropriate design margins.

Core Type

Choice of a suitable core is dependent on the physical limits of the power supply enclosure. It is recommended that only cores with low loss be used to reduce thermal challenges.

Safety Margin, M (mm)

For designs that require safety isolation between primary and secondary that are not using triple insulated wire, the width of the safety margin to be used on each side of the bobbin is important. For universal input designs, a total margin of 6.2 mm is typically required – 3.1 mm on either side of the winding. For vertical bobbins the margin may not be symmetrical. However, if a total margin of 6.2 mm is required then the physical margin can be placed on only one side of the bobbin. For designs using triple insulated wire it may still be necessary to add a small margin in order to meet required creepage distances. Many bobbins exist for each core size and each will have different mechanical spacing. Refer to the bobbin data sheet or seek guidance to determine what specific margin is required. As the margin reduces the available area for the windings, the winding area will disproportionately reduce for small core sizes.

It is recommended that for compact power supply designs using an InnoSwitch4-Pro IC, triple-insulated wire be used for the secondary windings.

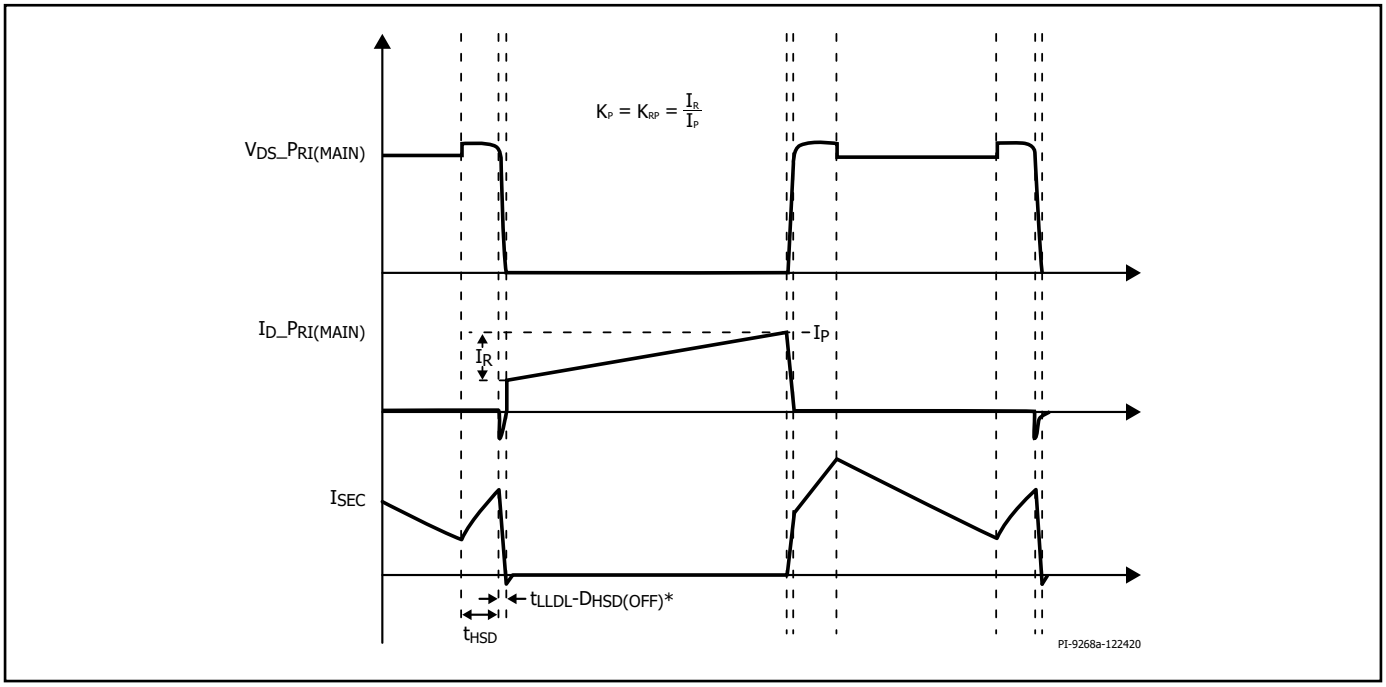


Figure 30. Continuous Conduction Mode Current Waveform at Low-Line, K_P < 1. *$D_{HSD(OFF)}$ is delay from HSD low to ClampZero OFF, please refer to ClampZero data sheet.

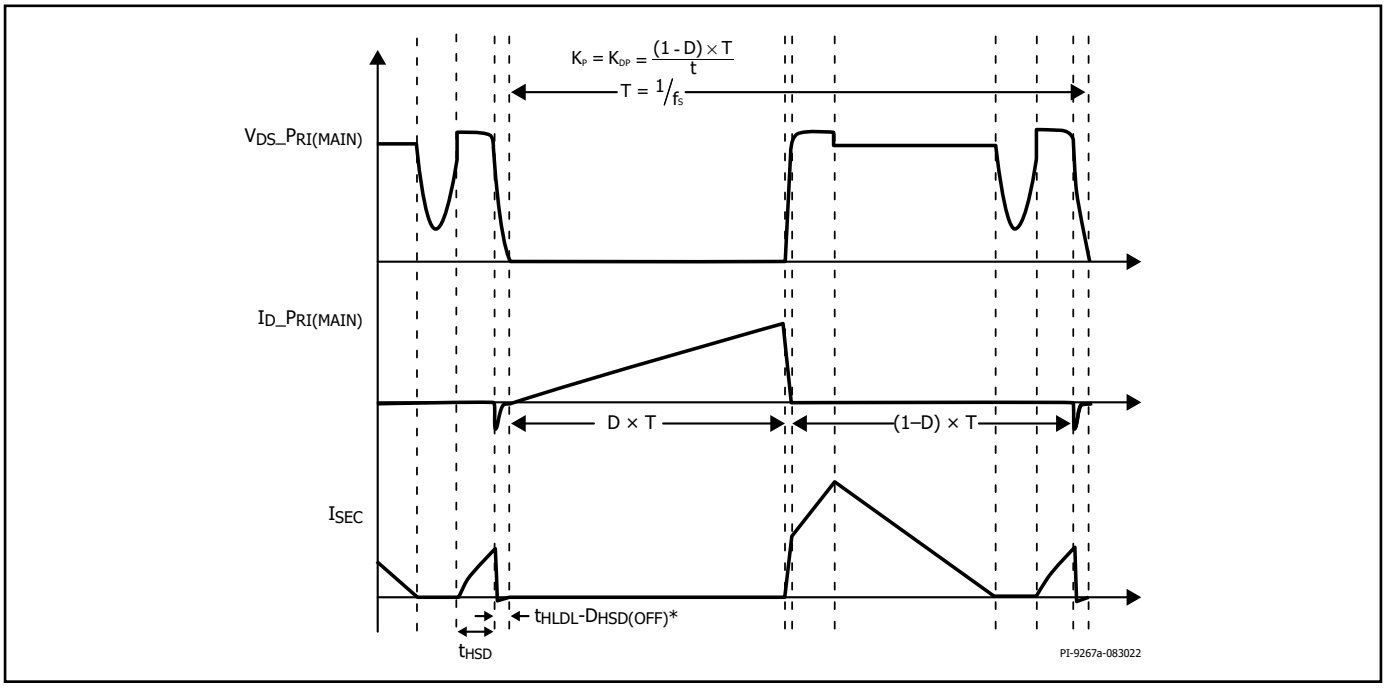


Figure 31. Discontinuous Conduction Mode Current Waveform at High-Line, K_P > 1. *$D_{HSD(OFF)}$ is delay from HSD low to ClampZero OFF, please refer to ClampZero data sheet.

Primary Layers, L
Primary layers should be in the range of 1 ≤ L ≤ 3 and in general should be the lowest number that meets the primary current density limit (CMA). A value of ≥200 Cmils / Amp can be used as a starting point for most designs. Higher values may be required due to thermal constraints. For universal input designs minimum 2% leakage inductance is required to achieve ZVS during CCM operation. However, for DCM only designs it is recommended to minimize leakage inductance. Designs with more than 3 layers are possible but the increased leakage inductance and the physical fit of the windings should be considered. A split primary construction may be helpful for DCM only designs. In split primary construction, half of the primary winding is placed on either side of the secondary (and bias) winding in a sandwich arrangement. This arrangement is often disadvantageous for low power designs as this typically increases common mode noise and adds cost to the input filtering.

Maximum Operating Flux Density, B_M (Gauss)
A maximum value of 3800 Gauss at the peak device current limit (at 180 kHz) is recommended to limit the peak flux density at start-up and under output short-circuit conditions. Under these conditions the output voltage is low and little reset of the transformer occurs during the switch off-time. This allows the transformer flux density to staircase beyond the normal operating level. A value of 3800 Gauss at the peak current limit of the selected device together with the built-in protection features of InnoSwitch4-Pro IC provide sufficient margin to prevent core saturation under start-up or output short circuit conditions.

Transformer Primary Inductance, (LP)
Once the lowest operating input voltage, switching frequency at full load, and required VOR are determined, the transformer primary inductance can be calculated. The PIXIs design spreadsheet can be used to assist in designing the transformer.

Quick Design Checklist

As with any power supply, the operation of all InnoSwitch4-Pro designs should be verified on the bench to make sure that component limits are not exceeded under worst-case conditions.

As a minimum, the following tests are strongly recommended:

1. Maximum Drain Voltage – Verify that V_{DS} of InnoSwitch4-Pro and SR FET do not exceed 90% of breakdown voltages at the highest input voltage and peak (overload) output power in normal operation and during start-up.
2. Maximum Drain Current – At maximum ambient temperature, maximum input voltage and peak output (overload) power. Review drain current waveforms for any signs of transformer saturation or excessive leading-edge current spikes at start-up. Repeat tests under steady-state conditions and verify that the leading edge current spike is below $I_{LIMIT(MIN)}$ at the end of $t_{LEB(MIN)}$. Under all conditions, the maximum drain current for the primary switch should be below the specified absolute maximum ratings.
3. Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that temperature specification limits for InnoSwitch4-Pro IC, transformer, output SR FET, and output capacitors are not exceeded. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of the InnoSwitch4-Pro IC. Under low-line, maximum power, a maximum InnoSwitch4-Pro
4. SOURCE pin temperature of 110 °C is recommended to allow for these variations.

Design Considerations When Using PowiGaN Devices

For a flyback converter configuration, typical voltage waveform at the DRAIN pin of the IC is shown in Figure 32.

V_{OR} is the reflected output voltage across the primary winding when the secondary is conducting. V_{BUS} is the DC voltage connected to one end of the transformer primary winding. The peak drain voltage of the primary switch is the total of V_{BUS} and V_{OR}. V_{OR} and the clamp voltage V_{CLM} should be selected such that the peak drain voltage is lower than 650 V for all normal operating conditions. This provides sufficient margin to ensure that occasional increase in voltage during line transients such as line surges will maintain the peak drain voltage well below 750 V under abnormal transient operating conditions. This ensures excellent long term reliability and design margin.

To make full use of ZVS capability and ensure flattest efficiency over line/load, set reflected output voltage (V_{OR}) to maintain K_P = 0.7 at minimum input voltage for universal input and $K_P \geq 1$ for high-line-only conditions.

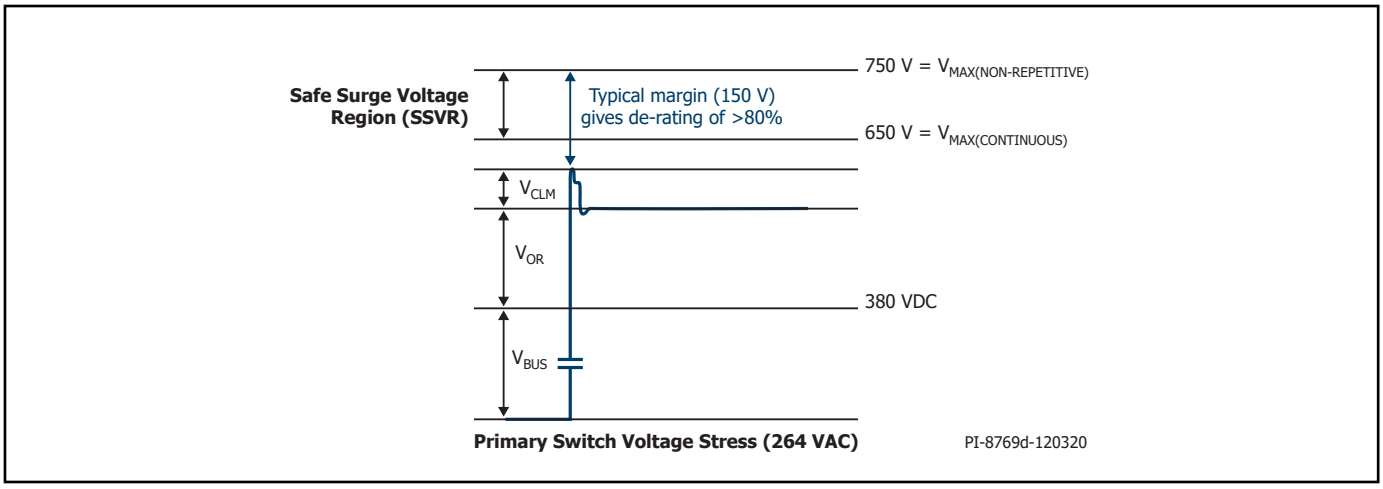


Figure 32. Peak Drain Voltage for 264 VAC Input Voltage.

Absolute Maximum Ratings[1,2]

DRAIN Pin Voltage[6] ..... -0.3 V to 750 V
DRAIN Pin Peak Current: PowiGaN device INN4374F.....6.5 A[7]
PowiGaN device INN4x74F.....10 A[7]
PowiGaN device INN4x75F.....14 A[7]
PowiGaN device INN4x76F.....19 A[7]
PowiGaN device INN4x77F.....26 A[7]
BPP/BPS Pin Voltage .....-0.3 to 6 V
BPP/BPS Pin Current ..... 100 mA
HSD Pin Voltage: PowiGan device INN437xF ..... -0.3 to 6 V
PowiGan device INN447xF ..... -0.3 to 6 V
SCL, SDA, uVCC Pin Voltage .....-0.3 to 6 V
uVCC Pin Current[5] .....12 mA
FWD Pin Voltage ..... -1.5 V to 150 V
SR Pin Voltage .....-0.3 V to 6 V
V Pin Voltage .....-0.3 V to 650 V
VOUT Pin Voltage .....-0.3 V to 27 V
VB/D Pin Current ..... 50 mA
VB/D Pin Voltage ..... -0.3 to 35 V
IS Pin Voltage .....-0.3 V to 0.3 V[8]
Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature[3].....-40 to 150 °C
Ambient Temperature .....-40 to 105 °C
Lead Temperature[4] .....260 °C

Notes:
1. All voltages referenced to SOURCE and Secondary GROUND, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Normally limited by internal circuitry.
4. 1/16" from case for 5 seconds.
5. Only at 5 V output, the uVCC pin can supply 40 mA maximum current for 0.5 seconds.
6. PowiGaN devices:
   Maximum drain voltage (non-repetitive pulse); for derating calculation ..... -0.3 V to 750 V
   Maximum continuous drain voltage.....-0.3 V to 650 V
7. Please refer to Figure 37 for maximum allowable voltage and current combinations.
8. Absolute maximum voltage for less than 500 µs is 3 V.

Thermal Resistance

Thermal Resistance: INN4x73F
(θ_{JA}).....71 °C/W[2], 66 °C/W[3]
(θ_{JC}).....25 °C/W[1]
INN4x75F
(θ_{JA}).....70 °C/W[2], 64 °C/W[3]
(θ_{JC}).....21 °C/W[1]
INN4x77F
(θ_{JA}).....55 °C/W[2], 51 °C/W[3]
(θ_{JC}).....16 °C/W[1]

Notes:
1. The case temperature is measured on the top of the package.
2. Soldered to 0.36 sq. inch (232 mm²), 2 oz. (610 g/m²) copper clad.
3. Soldered to 1.0 sq. inch (645 mm²), 2 oz. (610 g/m²) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Start-Up Switching Frequency	f_{SW}	T_J = 25 °C			25	27	kHz
Jitter Modulation Frequency	f_M	T_J = 25 °C f_{SW} = 100 kHz			1.25		kHz
Maximum On-Time	$t_{ON(MAX)}$	T_J = 25 °C		13	16.5		µs
Minimum Primary Feedback Block-Out Timer	t_{BLOCK}					$t_{OFF(MIN)}$	µs
BPP Supply Current	I_{S1}	V_{BPP} = V_{BPP} + 0.1 V (Switch not Switching) T_J = 25 °C			300	425	µA
	I_{S2}	V_{BPP} = V_{BPP} + 0.1 V (Switch Switching at 180 kHz) T_J = 25 °C	INN4373F		2.1	2.7	mA
			INN4374F		3.2	3.7	
			INN4375F		3.2	3.7	
			INN4376F		4.29	5.15	
			INN4377F		4.3	5.16	
			INN4474F		2.95	3.54	
			INN4475F		2.96	3.55	
			INN4476F		4.2	5.04	
			INN4477F		4.29	5.15	
			INN4574F		3.2	3.7	
			INN4575F		3.2	3.7	
			INN4576F		4.29	5.15	
			INN4577F		4.3	5.16	
			INN4674F		2.95	3.54	
			INN4675F		2.96	3.55	
			INN4676F		4.2	5.04	
			INN4677F		4.29	5.15	
BPP Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C			-1.35		mA
	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C			-4.65		
BPP Pin Voltage	V_{BPP}	T_J = 25 °C		4.8	5.00	5.16	V
BPP Pin Voltage Hysteresis	$V_{BPP(H)}$	T_J = 25 °C			0.5		V
BPP Shunt Voltage	V_{SHUNT}	I_{BPP} = 2 mA T_J = 25 °C		5.16	5.36	5.7	V
UV/OV Pin Brown-In Threshold	I_{UV+}	T_J = 25 °C		23.1	25.2	27.5	µA
UV/OV Pin Brown-Out Threshold	I_{UV-}	T_J = 25 °C		20.5	23.0	25	µA
Brown-Out Delay Time	t_{UV-}				35		ms

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
UV/OV Pin Line Overvoltage Threshold	I_{OV+}	T_J = 25 °C		106	115	118	µA
UV/OV Pin Line Overvoltage Hysteresis	$I_{OV(H)}$	T_J = 25 °C			8		µA
UV/OV Pin Line Overvoltage Recovery Threshold	I_{OV-}	T_J = 25 °C		100	107		µA
Line Fault Protection							
VOLTAGE Pin Line Overvoltage Deglitch Filter	t_{OV+}	T_J = 25 °C See Note B			3		µs
Circuit Protection							
Standard Current Limit (BPP) Capacitor = 0.47 µF See Note D	I_{LIMIT} (switching at 100 kHz)	di/dt = 400 mA/µs T_J = 25 °C	INN4373F	1581	1700	1819	mA
		di/dt = 475 mA/µs T_J = 25 °C	INN4374F	1953	2100	2247	
		di/dt = 500 mA/µs T_J = 25 °C	INN4375F	2139	2300	2461	
		di/dt = 660 mA/µs T_J = 25 °C	INN4376F	2697	2900	3103	
		di/dt = 770 mA/µs T_J = 25 °C	INN4377F	3162	3400	3638	
		di/dt = 1200 mA/µs T_J = 25 °C	INN4474F	3348	3600	3852	
		di/dt = 1300 mA/µs T_J = 25 °C	INN4475F	3534	3800	4066	
		di/dt = 1600 mA/µs T_J = 25 °C	INN4476F	3906	4200	4494	
		di/dt = 1700 mA/µs T_J = 25 °C	INN4477F	4278	4600	4922	
		di/dt = 475 mA/µs T_J = 25 °C	INN4574F	1953	2100	2247	
		di/dt = 500 mA/µs T_J = 25 °C	INN4575F	2139	2300	2461	
		di/dt = 660 mA/µs T_J = 25 °C	INN4576F	2697	2900	3103	
		di/dt = 770 mA/µs T_J = 25 °C	INN4577F	3162	3400	3638	
		di/dt = 1200 mA/µs T_J = 25 °C	INN4674F	3348	3600	3852	
		di/dt = 1300 mA/µs T_J = 25 °C	INN4675F	3534	3800	4066	
		di/dt = 1600 mA/µs T_J = 25 °C	INN4676F	3906	4200	4494	
		di/dt = 1700 mA/µs T_J = 25 °C	INN4677F	4278	4600	4922	

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection (cont.)							
Increased Current Limit (BPP) Capacitor = 4.7 µF See Note D	$I_{LIMIT+1}$ (switching at 100 kHz)	di/dt = 400 mA/µs T_J = 25 °C	INN4373F	1748	1900	2052	mA
		di/dt = 475 mA/µs T_J = 25 °C	INN4374F	2162	2350	2538	
		di/dt = 500 mA/µs T_J = 25 °C	INN4375F	2374	2580	2786	
		di/dt = 660 mA/µs T_J = 25 °C	INN4376F	2990	3250	3510	
		di/dt = 770 mA/µs T_J = 25 °C	INN4377F	3505	3810	4115	
		di/dt = 1200 mA/µs T_J = 25 °C	INN4474F	3708	4030	4352	
		di/dt = 1300 mA/µs T_J = 25 °C	INN4475F	3919	4260	4601	
		di/dt = 1600 mA/µs T_J = 25 °C	INN4476F	4324	4700	5076	
		di/dt = 1700 mA/µs T_J = 25 °C	INN4477F	4738	5150	5562	
		di/dt = 475 mA/µs T_J = 25 °C	INN4574F	2162	2350	2538	
		di/dt = 500 mA/µs T_J = 25 °C	INN4575F	2374	2580	2786	
		di/dt = 660 mA/µs T_J = 25 °C	INN4576F	2990	3250	3510	
		di/dt = 770 mA/µs T_J = 25 °C	INN4577F	3505	3810	4115	
		di/dt = 1200 mA/µs T_J = 25 °C	INN4674F	3708	4030	4352	
		di/dt = 1300 mA/µs T_J = 25 °C	INN4675F	3919	4260	4601	
		di/dt = 1600 mA/µs T_J = 25 °C	INN4676F	4324	4700	5076	
		di/dt = 1700 mA/µs T_J = 25 °C	INN4677F	4738	5150	5562	
Overload Detection Frequency	f_{OVL}	T_J = 25 °C		130	140	151	kHz
BYPASS Pin Fault Shutdown Threshold Current	I_{SD}	T_J = 25 °C		6.0	7.5		mA
Auto-Restart On-Time	t_{AR}	T_J = 25 °C			82		ms
Auto-Restart Trigger Skip Time	$t_{AR(SK)}$	T_J = 25 °C See Note A			1.3		sec
Auto-Restart Off-Time	$t_{AR(OFF)}$	T_J = 25 °C			2.00		sec
Short Auto-Restart Off-Time	$t_{AR(OFF)SH}$	T_J = 25 °C			0.20		sec
HSD On-Time	t_{HSD}	T_J = 25 °C	INN437xF	440	500	560	ns
			INN447xF				

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Output							
ON-State Resistance	$R_{DS(ON)}$	INN4373F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.52	0.68	Ω
			T_J = 100 °C		0.78	1.02	
		INN4374F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.35	0.44	
			T_J = 100 °C		0.49	0.62	
		INN4375F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.29	0.39	
			T_J = 100 °C		0.41	0.54	
		INN4376F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.18	0.28	
			T_J = 100 °C		0.27	0.37	
		INN4377F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.145	0.21	
			T_J = 100 °C		0.23	0.29	
		INN4474F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.35	0.44	
			T_J = 100 °C		0.49	0.62	
		INN4475F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.29	0.39	
			T_J = 100 °C		0.41	0.54	
		INN4476F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.18	0.28	
			T_J = 100 °C		0.27	0.37	
		INN4477F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.145	0.21	
			T_J = 100 °C		0.23	0.29	
		INN4574F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.35	0.44	
			T_J = 100 °C		0.49	0.62	
		INN4575F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.29	0.39	
			T_J = 100 °C		0.41	0.54	
		INN4576F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.18	0.28	
			T_J = 100 °C		0.27	0.37	
		INN4577F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.145	0.21	
			T_J = 100 °C		0.23	0.29	
		INN4674F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.35	0.44	
			T_J = 100 °C		0.49	0.62	
		INN4675F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.29	0.39	
			T_J = 100 °C		0.41	0.54	
		INN4676F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.18	0.28	
			T_J = 100 °C		0.27	0.37	
		INN4677F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.145	0.21	
			T_J = 100 °C		0.23	0.29	
OFF-State Drain Leakage Current	I_{DSS1}	$V_{BPP} = V_{BPP}$ + 0.1 V, V_{DS} = 80% Peak Drain Voltage T_J = 125 °C				200	µA
	I_{DSS2}	$V_{BPP} = V_{BPP}$ + 0.1 V, V_{DS} = 325 V T_J = 25 °C			15		
Drain Supply Voltage		See Note B		50			V
Thermal Shutdown	T_{SD}	See Note A		135	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$	See Note A			70		°C

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Secondary						
Maximum Secondary Frequency	f_{SREQ}	T_J = 25 °C	164	180		kHz
Minimum Off-time	$t_{OFF(MIN)}$			1.9	2.05	µs
BPS Pin Latch Command Shutdown Threshold Current	$I_{BPS(SD)}$		6	8.9		mA
Start-Up VOUT Pin Regulation Voltage	$VOUT_{REG}$	T_J = 25 °C	4.85	5	5.15	V
Output Voltage Programming Range	$V_{OUT(R)}$	Default = 5 V	3.00		24.00	V
	TOL_{VOUT}	Tolerance T_J = 25 °C	-3		+3	%
Output Voltage Step Size	ΔV_{OUT}	T_J = 25 °C		10		mV
Report-Back Output Voltage Tolerance	$V_{OUT(T)}$	T_J = 25 °C	-3		+3	%
Normalized Output Current	I_{OUT}	0.6 - 1.0 T_J = 25 °C, See Note C	-5		+5	%
		0.2 T_J = 25 °C, See Note C	-15		+15	
Normalized Output Current Step Size	ΔI_{OUT}	T_J = 25 °C		0.52		%
Maximum V/I Update Rate	t_{VI}	See Note B		10		ms
Minimum Time Delay Between I²C Commands	t_{DELAY}	See Note B	150			µs
Internal Current Limit Voltage Threshold	$I_{SV(TH)}$	T_J = 25 °C Across External IS to GND Pin Resistor See Note F		32		mV
Cable Drop Compensation (CDC) Programming Range	ϕ_{CD}	T_J = 25 °C Default = 0 V	0		600	mV
CDC Tolerance	$TOL\phi_{CD}$	CDC ≥ 100 mV T_J = 25 °C	-35		+35	mV
CDC Programming Step Size	$\Delta\phi_{CD}$	T_J = 25 °C		50		mV
Output Overvoltage Programming Range	V_{OVA}	Default = 6.2 V	3.3		25	V
Output Overvoltage Tolerance	TOL_{OVA}	T_J = 25 °C	-3		+3	%
Output Overvoltage Programming Step Size	ΔV_{OVA}			100		mV
Output Undervoltage Programming Range	V_{UVA}	Default = 3.6 V	2.7		24	V
Output Undervoltage Tolerance	TOL_{UVA}	T_J = 25 °C	-3		+3	%

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Secondary (cont.)							
Output Undervoltage Programming Step Size	ΔV_{UVA}				100		mV
Output Undervoltage Timer Programming Options	t_{UVL}	T_J = 25 °C See Notes B, E	Programming Option 1		8		ms
			Programming Option 2		16		
			Programming Option 3		32		
			Default Programming Option 4		64		
Constant Output Power Onset Threshold Programming Range	V_{KP}	Default = 24 V		5.3		24	V
Constant Output Power Tolerance	$TOLP_{OUT}$	At 85% of Full Scale Current		-10		+10	%
Constant Output Power Onset Threshold Programming Step Size	ΔV_{KP}				100		mV
Constant Voltage Mode Timer Programming Options	t_{CVO}	T_J = 25 °C See Notes B, E	Programming Option 1		8		ms
			Programming Option 2		16		
			Programming Option 3		32		
			Programming Option 4		64		
Watchdog Timer	t_{WDT}	Default Programming Option 1 See Note B			0.5		sec
		Programming Option 2, See Note B			1		
		Programming Option 3, See Note B			2		
VB/D Drive Voltage	$V_{VB/D}$	With Respect to VOUT Pin		4	7		V
VB/D Pin Internal Current Discharge	$I_{B/D(DS)}$			50			mA
Secondary Over-Temperature Hysteresis	$T_{SEC(HYS)}$	Programming Option 1 See Note B			40		°C
		Programming Option 2 See Note B			60		
VOUT Pin Bleeder Current	IVO_{BLD}	VOUT = 5 V			270		mA
uVCC Supply Voltage	uVCC	V_{OUT} = 5 V, 10 mA < I_{UVCC} ≤ 40 mA T_J = 25 °C, See Note 5 in Absolute Maximum Ratings Table		3.3	3.6	3.78	V
		V_{OUT} ≥ 3.9 V I_{uVCC} ≤ 10 mA T_J = 25 °C		3.42	3.6	3.78	

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Secondary (cont.)							
uVCC Pin Output Resistance	R_{uVCC}	T_J = 25 °C				20	Ω
uVCC Reset Voltage Threshold	$uVCC_{RST}$	See Note A			2.5	2.65	V
BPS Pin Voltage	V_{BPS}			4.3	4.5		V
BPS Pin Current	I_{SNL}	T_J = 25 °C VBUS Switch Open			0.7	0.9	mA
		T_J = 25 °C VBUS Switch Closed			1	1.45	
BPS Pin Undervoltage Threshold	$V_{BPS(UVLO)TH}$				3.8	4.0	V
BPS Pin Undervoltage Hysteresis	$V_{BPS(UVLO)H}$				0.7		V
FORWARD Pin Breakdown Voltage	BV_{FWD}			150			V
Synchronous Rectifier @ T_J = 25 °C							
SR Pin Drive Voltage	V_{SR}			4.3	4.5		V
SR Pin Voltage Threshold	$V_{SR(TH)}$				-6	-2	mV
Rise Time	$t_{R(SR)}$	T_J = 25 °C C_{LOAD} = 2nF See Note B	10-90%		50		ns
Fall Time	$t_{F(SR)}$	T_J = 25 °C C_{LOAD} = 2nF See Note B	90-10%		30		ns
Output Pull-Up Resistance	R_{PU}	T_J = 25 °C V_{BPS} + 0.1 V I_{SR} = 30 mA				11.5	Ω
Output Pull-Down Resistance	R_{PD}	T_J = 25 °C V_{BPS} + 0.2 V I_{SR} = 30 mA				5	Ω

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
I²C Bus Specifications (SDA and SCL Pins) *See Note B						
SCL Clock Frequency	f_{SCL}	See Note G	50	400	535	kHz
Low-level Input Voltage	V_{IL}		-0.5		0.3 × uVCC	V
High-level Input Voltage	V_{IH}		0.7 × uVCC		uVCC + 0.5 V	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}		0.05 × uVCC			V
Low-Level Output Voltage (Open Drain or Collector)	V_{OL}	uVCC >2.8 V 3 mA Sink Current	0		0.4	V
Low-level Output Current	I_{OL}		3			mA
Output Fall-Time from $V_{IH(MIN)}$ to $V_{IL(MAX)}$	t_{OF}	Bus Capacitance from 10 pF to 400 pF	-		250	ns
SDA/SCL Input Current	I_I	(0.1 × uVCC) < (V_{SCL}/V_{SDA}) < (0.9 × uVCC)	-1		1	µA
SDA/SCL Capacitance	C_I		-		10	pF
Pulse Width of Spike Suppressed by Input Filter	t_{SP}		50			ns
High Period for SCL Clock	t_{HIGH}	f_{SCL} = 400 kHz	0.6			µs
Low Period for SCL Clock	t_{LOW}	f_{SCL} = 400 kHz	1.3			µs
Serial Data Set-up Time	$t_{SU:DAT}$		100			ns
Serial Data Hold time	$t_{HD:DAT}$		0			sec
Valid Data Time	$t_{VD:DAT}$	SCL Low to SDA Output Valid			0.9	µs
Valid Data Time for ACK	$t_{VD:ACK}$	ACK from SCL Low to SDA Low			0.9	µs
I²C Bus Free Time Between Start and Stop	t_{BUF}		1.3			µs
I²C Fall Time (Both SCL and SDA)	t_{fCL}				300	ns
I²C Rise Time (Both SCL and SDA)	t_{rCL}				300	ns
I²C Start or Repeated Start Condition Set-up Time	$t_{SU:STA}$		0.6			µs
I²C Start or Repeated Start Condition Hold Time	$t_{HD:STA}$		0.6			µs

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
I²C Bus Specifications (SDA and SCL Pins) *See Note B						
I²C Stop Condition Set-up Time	$t_{SU:STO}$		0.6			µs
Capacitive Load	C_B				400	pF
Noise Margin at the Low Level	V_{NL}		0.1 × uVCC			V
Noise Margin at the High Level	V_{NH}		0.1 × uVCC			V
SCL Pin Interrupt Timer	$t_{INT(SCL)}$	T_J = 25 °C		50		µs

NOTES:
A. This parameter is derived from characterization.
B. This parameter is guaranteed by design.
C. Use 1% tolerance resistor.
D. To ensure correct current limit it is recommended that nominal 0.47 µF / 4.7 µF capacitors are used. In addition, the BPP capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application. The minimum and maximum capacitor values are guaranteed by characterization.

Nominal BPP Pin Capacitor Value	BPP Capacitor Value Tolerance	
	Minimum	Maximum
0.47 µF	-60%	+100%
4.7 µF	-50%	N/A

Recommended to use at least 10 V / 0805 / X7R SMD MLCC.

E. Settling delay in averaging register will increase total observed time under light and no-load conditions.
F. This parameter should be used only for calculation of typical value of current sense resistor. The value programmed in CC register (0x98) regulates the output current. The tolerance is specified in the Normalized Output Current parameter (I_{OUT}).
G. Guarantee minimum low period for SCL clock of 930 ns while operating at any SCL clock frequency. This may require using asymmetrical SCL clock (reduced duty cycle) at higher frequencies.

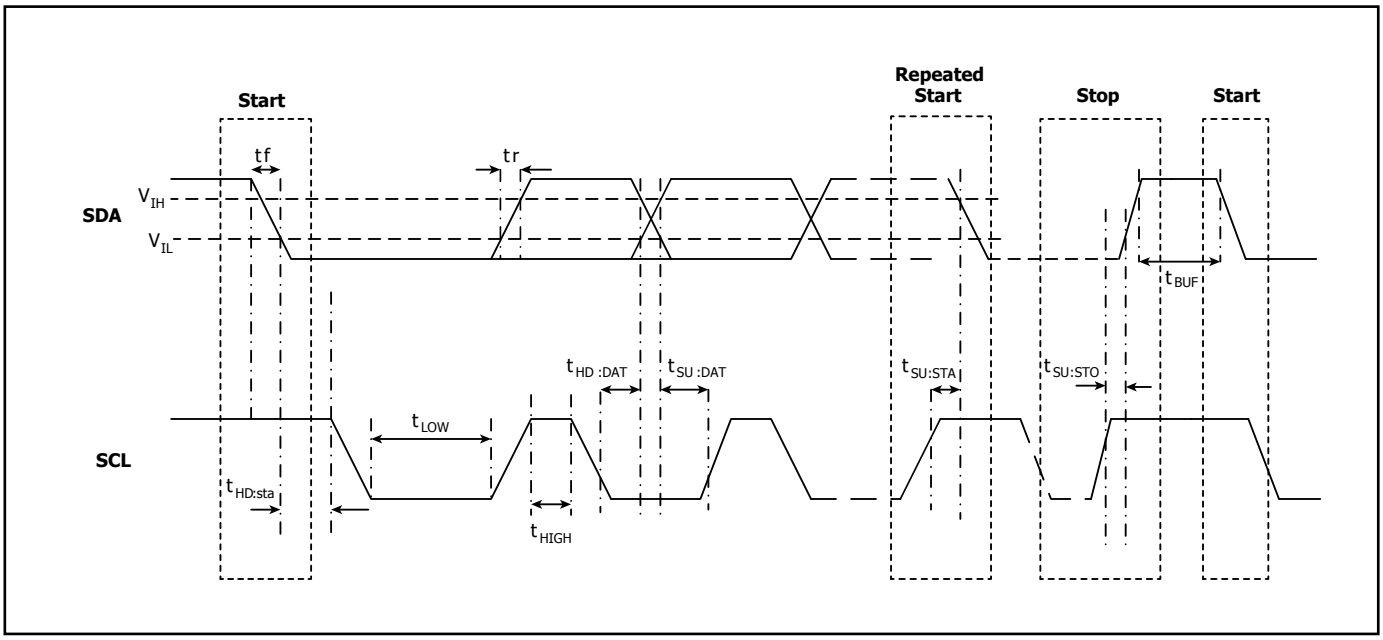
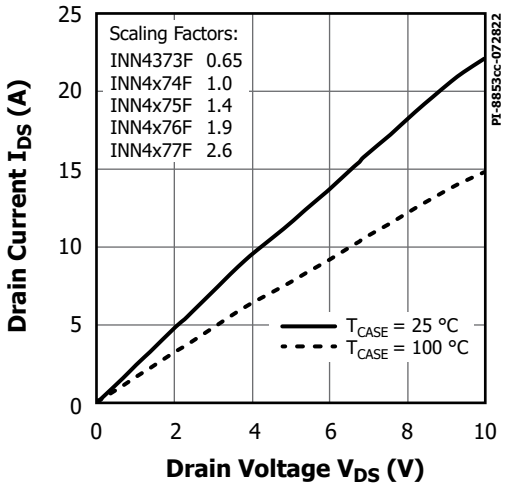
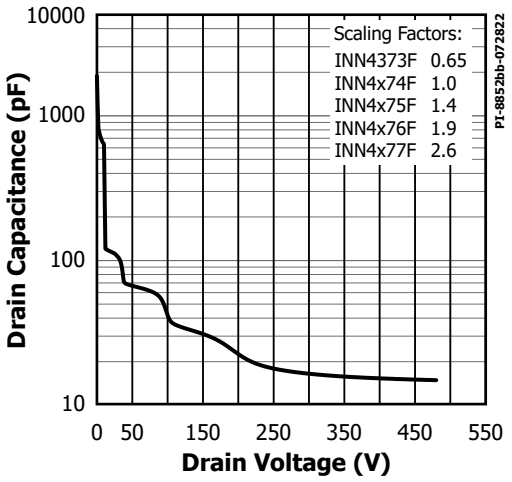


Figure 33. I²C Timing Diagram.

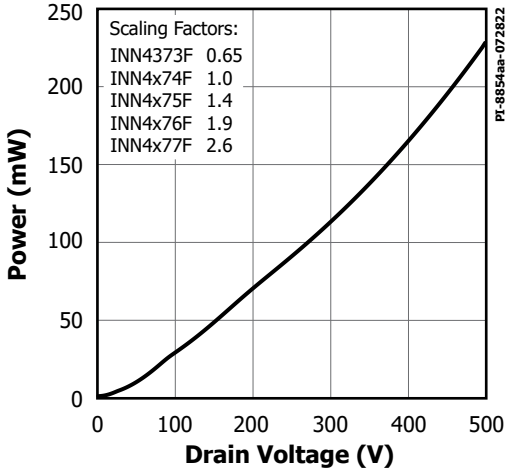
Typical Performance Curves



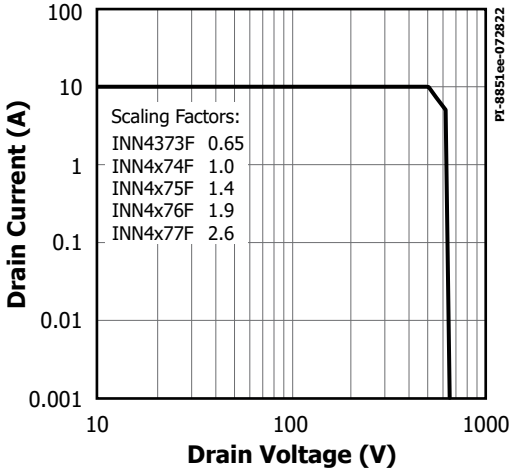
34. Output Characteristics.



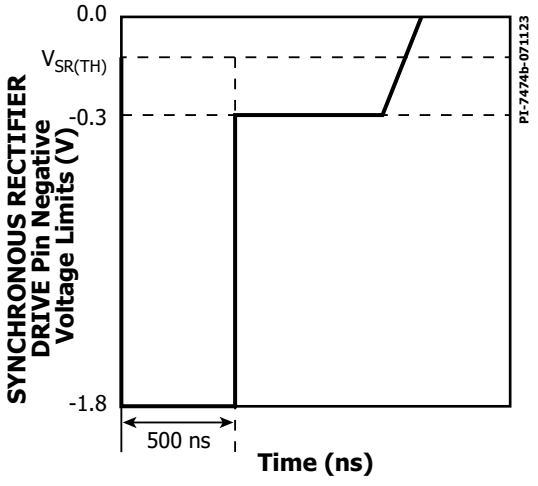
35. C_{OSS} vs. Drain Voltage.



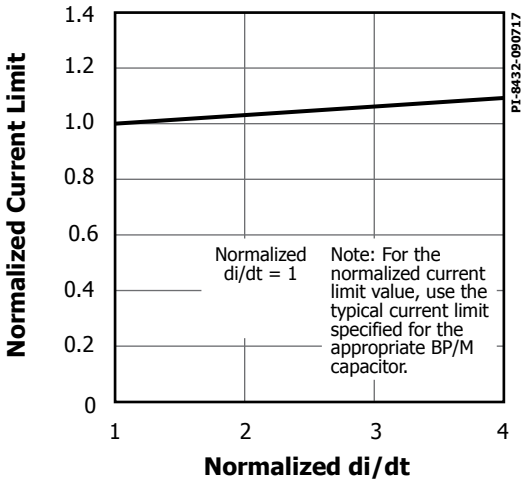
36. Drain Capacitance Power.



37. Maximum Allowable Drain Current vs. Drain Voltage.

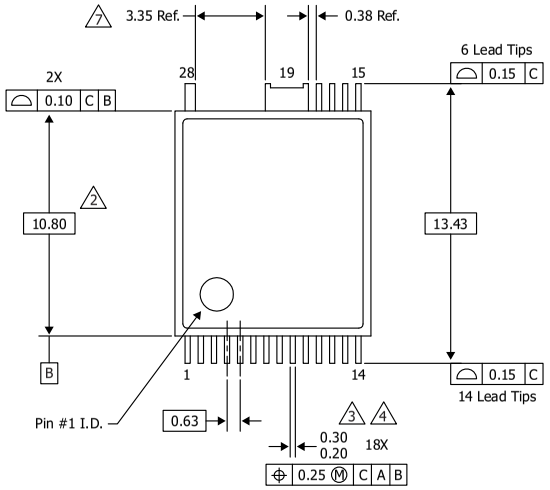


38. SYNCHRONOUS RECTIFIER DRIVE Pin Negative Voltage Limits.

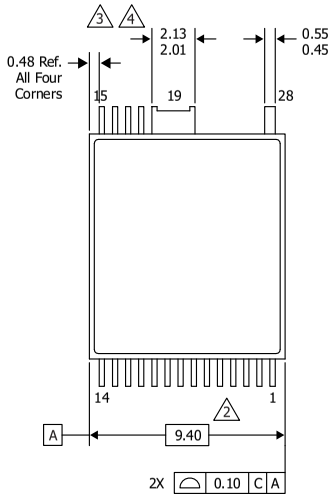


39. Standard Current Limit vs. di/dt.

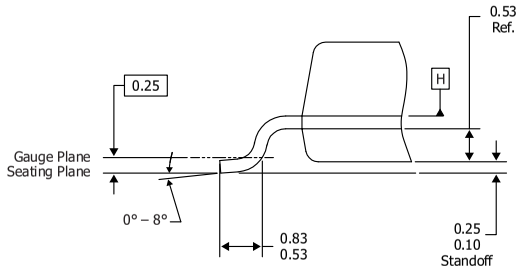
InSOP-T28D



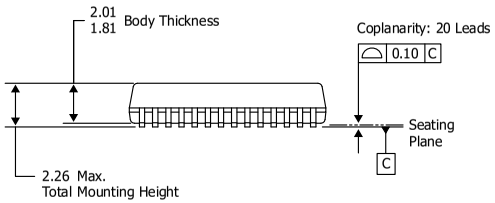
TOP VIEW



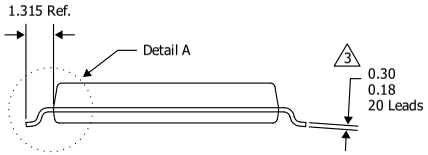
BOTTOM VIEW



DETAIL A



SIDE VIEW



END VIEW

NOTES:

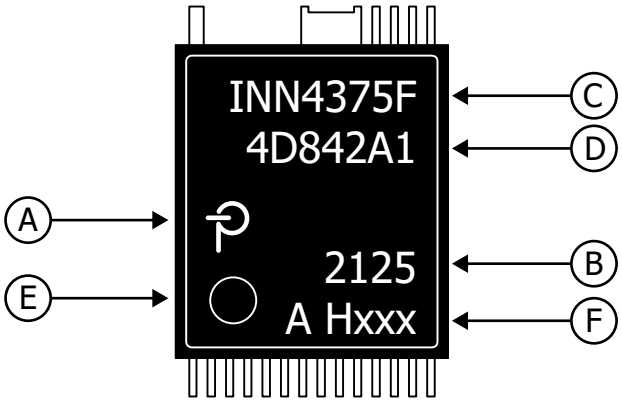
1. Dimensioning and Tolerancing per ASME Y14.5M – 1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in millimeters.
6. Datums A & B to be determined at Datum H.
7. This dimension is the nominal dimension between leadtips, not including plating, and not including metal protrusions. Metal-to-Metal distance (Creepage) is 3.20 mm minimum.

PI-9406-041923
POD-inSOP-T28D Rev B

POD-inSOP-T28D_B_032623

PACKAGE MARKING

InSOP-T28D



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year (YY) followed by 2-digit work week (WW)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code
E. Pin 1 Indicator
F. Test Lot Information and Feature Code

PI-9405-092322

Safety Certification Specifications (Safety approval pending)

Parameter	Conditions	Rating	Units
Ratings for UL1577			
Primary-Side Current Rating	Current from pin (19-22) to pin 28	0.6	A
Primary-Side Power Rating	T_{AMB} = 25 °C (Device mounted in socket resulting in T_{CASE} = 120 °C)	1.35	W
Secondary-Side Power Rating	T_{AMB} = 25 °C (Device mounted in socket)	0.125	W
Package Characteristics			
Clearance		11.4	mm (min)
Creepage		11.4	mm (min)
Distance Through Insulation (DTI)		0.4	mm (min)
Transient Isolation Voltage		6	kV (min)
Comparative Tracking Index (CTI)		>600	V

Feature Code Table

Summary Features	H341	H342
I_{LIM} Selectable	Yes	Yes
Over-Temperature Protection	Hysteretic	Hysteretic
Line OV/UV	Enabled	Enabled
Line UV Timer (35 ms or 400 ms)	35 ms	35 ms
Mode of Operation	ACF Mode Switching	Quasi Resonant Mode Switching

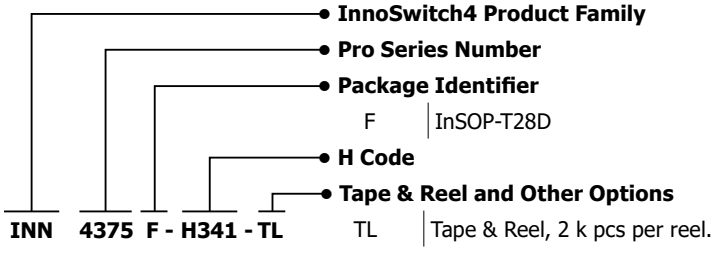
MSL Table

Part Number	MSL Rating
INN4x7xF	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	**JESD78D**	> ±100 mA or > 1.5 × V_{MAX} on all pins
Charge Device Model ESD	**ANSI/ESDA/JEDEC JS-002-2014**	> ±1 kV on all pins
Human Body Model ESD	**ANSI/ESDA/JEDEC JS-002-2014**	> ±2 kV on all pins

Part Ordering Information



Revision	Notes	Date
C	Production release.	09/22
D	Updates to command register table type values and active VOUT pin bleeder section.	11/22
E	Updated UVA bit column description on page 12.	03/23
F	Updated Figures 11, 38 and Package Drawing. Text addition to FORWARD Pin Resistor section on page 30 and added Note 9 to Absolute Maximum Ratings table. Updated Note 6 in ABS Max rating table. Updated page 1 UL1577 bullet.	07/23

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