

Product Summary

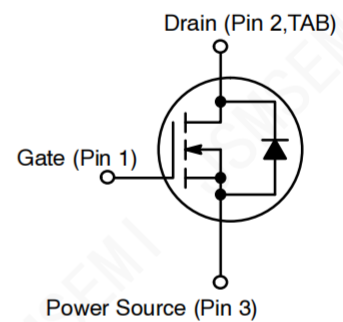
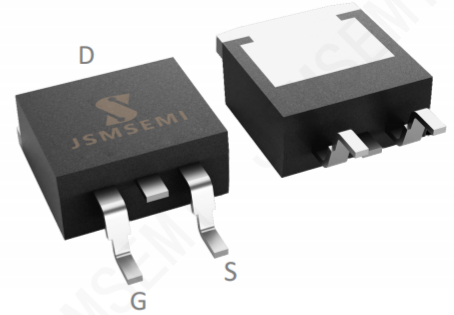
- V_{DS} 100V
- I_D 120A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <5.3m Ω
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor
- Motor drivers



ABSOLUTE MAXIMUM RATINGS ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_C=25^\circ\text{C}$) ⁽¹⁾	I_D	120	A
Continuous Drain Current ($T_C=100^\circ\text{C}$)	I_D	95	A
Pulsed Drain Current ⁽¹⁾	I_{DM}	480	A
Drain Power Dissipation	P_D	180	W
Single Pulsed Avalanche Energy ⁽²⁾	E_{AS}	340	mJ
Thermal Resistance from Junction to Ambient ⁽³⁾	$R_{\theta JA}$	43	$^\circ\text{C/W}$
Thermal Resistance from Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
Junction Temperature	T_J	-55~ +150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55~ +150	$^\circ\text{C}$

Notes:

- 1) Repetitive Rating: pulse width limited by maximum junction temperature
- 2) EAS condition : $T_J=25^\circ\text{C}$, $V_{DD}=50\text{V}$, $V_G=10\text{V}$, $L=1.0\text{mH}$, $R_g=25\Omega$, $I_{AS}=44.7\text{A}$
- 3) The value of $R_{\theta JA}$ Mounted on FR4 Board (25.4mm*25.4mm*t1.6mm) With 2oz Copper $T_A=25^\circ\text{C}$

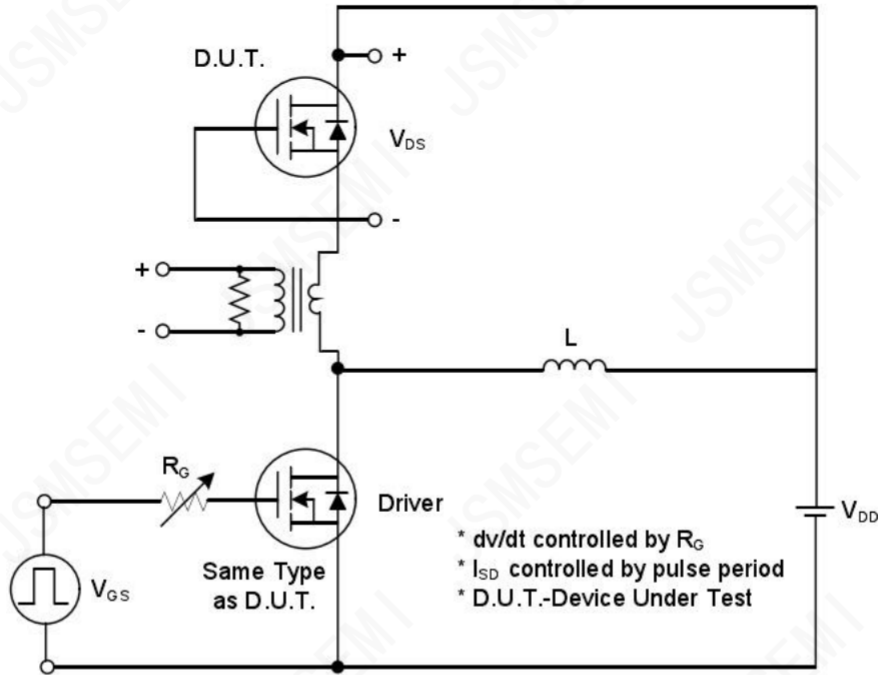
MOSFET ELECTRICAL CHARACTERISTICS(T_J=25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100	-	-	V
Zero gate voltage drain current	I _{DSS}	V _{DS} = 100V, V _{GS} = 0V	-	-	1	μA
Gate-body leakage current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V	-	-	±100	nA
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	2.0	3.0	4.0	V
Drain-source on-resistance	R _{DS(on)}	V _{GS} = 10V, I _D = 20A	-	4.5	5.3	mΩ
Forward transconductance	R _g	V _{GS} = 0V, V _{DS} = 0V, f = 1.0MHz	-	2.0	-	Ω
Dynamic characteristics						
Input Capacitance	C _{iss}	V _{DS} = 50V, V _{GS} = 0V, f = 1MHz	-	4628	-	pF
Output Capacitance	C _{oss}		-	1624	-	
Reverse Transfer Capacitance	C _{rss}		-	19	-	
Switching characteristics						
Turn-on delay time	t _{d(on)}	V _{DD} = 50V, I _D = 20A, R _G = 3Ω, V _{GS} = 10V	-	12	-	nS
Turn-on rise time	t _r		-	26	-	
Turn-off delay time	t _{d(off)}		-	38	-	
Turn-off fall time	t _f		-	31	-	
Total Gate Charge	Q _g	V _{DS} = 50V, I _D = 20A, V _{GS} = 10V	-	61	-	nC
Gate-Source Charge	Q _{gs}		-	19.5	-	
Gate-Drain Charge	Q _{gd}		-	8.7	-	
Source-Drain Diode characteristics						
Diode Forward voltage	V _{SD}	T _J = 25°C, V _{GS} = 0V, I _S = 20A	-	0.8	1.2	V
Diode Forward current	I _S	T _C = 25°C	-	-	120	A
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 20A, di/dt = 100A/us	-	77	-	nS
Body Diode Reverse Recovery Charge	Q _{rr}		-	189	-	nC

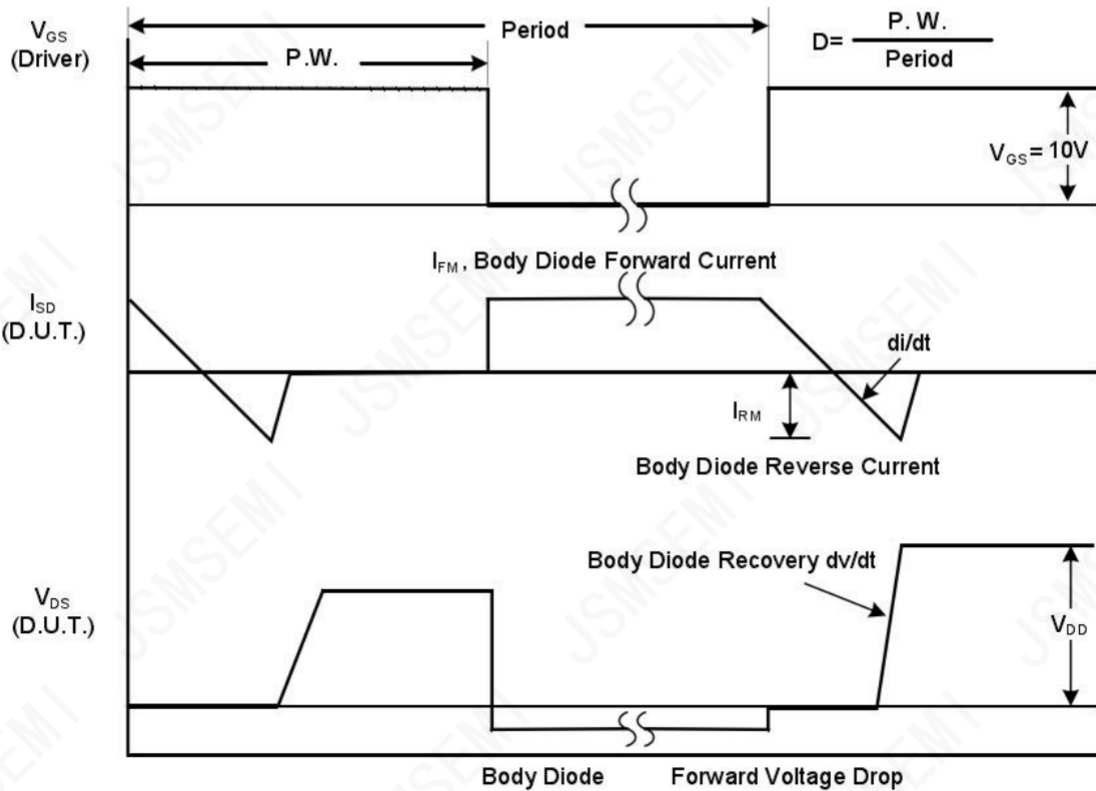
Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship, Quantity	Green
IPB120N10S405ATMA1-JSM	TO-263	4N1005	-55 to 150°C	1	T&R, 800	Rohs

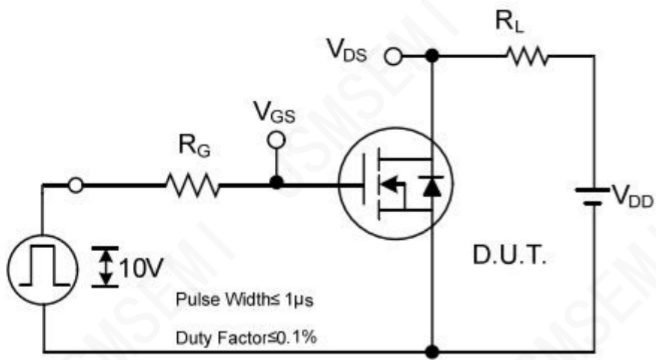
■ RATING AND CHARACTERISTIC CURVES



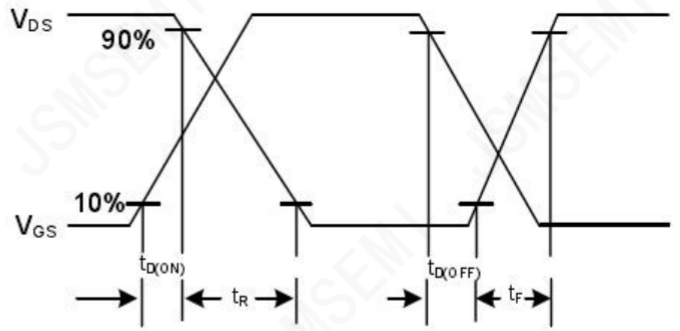
Peak Diode Recovery dv/dt Test Circuit



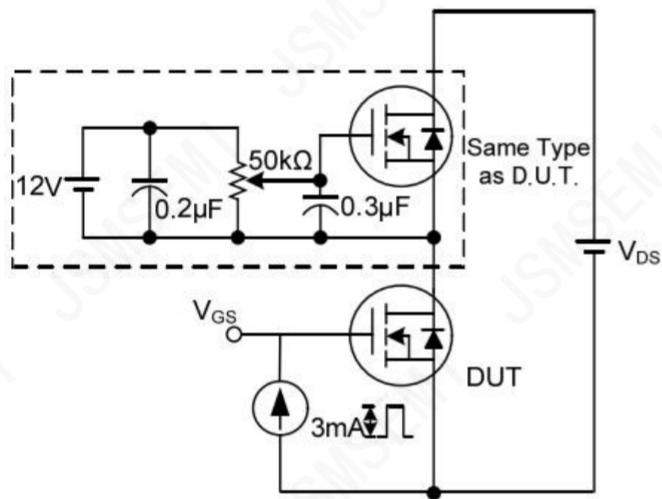
Peak Diode Recovery dv/dt Waveforms



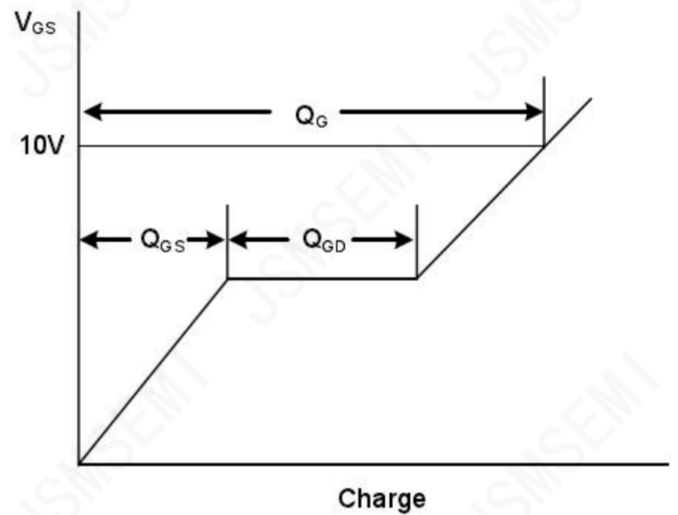
Switching Test Circuit



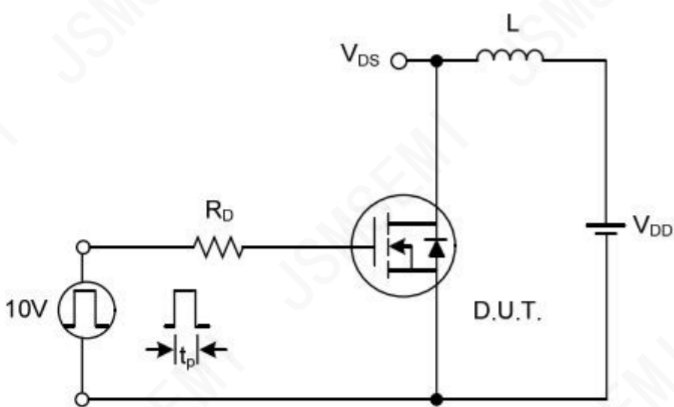
Switching Waveforms



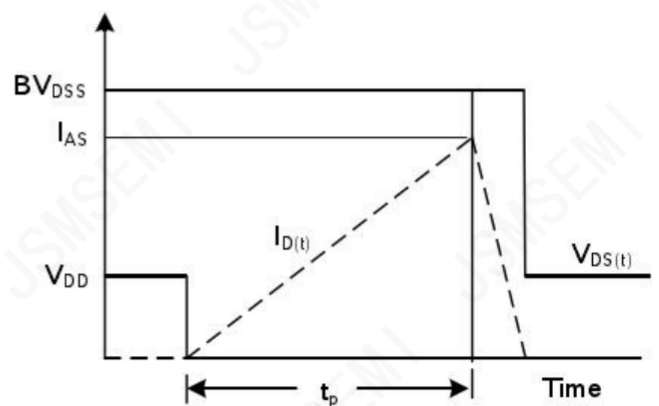
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

Typical Characteristics

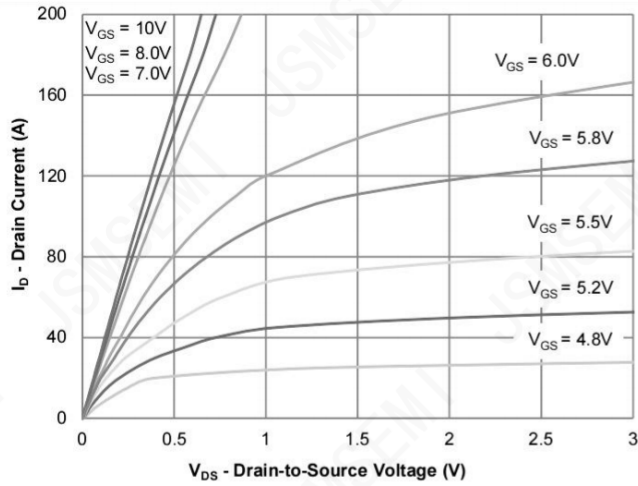


Figure 1: Output Characteristics

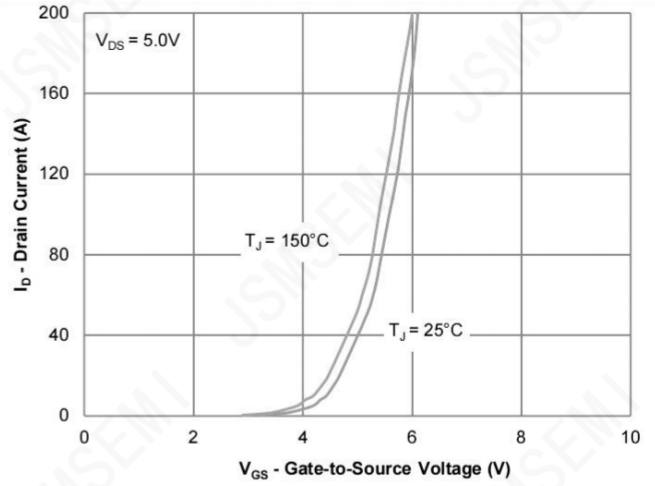


Figure 2: Transfer Characteristics

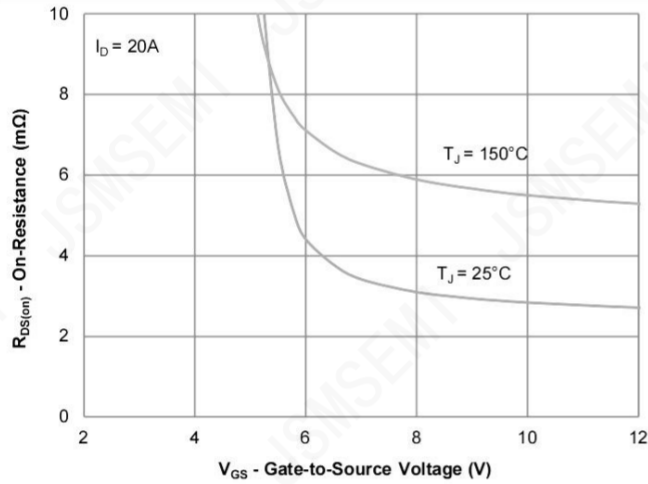


Figure 3: On-Resistance vs. Gate-Source Voltage

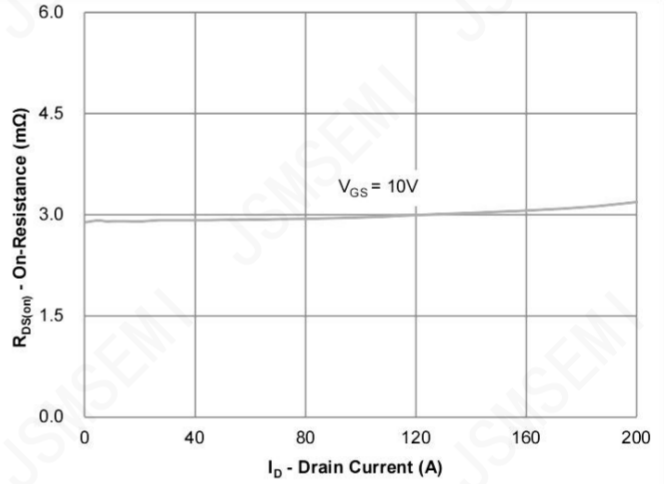


Figure 4: On-Resistance vs. Drain Current

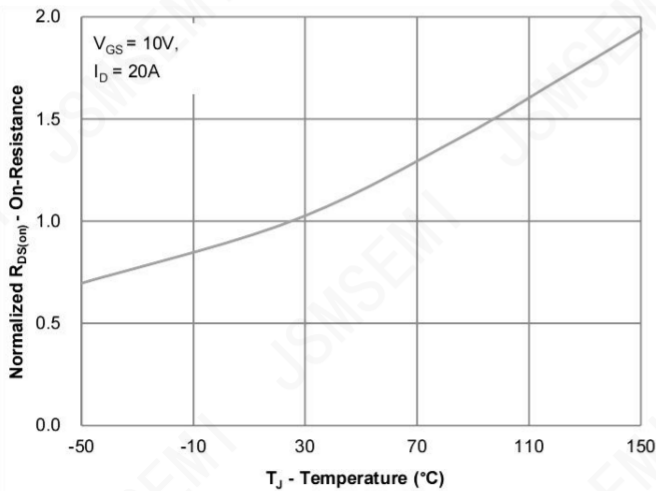


Figure 5: On-Resistance vs. Junction Temperature

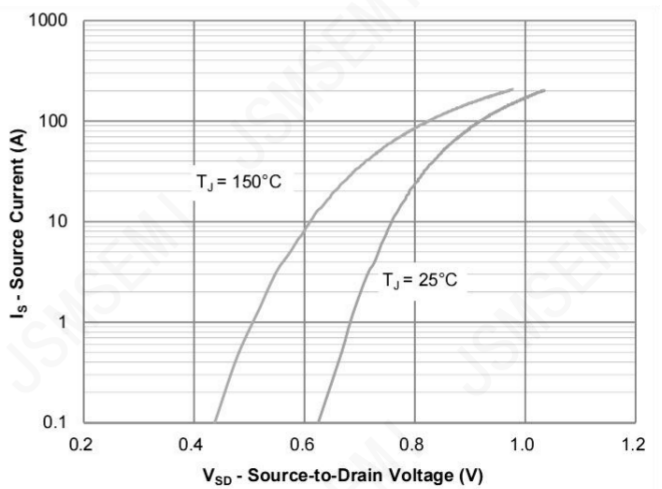


Figure 6: Source-Drain Diode Forward Voltage

Typical Characteristics

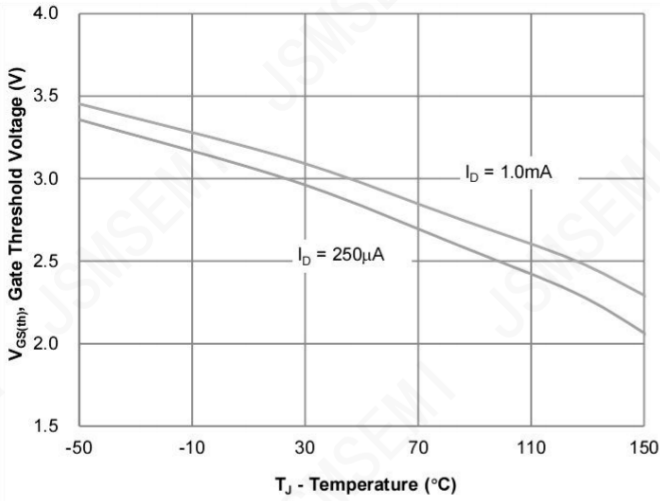


Figure 7: Gate Threshold Variation vs. Junction Temperature

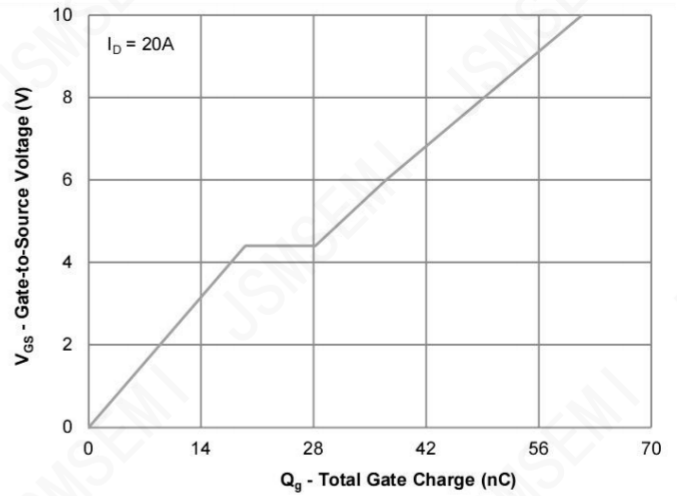


Figure 8: Gate Charge Characteristics

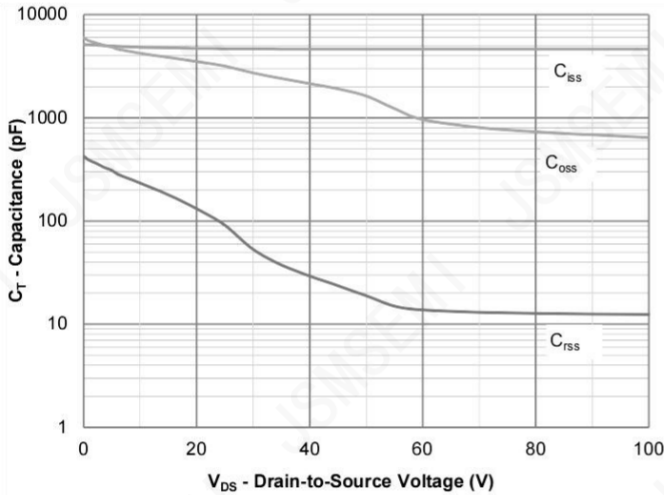


Figure 9: Capacitance Characteristics

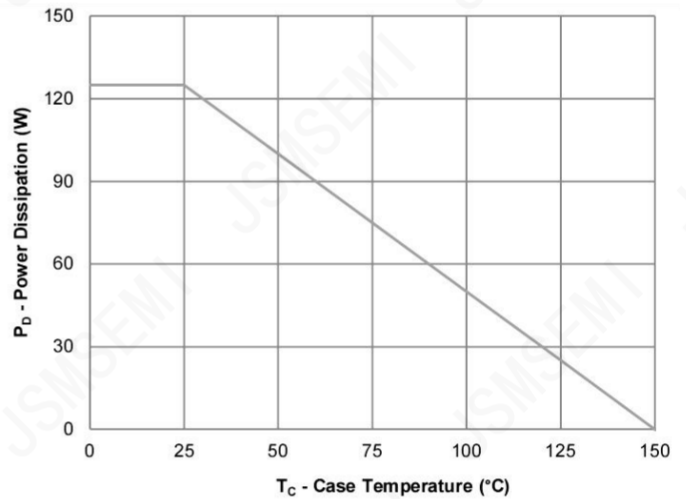


Figure 10: Power Derating

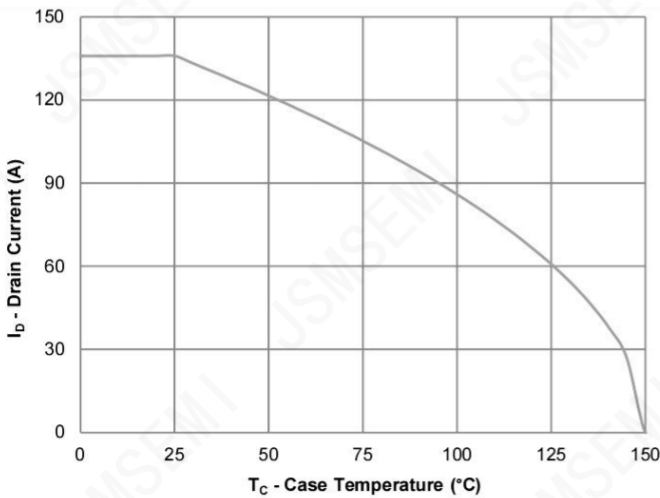


Figure 11: Current Derating

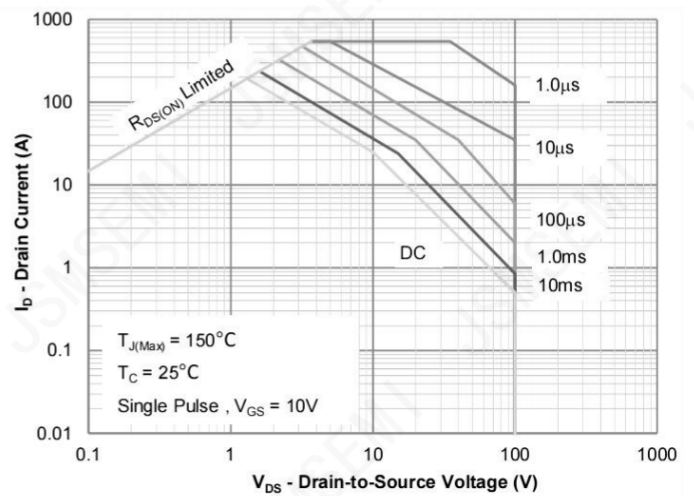


Figure 12: Safe Operating Area

Typical Characteristics

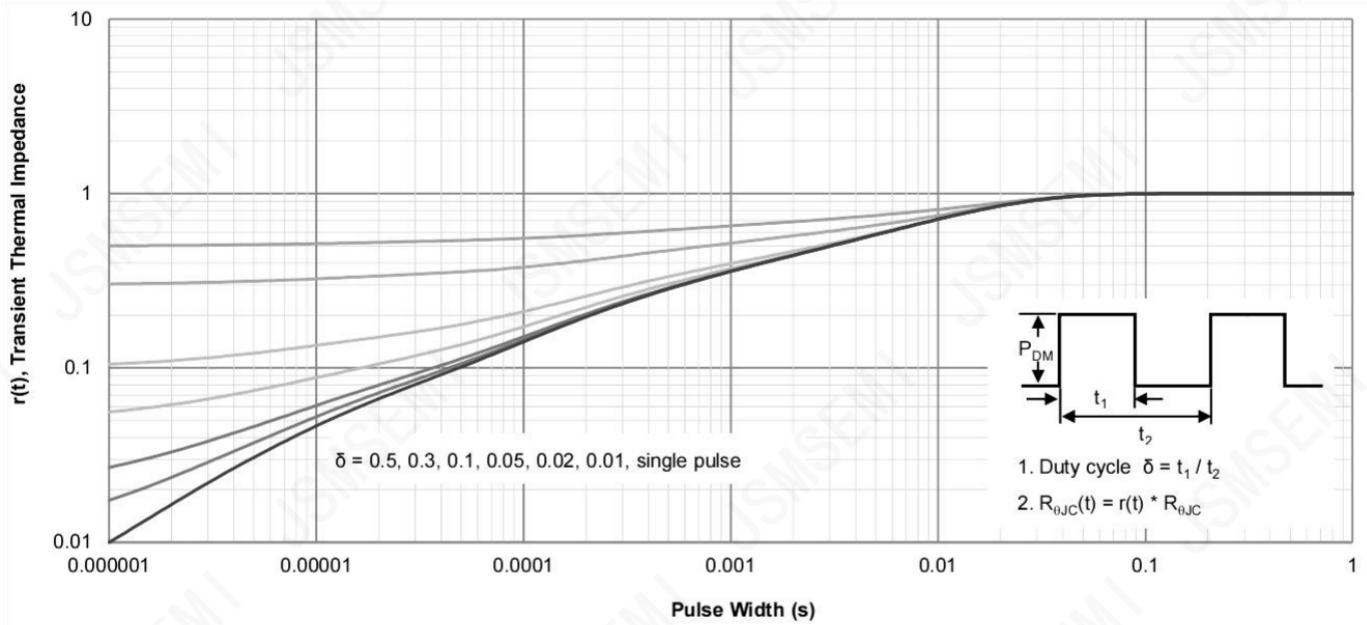
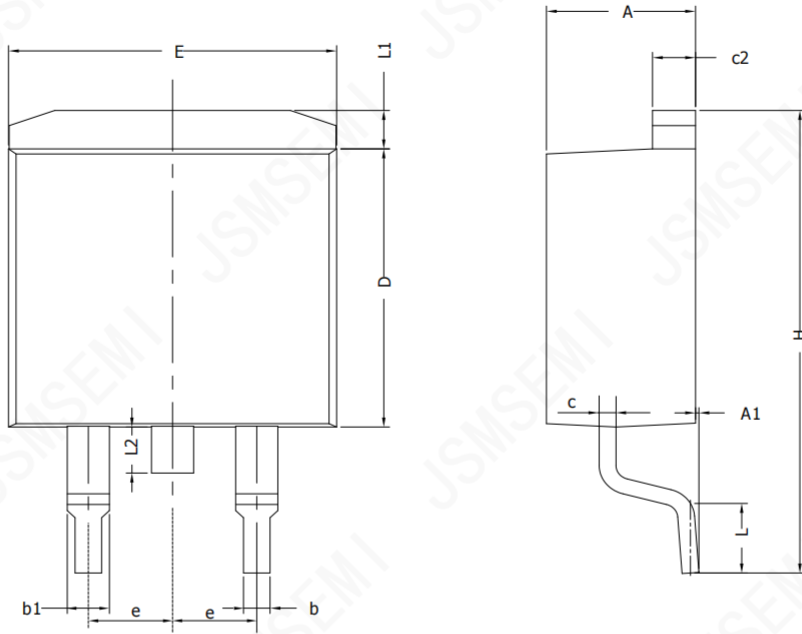


Figure 13: Normalized Maximum Transient Thermal Impedance

Package Information

TO-263-2



SYMBOL	MIN	NOM	MAX
A	4.30	4.57	4.72
A1	0	0.10	0.25
b	0.71	0.81	0.91
c	0.30	---	0.60
c2	1.17	1.27	1.37
D	8.50	---	9.35
E	9.80	---	10.45
e	2.54BSC		
H	14.70	---	15.75
L	2.00	2.30	2.74
L1	1.12	1.27	1.42
L2	---	---	1.75

Revision History

Rev.	Change	Date
V1.0	Initial version	9/17/2020

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