



## Description

The NTMD4840NR2G uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

## General Features

$V_{DS} = 30V$   $I_D = 8.5 A$

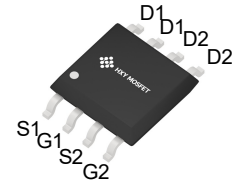
$R_{DS(ON)} < 18m\Omega$  @  $V_{GS}=4.5V$

## Application

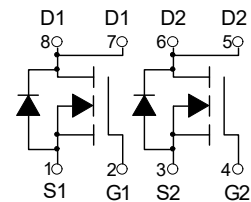
Battery protection

Load switch

Uninterruptible power supply



SOP-8  
(SOIC-8)



Dual N-Channel MOSFET

## Ordering Information

Product ID	Pack	Brand	Qty(PCS)
NTMD4840NR2G	SOP-8(SOIC-8)	HXY MOSFET	3000

## Absolute Maximum Ratings@ $T_J=25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_A=25^\circ C$	Drain Current, $V_{GS} @ 4.5V^3$	8.5	A
$I_D@T_A=70^\circ C$	Drain Current, $V_{GS} @ 4.5V^3$	5.8	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	37	A
$P_D@T_A=25^\circ C$	Total Power Dissipation	1.5	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{thj-a}$	Maximum Thermal Resistance, Junction-ambient <sup>3</sup>	85	$^\circ C/W$



**Electrical Characteristics ( $T_J=25\text{ }^\circ\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$	---	0.034	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=7A$	---	15	18	m $\Omega$
		$V_{GS}=4.5V, I_D=4A$	---	22	28	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	---	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-5.8	---	$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	$\mu\text{A}$
		$V_{DS}=24V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
gfs	Forward Transconductance	$V_{DS}=5V, I_D=7A$	---	6	---	S
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	2.5	---	$\Omega$
$Q_g$	Total Gate Charge (4.5V)	$V_{DS}=15V, V_{GS}=4.5V, I_D=7A$	---	6	---	nC
$Q_{gs}$	Gate-Source Charge		---	2.5	---	
$Q_{gd}$	Gate-Drain Charge		---	2.1	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V, R_G=3.3\Omega$ $I_D=7A$	---	2.4	---	ns
$T_r$	Rise Time		---	7.8	---	
$T_{d(off)}$	Turn-Off Delay Time		---	22	---	
$T_f$	Fall Time		---	4	---	
$C_{iss}$	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	572	---	pF
$C_{oss}$	Output Capacitance		---	80	---	
$C_{rss}$	Reverse Transfer Capacitance		---	65	---	
$I_S$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V, \text{Force Current}$	---	---	7.3	A
$I_{SM}$	Pulsed Source Current <sup>2,5</sup>		---	---	37	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F=7A, di/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	20	---	nS
$Q_{rr}$	Reverse Recovery Charge		---	1.1	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.1\text{mH}, I_{AS}=21A$
- 4.The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- 5.The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.



### Typical Characteristics



Fig.1 Typical Output Characteristics

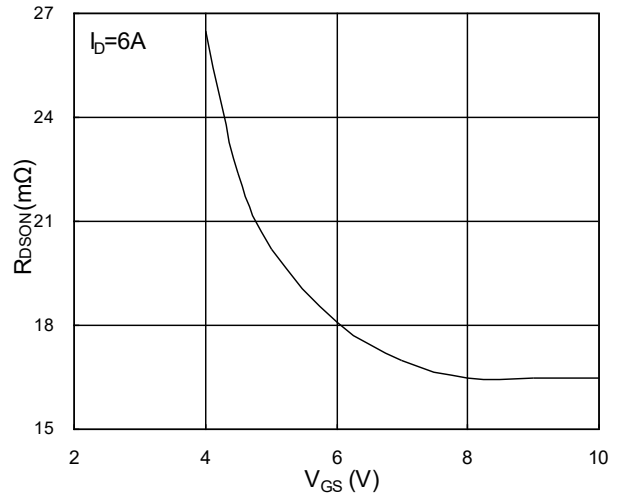


Fig.2 On-Resistance vs. G-S Voltage

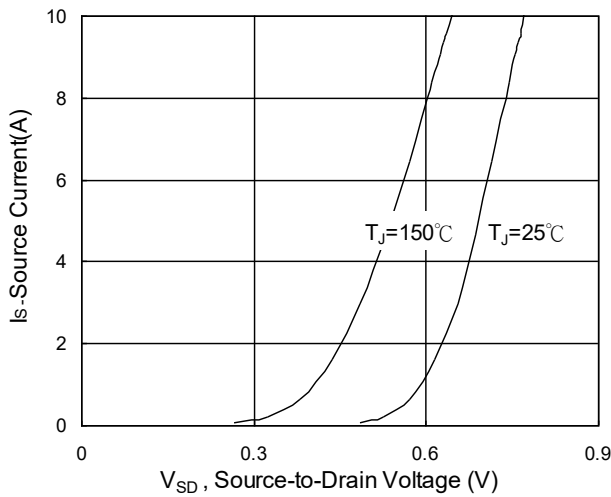


Fig.3 Forward Characteristics Of Reverse

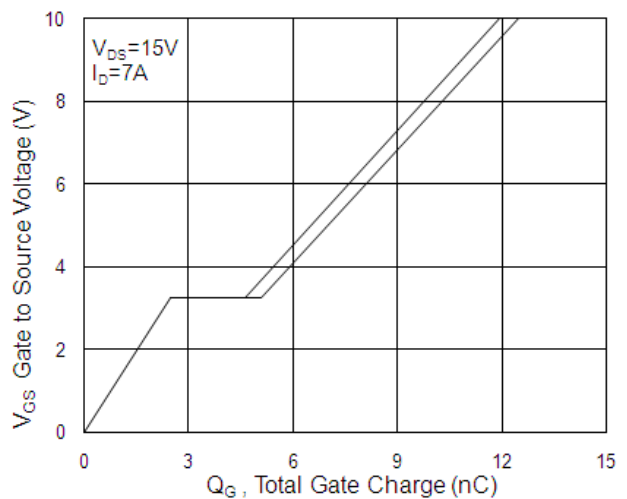


Fig.4 Gate-Charge Characteristics

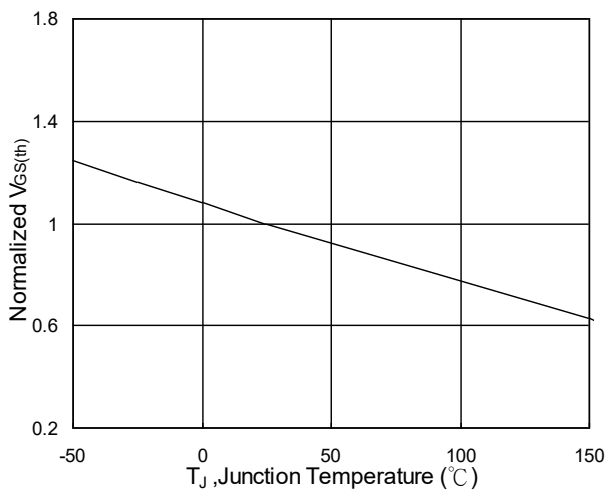


Fig.5 Normalized V<sub>GS(th)</sub> vs. T<sub>J</sub>

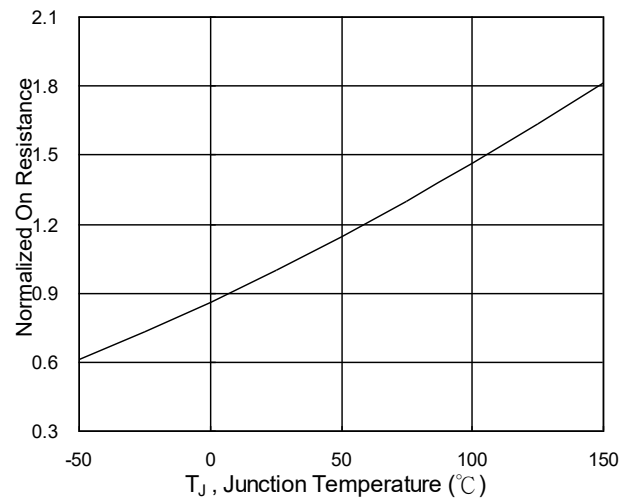


Fig.6 Normalized R<sub>DS(on)</sub> vs. T<sub>J</sub>

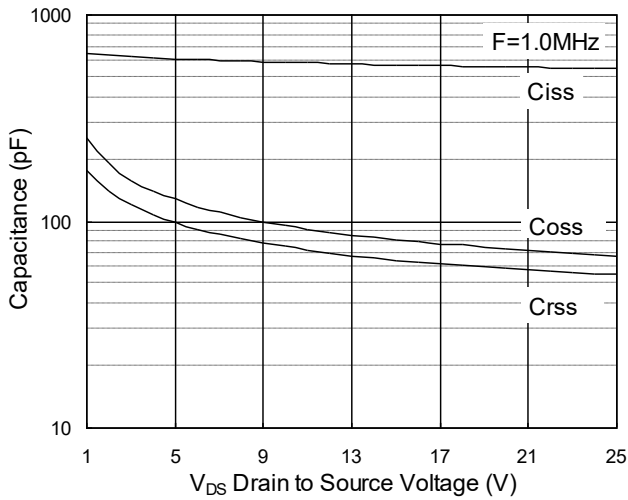


Fig.7 Capacitance

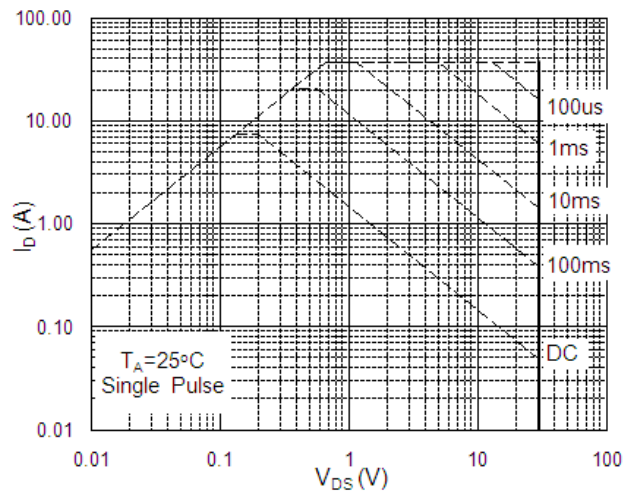


Fig.8 Safe Operating Area

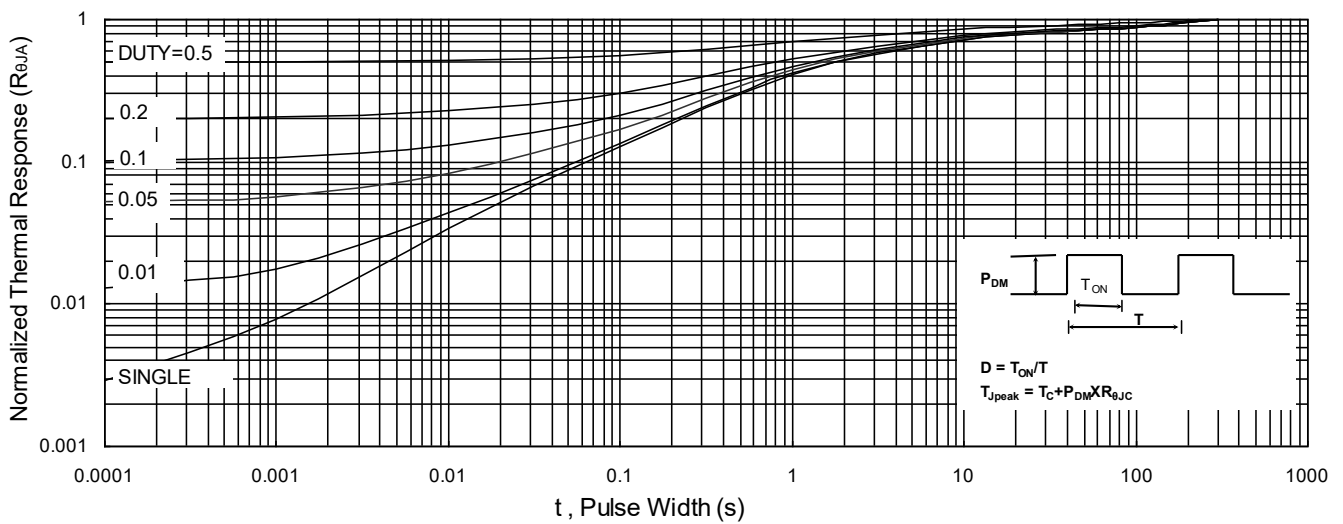


Fig.9 Normalized Maximum Transient Thermal Impedance

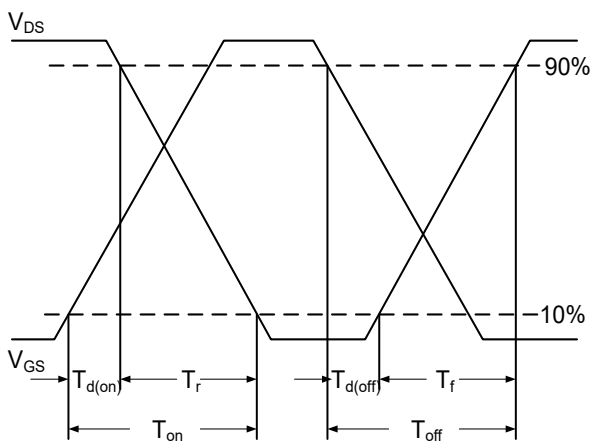


Fig.10 Switching Time Waveform

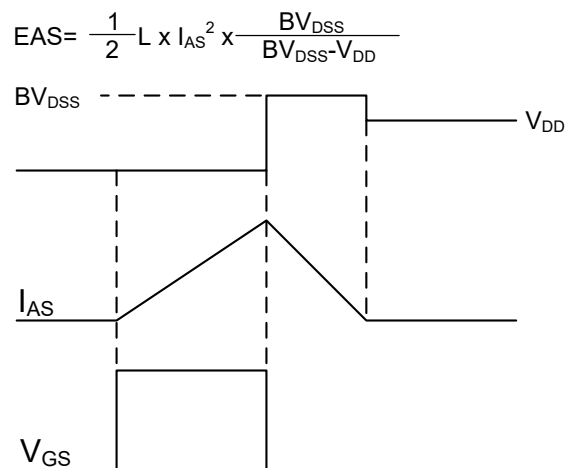
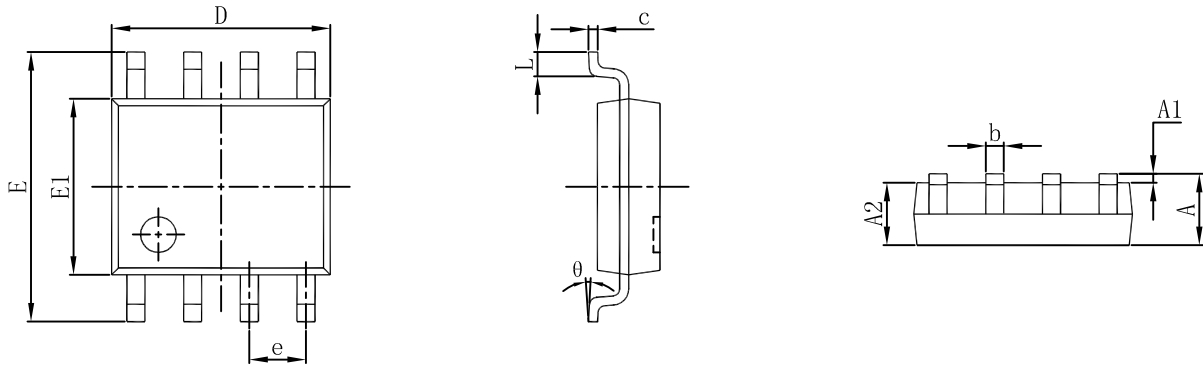


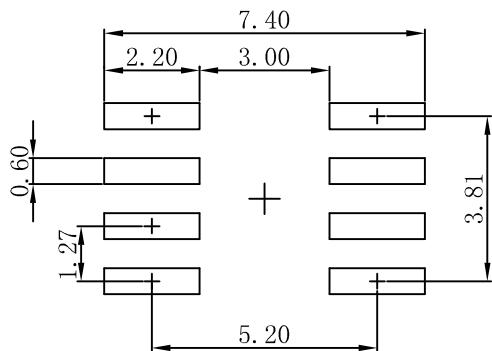
Fig.11 Unclamped Inductive Switching Waveform



### SOP-8(SOIC-8) Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
theta	0°	8°	0°	8°



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance:  $\pm 0.05\text{mm}$ .  
 3. The pad layout is for reference purposes only.



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