钍地半导体
Tudi Semiconductor

Product Specification

TUDI-TMP75B

1.8V digital temperature sensor with two-wire interface and alarm function

网址 www.sztdbdt.com

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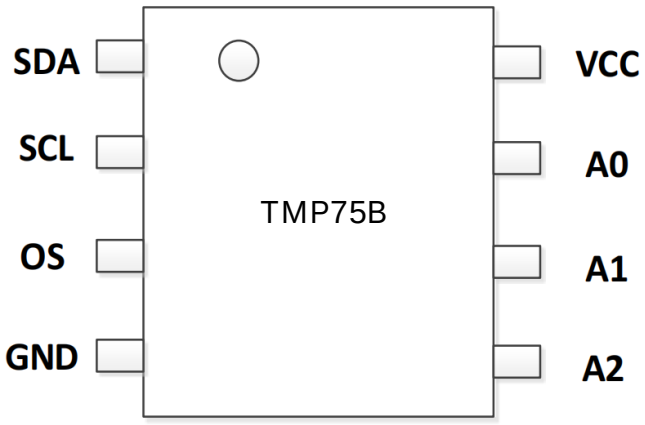
semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Feature

- a power supply range of 1.4 V to 3.6 V.
- I2C bus interface supports up to 8 devices on the same bus.
- Power supply voltage range: 1.4 V to 3.6 V
- The temperature range is from-55°C to +125°C.
- The frequency range is 20 Hz to 400 kHz, with a bus fault timeout feature that prevents bus suspension.
- An 11-bit ADC with a temperature resolution of 0.0825 °C
- Programmable alarm temperature thresholds and hysteresis values
- Temperature accuracy:

0°C From to +50°C: ±0.5
–25°C to +100°C: ±1°C
–55°C to +125°C: ±1 .5°C



SOP8 MSOP8 Pin Diagram

- The power supply current in shutdown mode is 0.1 µA to achieve energy savings.
- It can be used independently as a thermostat when powered on.
- ESD protection exceeds the requirements of JESD22-A114 4500 V HBM and JESD22-C101 1000V CDM.
- Complete the latch test for currents exceeding 100 mA according to the JEDEC standard JESD78.
- Small 8-pin package type: SOP8 , MSOP8.

Applications

- Autonomous Driving Module
- Media Center and Display
- Audio Head Unit and Digital Cockpit
- Intelligent Telematics and Gateway
- ADAS Domain Controller and SeFusion
- Body Control Module
- On-Board Charger
- Battery System

The TMP75B undergoes precision calibration at the factory, so users do not need to perform any additional processing on the temperature output.

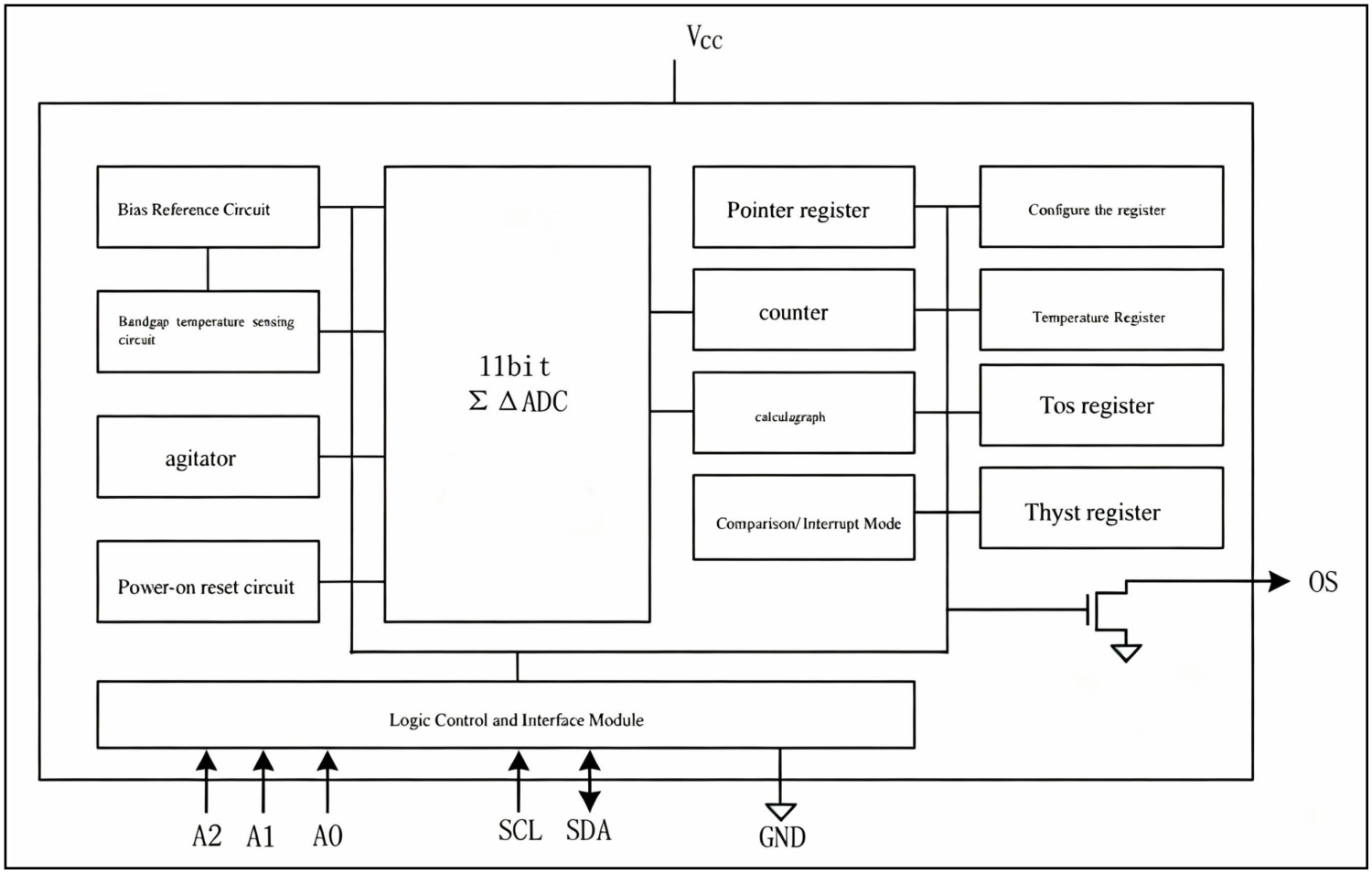
Explanation

The TMP75B is a temperature-to-digital converter that employs an on-chip bandgap temperature sensor andΣ-Δ A/D conversion technology, featuring an overheat detection output. The TMP75B includes a series of data registers: configuration registers (Conf) storing device settings such
as operating mode, OS operating mode, OS polarity, and OS fault queue (for detailed description, see Section 7 "Functional Description"); temperature registers (Temp) for storing digital temperature data; and setting point registers(Tos and Thyst) containing program-mable overheat shutdown thresholds and hysteresis limits, all communicable with the controller via a 2-wire serial I ²C bus interface. The device also provides an opendrain output (OS), which activates when temperatures exceed programmed threshold values.
The temperature sensor features three logical address pins, enabling up to eight devices connected on the same bus without address conflict.
The TMP75B can be configured in various operating modes. It can be set to normal mode for periodic environmental temperature monitoring or to shutdown mode to minimize power consumption. The OS output operates in either of two optional modes: OS comparator Mode or OS Interrupt Mode, with its output level configurable as high or low. Both the number of consecutive failures required to activate the OS output and the setpoint threshold are programmable.
The temperature register consistently stores 11-bit binary complement data, with a temperature resolution of 0.0825°C. This high resolution is particularly advantageous for applications requiring precise measurement of thermal drift or thermal escape. Accessing the TMP75B does not interrupt the ongoing temperature conversion process—the I2C bus interface remains entirely independent of the Σ-Δ converter—allowing continuous access without communication delays, even during a single conversion cycle. This ensures the device can promptly update the temperature register with the latest conversion results. Once updated, the new conversion values become immediately available.
When powered on, the TMP75B operates in normal mode: the OS is in comparator mode, with a temperature threshold of 80°C and a hysteresis value of 75°C. Therefore, it can function as an independent thermostat with these predefined temperature setpoints.
The TMP75B employs an on-chip bandgap temperature sensor to measure device temperature with a resolution of 0.0825°C, storing the 11-bit binary output from the 11-bit A/D converter in the device temperature register. This register can be read at any time by the controller on the I2C bus. Reading the temperature data does not interfere with the ongoing temperature conversion during the read operation.
The device can be configured to operate in normal or sleep mode. In normal operating mode, the temperature conversion is performed every 100 ms, and the temperature register is updated upon completion of each conversion. Within the approximately 100 ms conversion cycle (Tconv), the device requires only 10 ms to complete the temperature-to-data conversion —referred to as the "temperature conversion time" (tconv(T))—with the remaining time spent in idle mode. This feature significantly reduces device power consumption.

Explanation (Continue)

In sleep mode, the device remains inactive with data conversion conversion initiates upon power-on or upon returning from sleep mode to normal operation.
disabled; the temperature register retains the latest measurement results, while its I2C bus interface remains functional for register write/write operations. The device's operating mode is controlled by programming the B0 bit of the configuration register. Temperature Furthermore, at the end of each conversion in normal mode, the temperature data in the temperature register is automatically compared with the data in the overtemperature shutdown register Tos (or Tth (^{ots})) and the data stored in the lag register Thyst (Thyst) to determine the device's output state accordingly. The device's Tos and Thyst registers support read/write operations and both operate using 9-bit binary digital data. To align with this 9-bit operation, the temperature register compares only the most significant 9 bits (MSB bits) of its 11-bit data.
The comparison method for the output response of the OS port is determined by the B1 bit of the configuration register, while the user-defined fault queue is defined by the configuration bits B3 and B4 .
In comparator mode, the OS port output behaves like a thermostat: it activates when the temperature exceeds Tth ($_{ots}$) and resets when the temperature falls below Thyst. Reading the register or placing the chip in sleep mode does not alter the chip's output state. In this mode, the OS output can be used to control the cooling fan or thermal switch.
In interrupt mode, the output behavior of the OS port is used for hot interrupts. When the device is powered on, it is first activated only when the temperature exceeds T Th(ots); thereafter, it remains in this state indefinitely until reset by reading any register. Once the OS output is activated via crossing T Th ($_{ots}$) and then reset, it can only be reactivated again when the temperature falls below Th Yst; subsequently, it remains activated indefinitely until reset by reading any register. The operating system interrupt operations proceed in the following sequence: T Th ($_{ots}$) trip, Reset, Th Yst trip, Reset, T Th ($_{ots}$) trip, Reset, Th Yst trip, Reset, etc. Setting bit 0 of the configuration register to put the device into sleep mode also resets the OS output.In both scenarios—comparator mode and interrupt mode—the OS output is activated only when multiple consecutive faults defined by the fault queue are met. The fault queue is programmable and stored in two bits of the configuration register, B3 and B4 . Additionally, by setting the corresponding bit B2 in the configuration register, the OS output enable state can be selected as high or low.
Upon power-on, the device enters normal mode with Tth ($_{ots}$) at 80°C, Thyst at 75°C, OS activation status at low, and the fault queue equal to 1. The first transition occurs within approximately 100 ms after power-on; temperature readings are unavailable prior to completion of this transition.
The temperature response of the OS port is shown in Figure 1.

Block diagram



Pin Description

Pin name	Pin	Description
SDA	1	Digital I/O,I²C bus bidirectional data line;open-drain output.
SCL	2	Digital input:I2C bus clock input.
OS	3	Overtemperature protection/interrupt output;open drain.
GND	4	The ground is connected to the system ground.
A2	5	Digital input:user configures address bit 2.
A1	6	Digital input:user configures address bit 1.
A0	7	For digital input,the user configures address bit 0.
Vcc	8	Power Supply Port

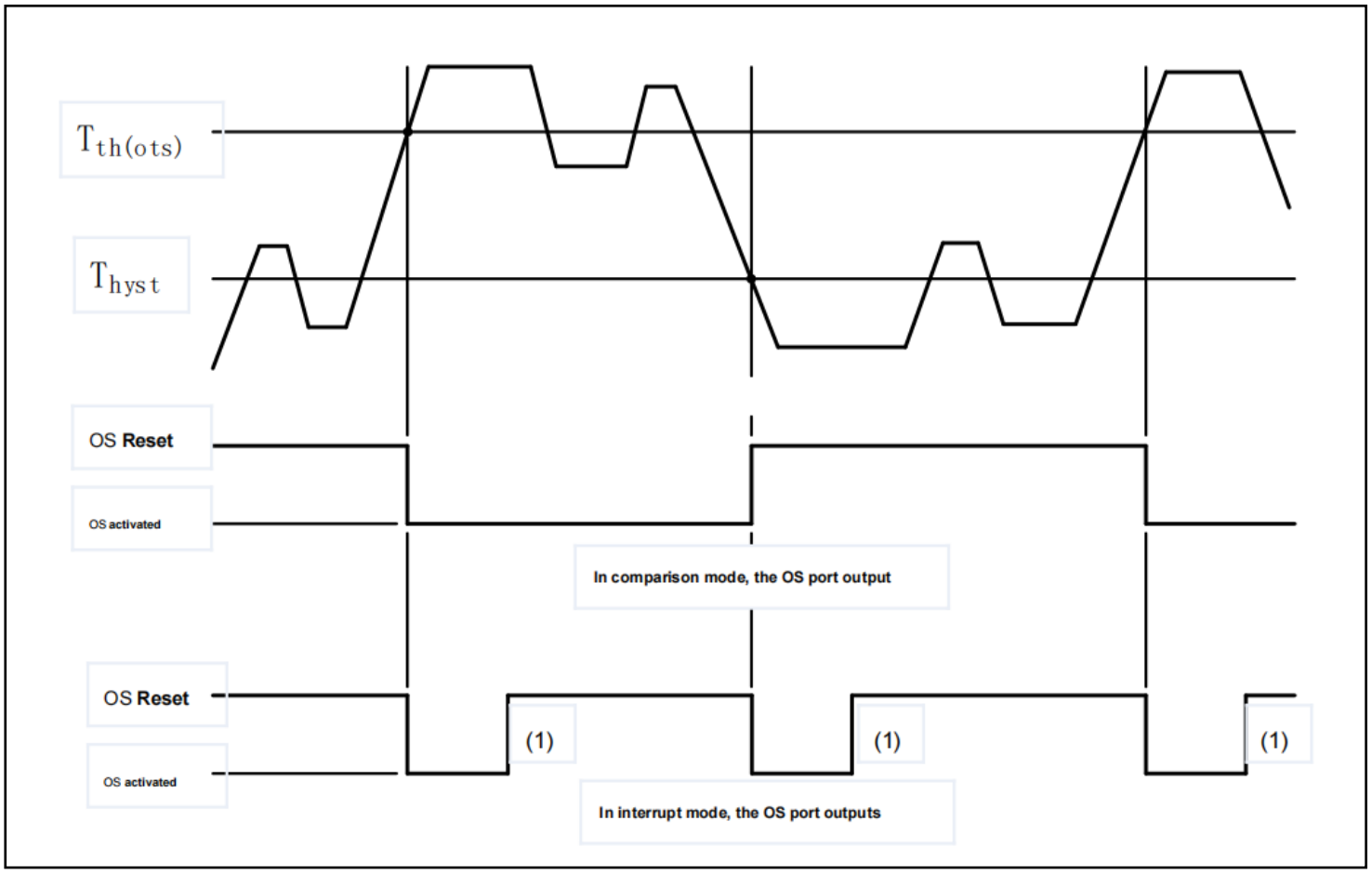


Figure 1. OS Port Output Diagram

(1) The OS is reset by reading the register or configuring the chip into sleep mode. Assume the fault queue is satisfied at each Tth(ots) and Thyst crssing point.

I2 C Bus Interface

The TMP75B can connect to a compatible 2-wire serial I2C bus, functioning as a slave device controlled by either a controller or master device, and communicates via the two device terminals SCL and SDA. Data must be written to the controller from the slave terminal SDA/SDA via these terminals. Note that if the pull-up resistor on the I2C bus is not installed as required, each of these ports requires an external pull-up resistor of approximately 10 kΩ. The bus communication protocol is detailed in Section 7.10.

Bus Error Timeout

If the SDA remains at a low level for more than tto (minimum 75 ms/13.3 Hz; ensure a minimum duration)At 50ms/20Hz, the TMP75B resets to an idle state (SDA released) and waits for new startup conditions. This ensures that the TMP75B does not disconnect from the bus when transmission conflicts occur.

Machine Address

The TMP75B slave address on the I2C bus is determined by the logic levels of pins A2 , A1 , and A0. Each of these pins is typically connected to GND (logic 0) or VCC (logic 1). These pins represent the three least significant bits (LSB) of the device's 7-bit address. The remaining four most significant bits (MSB) of the address data are preset to "1001" by default via internal wiring within the TMP75B. Table 1 displays the complete device addresses and indicates that up to eight devices can be connected to the same bus without address conflicts. Since the input pins SCL, SDA, and A2 to A0 have no internal bias, they should never remain floating in any application.

1 = Vcc; 0 = GND.

MSB						LSB
1	0	0	1	A2	A1	A0

Table 1. Address List

Register List

The TMP75B includes four data registers adjacent to the pointer register, as shown in Table 2 .Table 2 also displays the pointer values, read/write capabilities, and default contents of these registers when powered on.

Register name	Pointer value	Read/rite	Default power-on	Description
Conf	01h	Read/Write	00h	Configuration register:Contains an 8-bit data byte;used to set the chip operating conditions;default value is 0.
Temp	00h	Read only	n/a	Temperature register:Contains 28-bit data bytes for storing measured temperature data.
Tos	03h	Read/Write	5000h	Overtemperature shutdown register:Contains two 8-bit data bytes storing the Tth (ots)value;default value =80℃.
Thyst	02h	Read/Write	4B00h	Hysteresis register:Contains 28-bit data bytes;used to store the hysteresis value;default value =75℃

Table 2.Register List

Pointer Register

The pointer register contains a 8-bit data field, where the two least significant bits (LSB) represent the pointer values of the other four registers, while the remaining six most significant bits (MSB) are set to0 , as shown in Tables 3 and 4. The user cannot directly access the pointer register; instead, data register selection for write/read operations is achieved by incorporating the pointer data byte into the bus command.
When executing bus commands (including pointer bytes), the pointer value is latched into the pointer register; therefore, the pointer byte read from the TMP75Bmay or may not be included in the statement. When reading the register pre-set by the most recent pointer, the pointer byte
is not required. However, when reading a different register from the previous one, the pointer byte must be included. For write operations to the TMP75B, the pointer byte must always be included in the statement. The bus communication protocol is described in Section7.10.
Upon power-on, the pointer value is set to 00, and the temperature register is selected; subsequently, the user can read the temperature data without specifying the pointer byte.

B7	B6	B5	B4	B3	B2	B[1:0]
0	0	0	0	0	0	Pointer value

Table 3. Pointer Register

B1	B0	Register
0	0	Temperature Register (Temp)
0	1	Configure register (Conf)
1	0	Thyst Register
1	1	Overtemperature shutdown register(Tos)

Table 4.Pointer value

Configure the Register

The Configuration Register (Conf) is a write/read register containing an 8-bit non-complementary data byte, which is used to configure the chip for different operating conditions. Table 5 shows the bit allocation of this register.

Legend: * = default value.

Position	Symbol	Authority	Price	Description
B[7:5]	reserved	Read/Write	000*	Reserved for manufacturer use;maintain at zero during normal operation.
B[4:3]	OS_F_QUE[1:0]	Read/Write		OS Fault Queue Programming
			00*	Queue value =1
			01	Queue value =2
			10	Queue value =4
			11	Queue value =6
B2	OS_POL	Read/Write		OS polarity selection
			0*	The OS activation output is at a low level.
			1	OS activation output high level
B1	OS_COMP_INT Read/Write			OS Work Mode Selection
			0*	OS Compaison Mode
			1	OS Interrupt Mode
B0	SHUTDOWN Read/Write			Chip operating mode selection
			0*	normal
			1	Sleep

Table 5. Configuration Registers

Temperature Register

The Temperature Register (Temp) stores the temperature measurement or monitor results upon each analog-to-digital conversion. This register is read-only and contains two 8-bit data bytes, comprising one most significant byte (MSByte) and one least significant byte (LSByte). However, only 11 bits within these bytes are used to store temperature data in two's complement format, with a resolution of 0.0825°C. Table 6 shows the bit arrangement of the temperature data within the data bytes.

MSByte								LSByte							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X

Table 6. Temp register

When reading the temperature register, all 16 bits of the two data bytes (MSByte and LSByte) are provided to the bus and must be fully captured by the controller to complete the bus operation. However, only the 11 most significant bits should be used; the 5 least significant bits of LSByte are zero and should be ignored. One method for calculating the temperature value from the 11-bit temperature data is:

1. If the temperature data MSByte bit D10 = 0 , the tempe-rature is positive. The temperature value (°C) is calculated as: (+temperature data) × 0.0825°C;
2. If the temperature data MSByte bit D10 = 1 , the temperature is negative.

Temperature value (°C) = (supplement code of the two temperature data points) × 0.0825°C.

Table 7 Shows Examples of Temperature Data and Temperature Values.

11bit binary number	Hexadecimal number	Decimal number	Temperature scale
01111111000	3F8	1016	+127.000℃
01111110111	3F7	1015	+126.875℃
01111110001	3F1	1009	+126.125 ℃
01111101000	3E8	1000	+125.000℃
00011001000	0C8	200	+25.000 ℃
00000000001	001	1	0.125℃
00000000000	000	0	0.000℃
11111111111	7FF	-1	-0.125℃
11100111000	738	-200	-25.000℃
11001001001	649	-439	-54.875℃
11001001000	648	-440	-55.000℃

Table 7.Temperature register value

For applications requiring 9-bit temperature data that replaces the industrial standard XX75, only the 9 most significant bits (MSB) of two bytes are used, while the 7 least significant bits (LSB) are ignored. The TMP75B defines its 9-bit temperature data with a resolution of 0.5°C, identical to the standard XX75 specification, and operates similarly to the Tos and Thyst registers.You can also use a single-byte read command to obtain the MSB of the temperature. In this case, the temperature resolution will be set to 1 .00°C.

MSByte								LSByte							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D33	D2	D1	D0	X	X	X	X	X	X	X

Table 8 Overtemperature Turn-off Threshold Register and Hysteresis Register

Overtemperature shutdown threshold (Tos) and hysteresis register

These two registers are write/write registers, also known as setpoint registers. They store user-defined temperature thresholds—called the overtemperature shutdown threshold(Tth(ots)) and hysteresis temperature (Thyst)—for device watchdog operations. At the end of each conversion cycle, the temperature data is compared with the values stored in these registers to determine the OS output state; see Section 7.1.Each setpoint register contains two 8-bit data fields—a MSByte and an LSByte—similar to the temperature register. However, only 9 bits of each byte are used to store the setpoint value in binary format, with a resolution of 0.5°C. Tables 8 illustrate the bit arrangement of the Tos and Thyst data within the data bytes.
Note that since only 9 bits of data are used in the set value register, the device compares data using only the upper 9 bits (MSB) of the temperature data.
When reading the set value register, all 16 bits are provided to the bus and must be collected by the controller to complete the bus operation. However, only the 9 most significant bits should be used, while the 7 least significant bits of the LSByte are set to zero and should be ignored.
summary。

Shows Examples of Set Data and Values.

Binary number	Hexadecimal number	Decimal number	Temperature scale
011111010	0FA	250	+125℃
000110010	32	50	+25℃
000000001	001	1	+0.5℃
000000000	000	0	0℃
111111111	1FF	-1	-0.5℃
111001110	1CE	-50	-25.0℃
110010010	192	-110	-55.0℃

Table 9. Data and Numerical Settings for Tos and Thyst

OS Output and Polarity

The OS side provides an open-drain output, whose state indicates the result of the device watchdog operation described in Section 7.1. To observe this output state, an external pull-up resistor is required. The resistor should be as large as possible, up to 200 kΩ.Minimize temperature reading errors caused by internal heating induced by high OS notch current.
By programming bit B2 (OS_POL) in the Conf register, you can set the OS output active state to either high or low: setting OS_POL to logic 1 activates the OS output at high level, while setting bit B2 to logic 0 activates it at low level. Upon power-on, OS_POL defaults to logic 0 , resulting in the OS output being low-level.

OS Comparison and Interrupt Mode

As described in Section 7.1 , the OS output response is the comparison result between temperature register data and data from the Tos and Thyst registers, depending on the selected operating system mode: OS compare mode or interrupt mode. The OS mode is selected by configuring bit B1 of the Conf register (OS_COMP_INT): setting OS_COMP_INT to logic 1 selects OS interrupt mode, while setting it to logic 0 selects OS compare mode. Upon power-on, OS_COMP_INT defaults to logic 0 , selecting OS compare mode.
The primary distinction between these two modes lies in their behavior: In the comparison mode, the OS is activated when the temperature exceeds Tth (ots) and resets when the temperature falls below Thyst; reading the register or entering chip sleep mode does not alter the OS output state. In the interrupt mode, however, once the OS is activated by temperatures exceeding Tth (ots) or falling below Thyst, the OS output remains activated indefinitely until the register is read, after which the OS output is reset.
The temperature thresholds Tth (ots) and Thyst must satisfy Tth (ots)> Thyst. Otherwise, the OS output status will be undefined.

OS Fault Queue

The fault queue is defined as the minimum number of consecutive failures requiring active OS output. This prevents false activation due to noise. Since failures are determined upon completion of data conversion, the fault queue is also defined as the consecutive conversion count required for temperature trip activation.
By programming the two bits B4 and B3 in the Conf register (OS_F_QUE[1:0]), you can set the fault queue value. Note that the programming data differs from the fault queue value. Table 9 shows their one-to-one correspondence. Upon power-on, the fault queue data is 0 and the fault queue value is 1.

Fault queue data		Fault queue value
OS_F_QUE[1]	OS_F_QUE[0]	Decimal system
0	0	1
0	1	2
1	0	4
1	1	6

Table 9. List of Fault Cohorts

Sleep Mode

Select the operating mode by programming the B0 bit (sleep) in the Conf register. Setting B0 to logic 1 puts the device into sleep mode. Resetting the B0 bit to logic 0 returns it to normal mode. In sleep mode, approximately 0.1 μA of current is consumed; temperature conversion ceases, but the I2C bus interface remains active and supports register write/write operations. Upon entering sleep mode, the chip output remains unchanged in comparator mode and is reset in interrupt mode.

Default Power-on and Power-on Reset

Default power-on state of TMP75B:

- Normal operating mode
- OS Comparison Mode
- T_{th}(ots)=80℃
- Thys=75℃
- Set the OS output to low level
- Pointer register value 00 (temperature register)

When the power supply voltage drops below approximately 1.0 V (POR) and remains below this level for more than 2 μs, then rises again, the chip resets to its default power-on state.

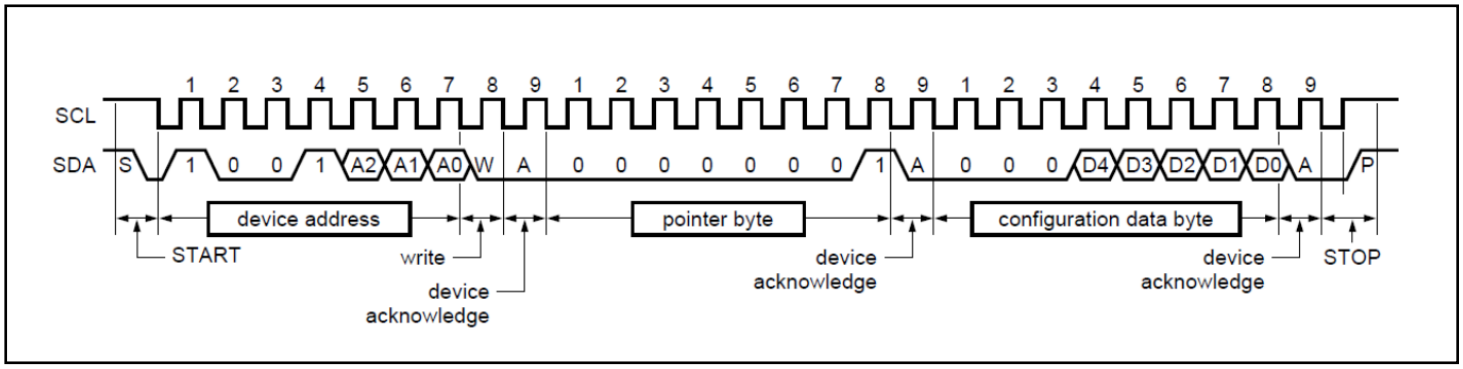
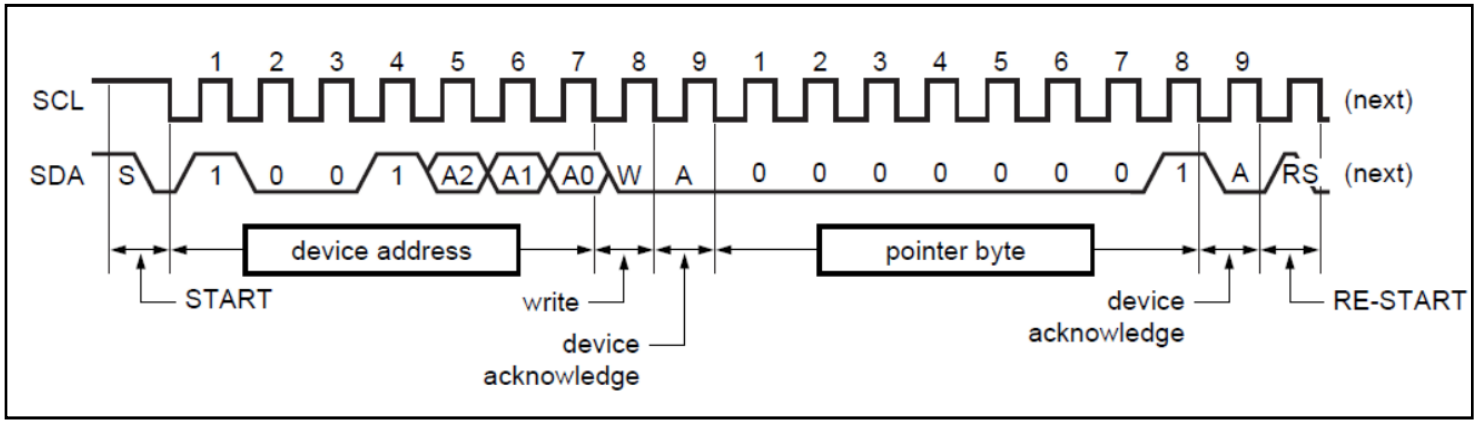


Figure 2. Writing Configuration Registers (1 Byte Data)



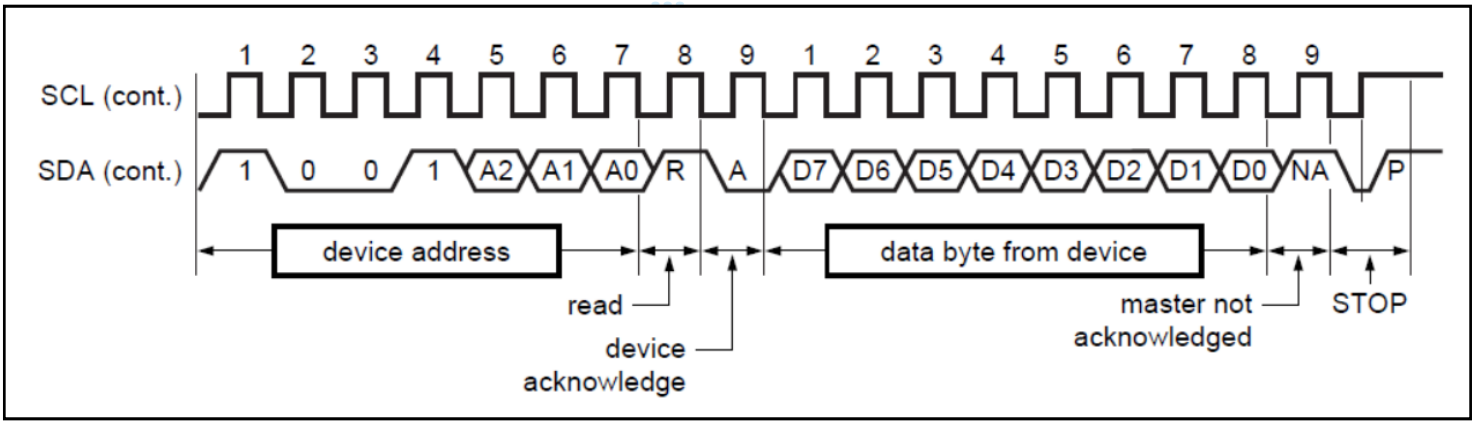


Figure 3. Reading Configuration Register (1-Byte Data)

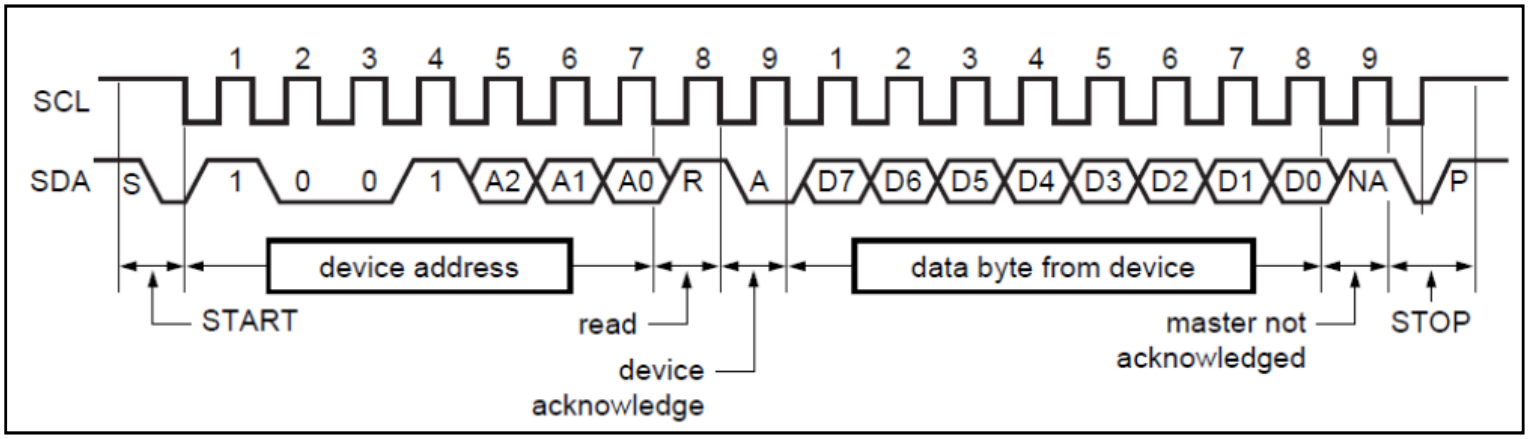


Figure 4 . Reading the Configuration or Temperature Register Using a Preset Pointer (1 -Byte Data)

Register Read/Write Protocol

Communication between the host and the TMP75B must strictly adhere to the rules defined by I2C bus management. The protocol for TMP75B register read/write operations follows the
definitions shown in Figures 2 through 7:

1. Before communication occurs, the I2C bus must be idle or not busy. This means that the SCL and SDA lines must be released by all devices on the bus and pulled high by the pull-up resistors on the bus.
2. The host must provide the SCL clock pulses required for communication. Data is transmitted as a sequence of 9 SCL clock pulses for every 8 bits of data, followed by a 1-bit ACK.
3. During data transmission, apart from start and stop signals, the SDA signal must remain stable when the SCL signal is high. This means the SDA signal can only change during the brief lowlevel duration of the SCL line.
4. S: The start signal, issued by the host to initiate communication. When SCL is high, SDA transitions from high to low.
5. RS: A restart signal identical to the startup signal, used to initiate read commands following write commands.

6. P: Stop signal issued by the host to terminate communication; SDA transitions from low to high, while SCL remains high. The bus is released.
7. W: Write bit, when the write/read bit in the write command is 0.
8. R: Read bit, when the write/read bit in the read command is 1.
9. A: The slave ACK bit returned by the TMP75B . If functioning normally, it is 0; if malfunctioning, it is
1. The host must release the SDA line during this period to allow devices on the bus to control it .
10. A': The host ACK bit is not returned by the slave but is issued by the host or the host during the reading of 2 bytes of data. Within this clock cycle, the host must set the SDA line to low to indicate that the first byte has been read, enabling the device to provide the second byte to the bus.11. NA: No ACK bit. During this clock cycle, both the device and the host release the SDA line upon completion of data transmission, enabling the host to generate a stop signal.
12. In the write protocol, data is transmitted from the host to the device; the host controls the SDA line, except during the clock cycle when the device sends its acknowledgment signal to the bus.
13. According to the protocol, data is transmitted from the device to the bus. The host must release the SDA line during the period when the device is transmitting data and controlling the SDA line, except during the clock cycle when the host sends its acknowledgment signal to the bus.

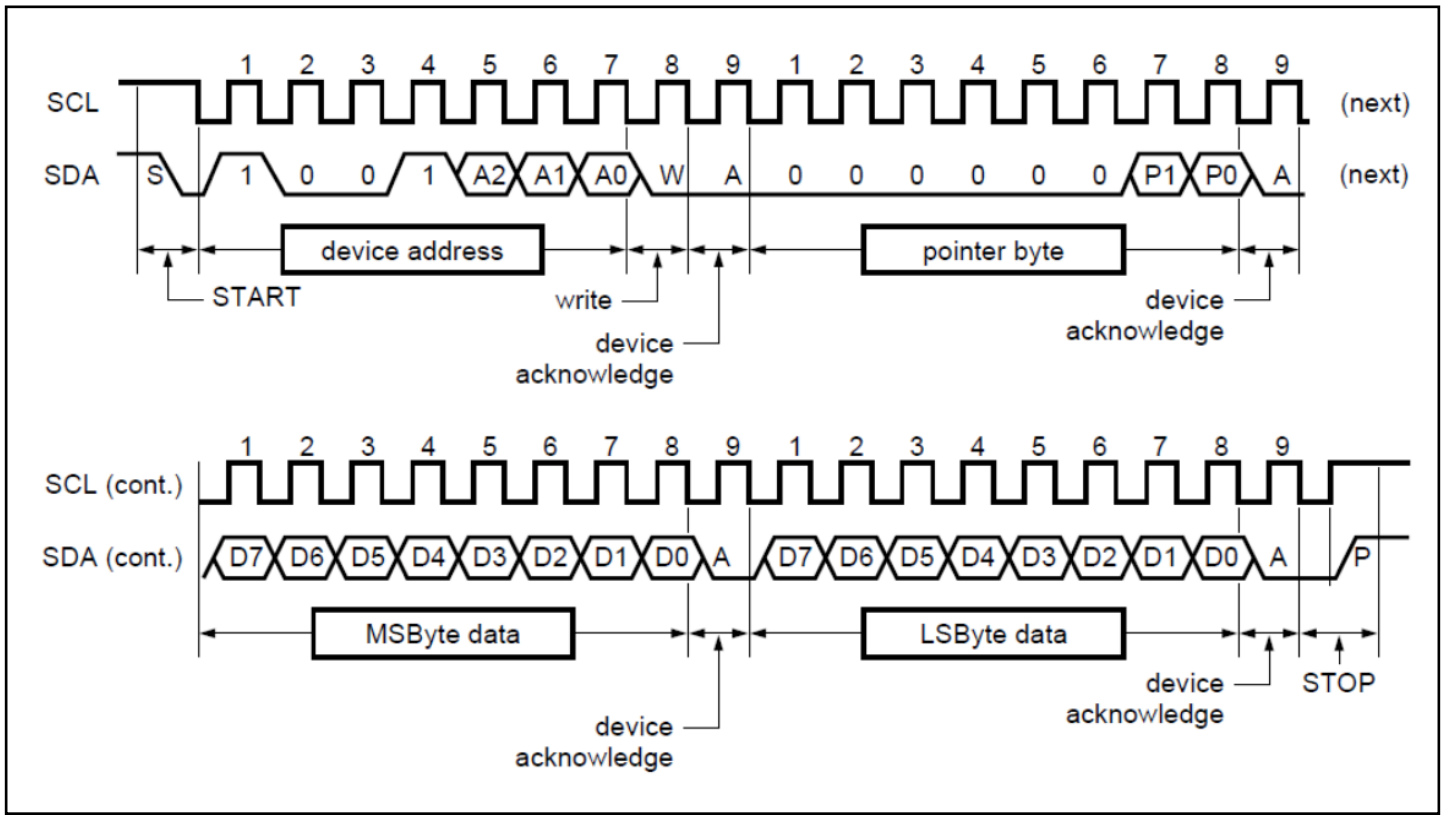


Figure 5. Write the Tos or Thyst Register (2-Byte Data)

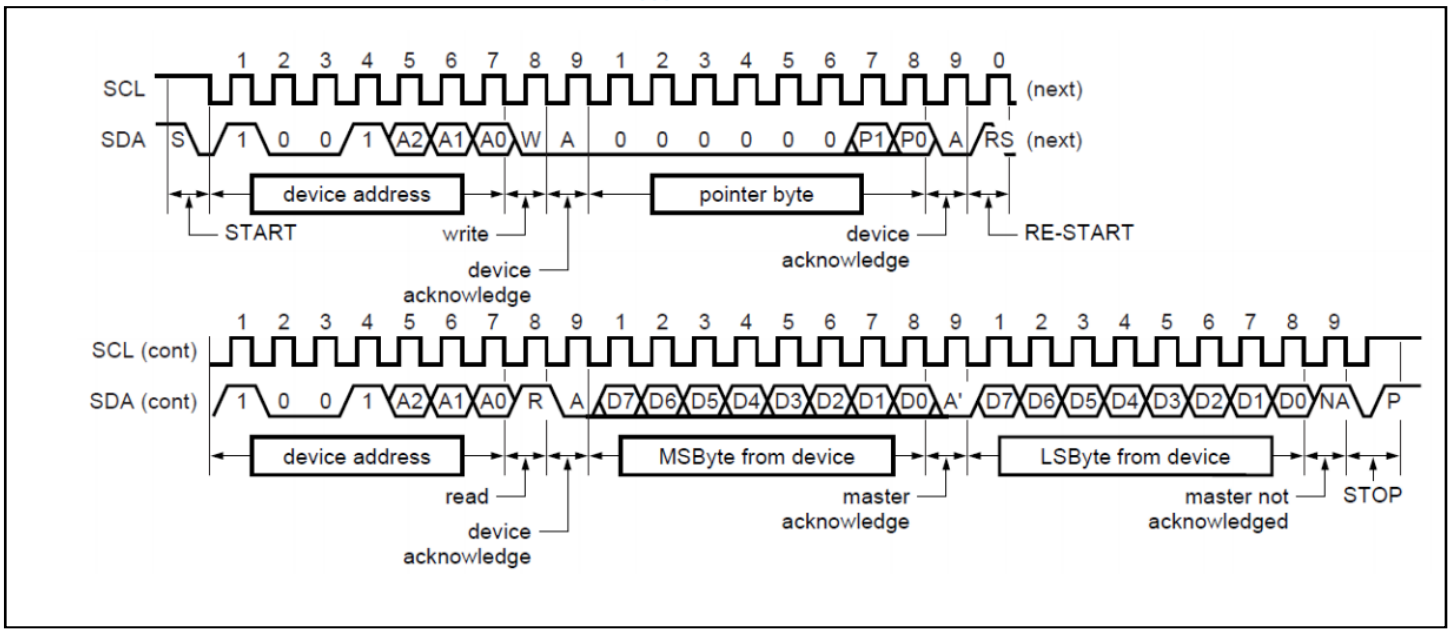


Figure 6. Read Temperature from the Tos or Thyst Register (2-Byte Data)

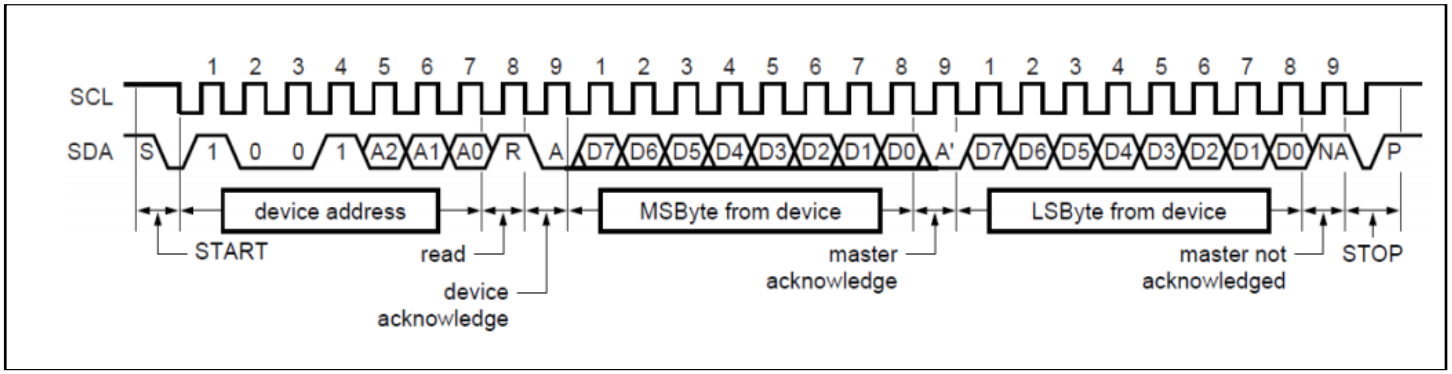


Figure 7. Read the Temperature, Tos, or Thyst Register Using a Preset Pointer (2-Byte Data)

Application Message

Temperature Precision

Since the local channel of the temperature sensor measures the mold temperature transmitted from its own body, it is essential to stabilize and saturate the device substrate's temperature for accurate readings. As the TMP75B operates at low power levels, thermal gradients within the device package have minimal impact on measurements. Measurement accuracy primarily depends on the ambient temperature, which is influenced by several factors: the printed circuit board housing the device; airflow contacting the device substrate (significant differences between ambient air temperature and PCB temperature may lead to unstable readings due to varying thermal paths between the mold and environment); and when the device is fully

immersed in a hot bath, the bath's constant-temperature liquid provides an optimal thermal environment. Thermal probes housed in sealed end-metal tubes within temperature-controlled air also offer a reliable temperature measurement method.

To calculate the effect of self-heating, use Equation 1 below:

Equation 1 is the formula for calculating the self-heating effect:

$T=Rth(j\text{-}a)(1)(V_{DD}I_{DD}(AV))+(VOL(SDA)I_{OL}(sink)(SDA))+(VOL(EVENT)I_{OL}(sink)EVENT)$

among：

T=Tj–Tamb

Tj= Temperature of the joint

Tamb = room temperatu - re; Rth(j-a) = package thermal resistance; VDD = supply voltage; IDD(AV) = average current

VOL(SDA) =SDA low output voltage

VOL(EVENT) =EVENT Low Output Vol - tage IOL(sink) (SDA) =~~SDA Low~~ Output Current IOL(sink) EVENT =EVENT Low Output Current

Calculation example:

Tamb (typical temperature inside a laptop) = 50CI$_{DD}$(AV)=400A

VDD=3.6V

MaximumVOL$_{(SDA)}$=0.4V

IOL(sink)(SDA)=1mA

VOL$_{(EVENT)}$=0.4V

IOL(sink)EVENT=3mARth$_{(j\text{-}a)}$=56Self-heating cau - sed by power consumption in C/W:

$T = 56\ (3.6\ \ 0.4) + (0.4\ \ 3) + (0.4\ \ 1) = 56ÿ°C/W\ \ 3.04\ mW = 0.17\ °C$ (2)

Noise Effect

The design of the TMP75Bdevice incorporates excellent noise rejection performance:

- Both the SCL and SDA pins feature low-pass filters;
- The minimum hysteresis voltage for the input voltage thresholds of SCL and SDA ports is approximately 500 mV.
- All pins feature ESD protection circuits to prevent damage from voltage surges. The ESD protection on the address, OS, SCL, and SDA pins grounds these pins. Under any supply voltage, the latch-based device breakdown voltage for address/OS is typically 11 V, while that for SCL/SDA is usually 9.5 V, though these values vary depending on manufacturing process and temperature. Since no protective diode exists between SCL/SDA and VCC, the TMP75B does not maintain a low level on the I2C line when VCC is absent; consequently, if the TMP75B loses power, the I2C bus remains operational.

However, when the device is used in highly noisy environments, it is recommended to adopt proper layout practices and additional noise filters.

- Use a decoupling capacitor at the VCC pin.
- Keep the digital path away from the switch power supply.
- Long-distance communication requires appropriate terminals.
- Add capacitors to the SCL and SDA lines to improve the characteristics of the low-pass filter on the bus.

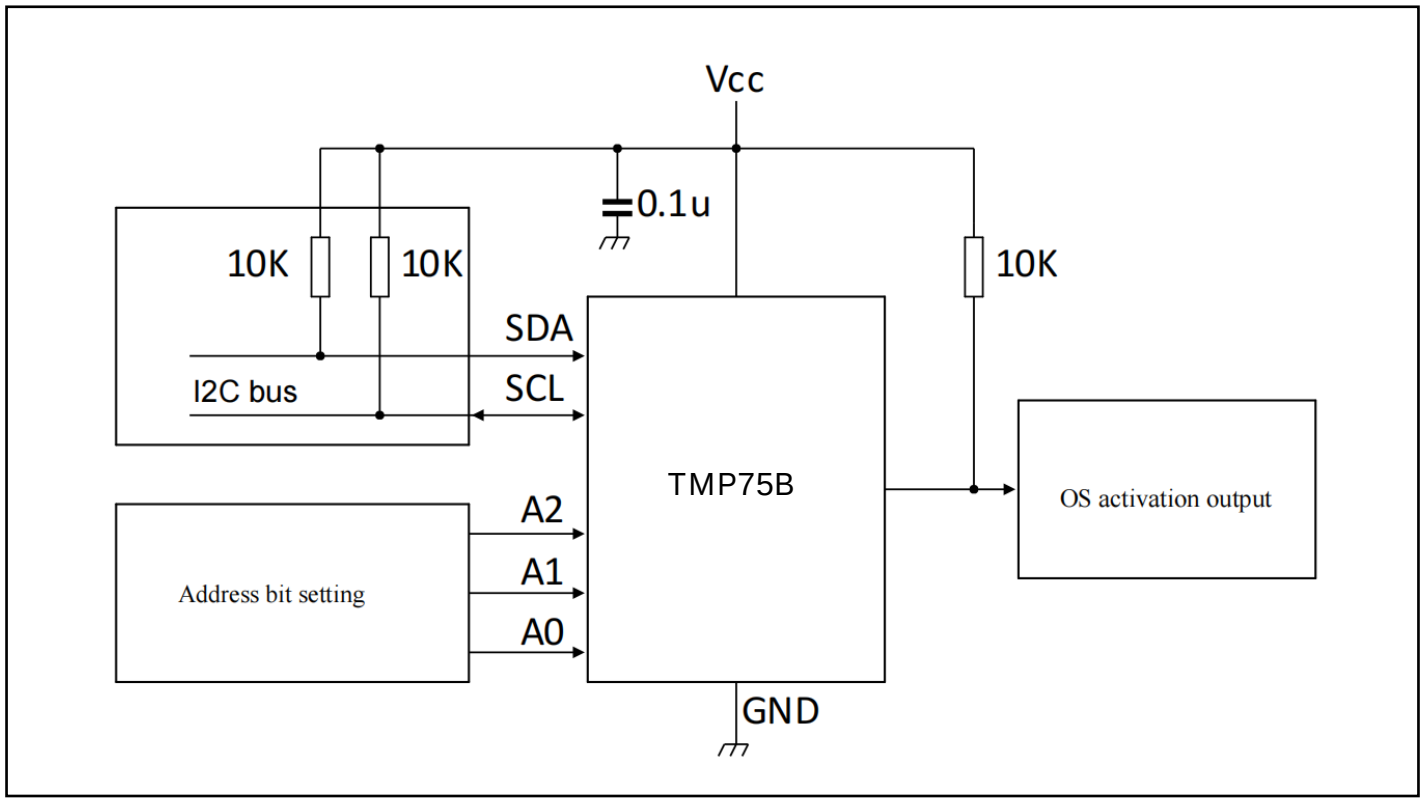


Figure 8. Typical Application

Recommended working conditions

Symbol	Parameter	State	Mini-mum	Typical case	Maximum	Unit
Vcc	Service voltage		1.4	/	3.6	V
Iamb	Room temperature		-55	/	+125	℃

Parameter limit

Symbol	Parameter	State	Minimum	Maximum	Unit
Vcc	Service voltage		-0.3	+6.0	V
V_1	Input voltage	At the input port	-0.3	+6.0	V
I	Input currenton	At the input port	-5.0	+5.0	mA
Io(sink)	Output leakage current	OS port	-	10.0	mA
Vo	Output voltage	OS port	-0.3	+6.0	V
Tstg	Storage temperature		-65	+150	℃
Tj	Junction temperature		-	150	℃

Dynamic Characteristics

VCC= 2.8 V to 5.5 V; Tamb= –55 °C to +125 °C;unless otherwise specified.

Symbol	Parameter	State		Mini-	Typical	Maxim	Unit
fscL	SCL clock frequency	See Figure 9		0.02	1	400	kHz
tHIGH	SCL clock high-level cycle			0.6	-	-	μs
tLow	SCL clock low-level cycle			1.3	-	-	μs
tHD;STA	Signal retention (repeat)time			100	-	-	ns
tsu;DAT	Data creation time			100	-	-	ns
tHD;DAT	Data retention time			0	-	-	ns
tsu;STO	Signal stop establishment time			100	-	-	ns
te	Drop-out time	SDA and OS output ports;			250	-	ns
		CL=400 pF;IoL=3 mA					
to	Timeout time		[2][3]	75	-	200	ms

[1] These specifications are guaranteed by the design and are not obtained through testing during production.
[2] This is the lower time limit for SDA serial interface reset.
[3] Maintaining the SDA line at a low level for more than t_{to}will cause the TMP75B to reset the SDA to the idle state of serial bus communication (SDA = 1).

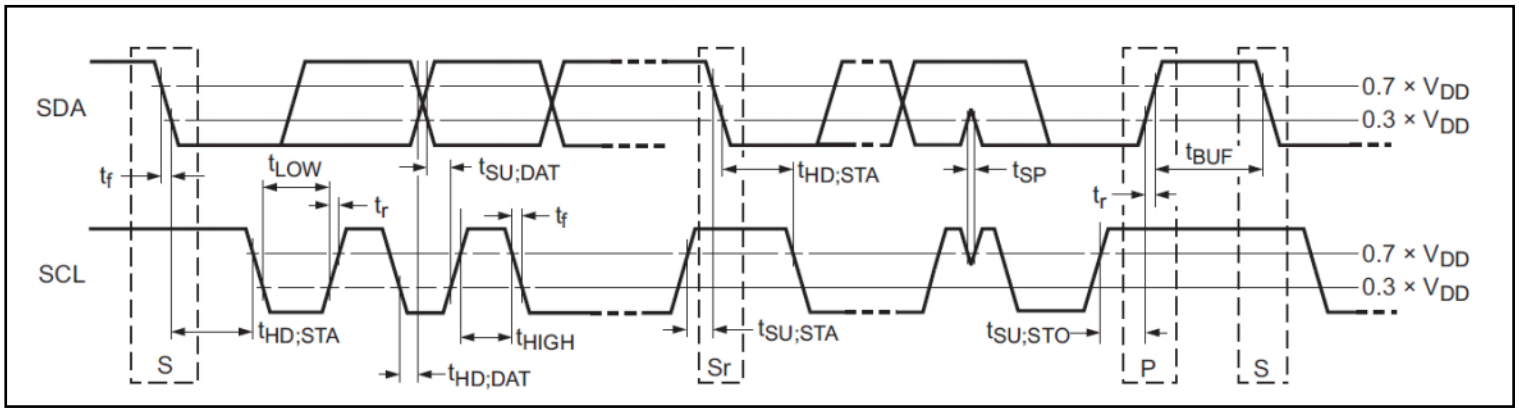


Figure 9. Time Series Chart

Static Characteristics

VCC= 2.8 V to 5.5 V; Tamb= –55 °C to +125 °C;unless otherwise specified.

Symbol	Parameter	State	Minimum	Typicall[1]	Maximum	Unit
Tacc	Temperature Precision	Tamb=-25℃ to+100℃	-1	-	+1	℃
		Tamb=-55℃ to+125℃	-2	-	+2	℃
Tres	Temperature resolution	11-bit digital data	-	0.0825	-	℃
tconv(T)	Temperature change time	Normal mode	-	10	1	ms
Tconv	Switching cycle	Normal mode	-	100	-	ms
IDD(AV)	average supply current	Normal mode:The I²C bus is not activated	-	80	200	μA
		Normal mode:I²C bus activated;fscL=400 kHz	-	-	300	μA
		Sleep Mode		0.2	1.0	μA
VIH	Input high level	Digital pins (SCL,SDA,A2 to A0)	0.7×Vcc		Vcc+0.3	V
VIL	Input low level	Digital Pin	-0.3	-	0.3×Vcc	V
Vi(hys)	Input hysteresis voltage	SCL and SDA pins	-	300		mV
		Pins A2,A1,A0	-	150		mV
IH	High-voltage input current	Digital pin;V_1=Vcc	-1.0	-	+1.0	μA
IL	Low-voltage input current	Digital pin;V_1=0V	-1.0	-	+1.0	μA
VoL	Output low voltage	SDA and OS pins;loL=3 mA	-	-	0.4	V
		loL=4 mA	-	-	0.8	V
ILo	Output leakage current	SDA and OS pins;VoH=Vcc	-	-	10	μA
Nfault	Number of defects	Programmable;Fault count conversion	1	-	6	
Tth(ots)	Overtemperature shutdown threshold	Windows default		80		℃
Thys	Hysteresis temperature point	Windows default	-	75	-	℃
C	Input capacitance	Digital Pin	-	20		pF

Table 10. Static Characteristics

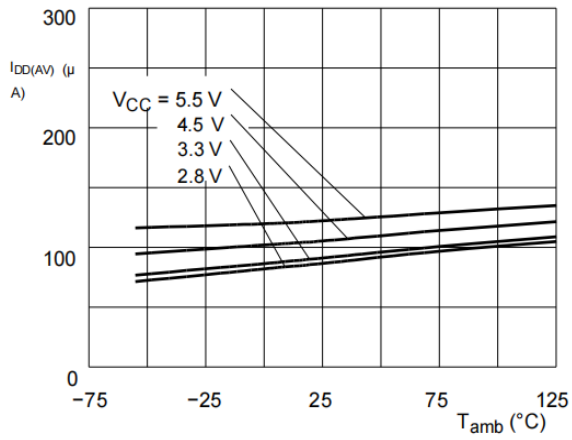


Figure10. Relationship curve between average current and temperature for I 2C in the inactive state

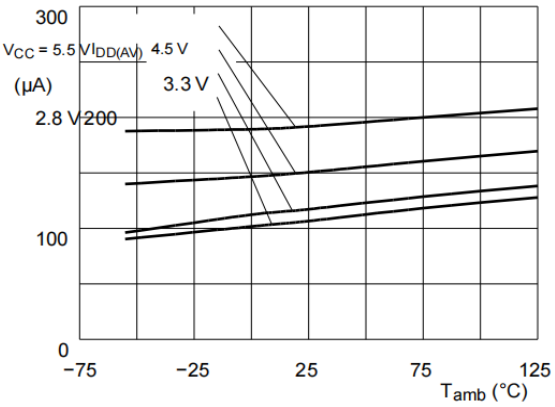


Figure11.The relationship curve between the average current and temperature when ²C is activated

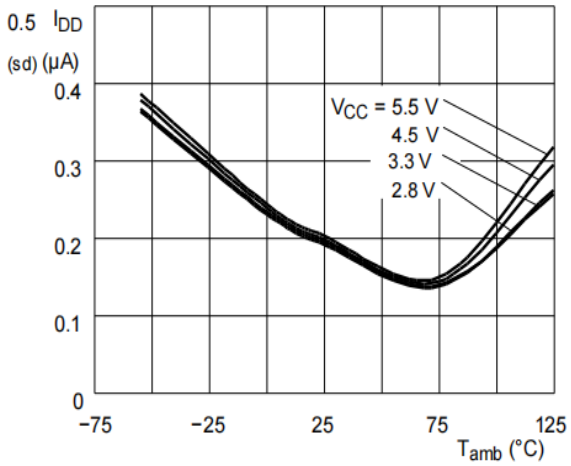


Figure12.Relationship between power supply current and temperature in sleep mode

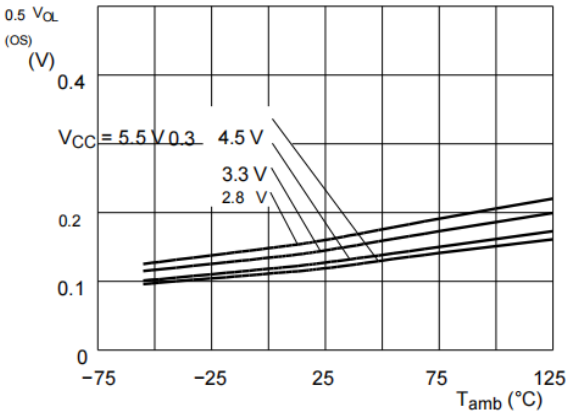


Figure13. Relationship between OS output voltage and temperature at IOL= 4 mA

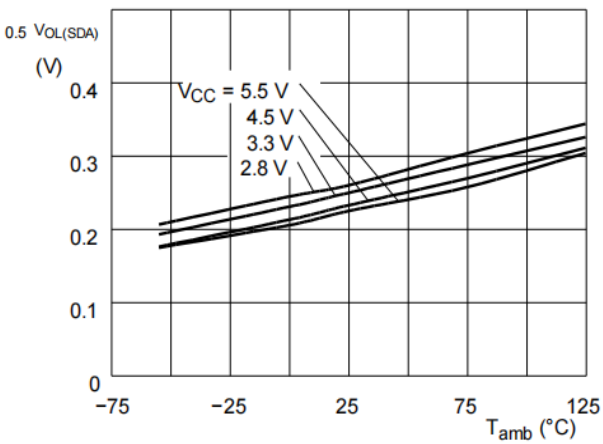


Figure 14. Relationship between SDA voltage and temperature at IOL= 4 mA

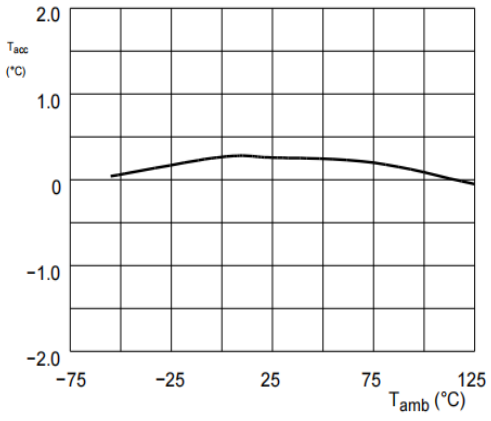
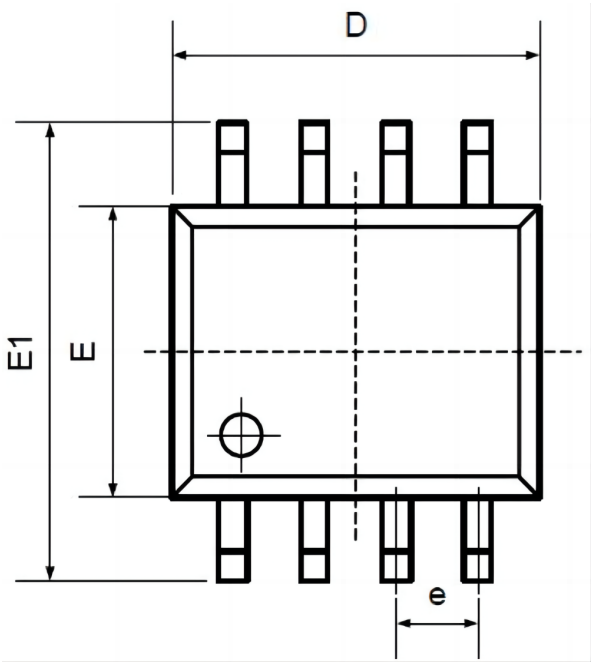


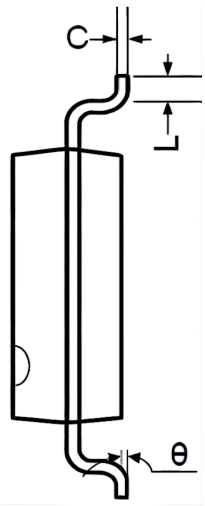
Figure 15. Typical temperature measurement accuracy with VCC= 3.3 V

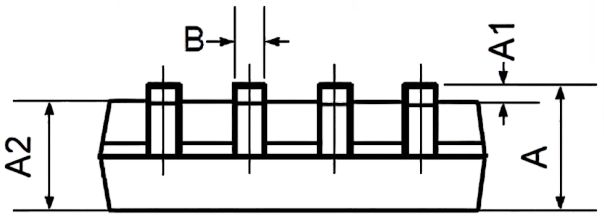
Order information

Order Number	Package	Package Quantity	Marking On The park	Temperature	Operating Voltage
TMP75BQDGKRQ1-TUDI	MSOP8	Tape,Reel,4000	T75BQ	-55℃ to 125℃	1.4V-3.6V
TMP75BQDRQ1-TUDI	SOP8	Tape,Reel,4000	T75BQ		

Package SOP8

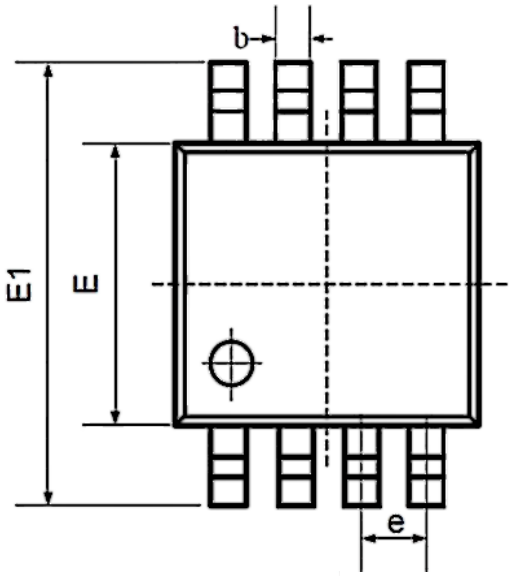


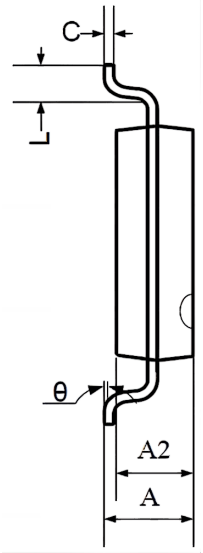


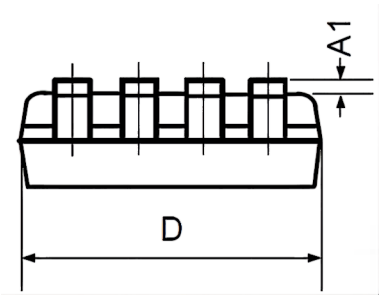


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package MSOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026 TYP	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

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