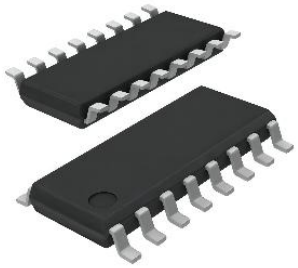
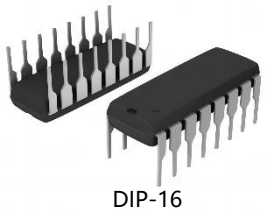
# HX4094-Seight-bitCMOS shift, memorybus register

The HX4094-S is an 8-bit serial shift register, each with a storage latch for strobe data from the serial input to the parallel buffered tristate output, which can be directly connected to the common bus. Data begins to shift at the rising edge of the input clock; When STROBE is high, the data in each shift register is transferred to the storage register; At the same time, when the output-enable signal is high, the data in the storage register will appear at the OUTPUT end. Two series outputs (QS, Q'S) can be used to cascade multiple HX4094 devices, and data can be obtained from the QS serial output at the clock rise edge to allow high-speed operation in cascading systems with fast clock rise times. When the clock of the cascade system rises slowly, the Q'S end can obtain the same serial information on the next clock falling edge. The QS end starts output on the rising edge of the 9th serial clock, and the Q'S end starts output on the falling edge of the 9th serial clock.



SOP-16



DIP-16

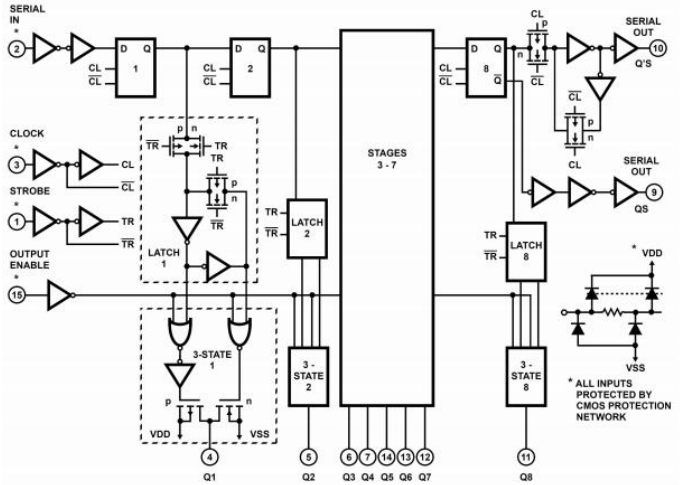
## Main feature

Wide operating voltage：3V to 15V5V，10V,15V Three-speed parameter
Full static operation
Tri-stable output
Standardized symmetrical output characteristics
Anti-jamming performance number：0.45VDD（Typ.）
Input level compatible with TLL
Operating temperature range：-20℃ to +85℃。

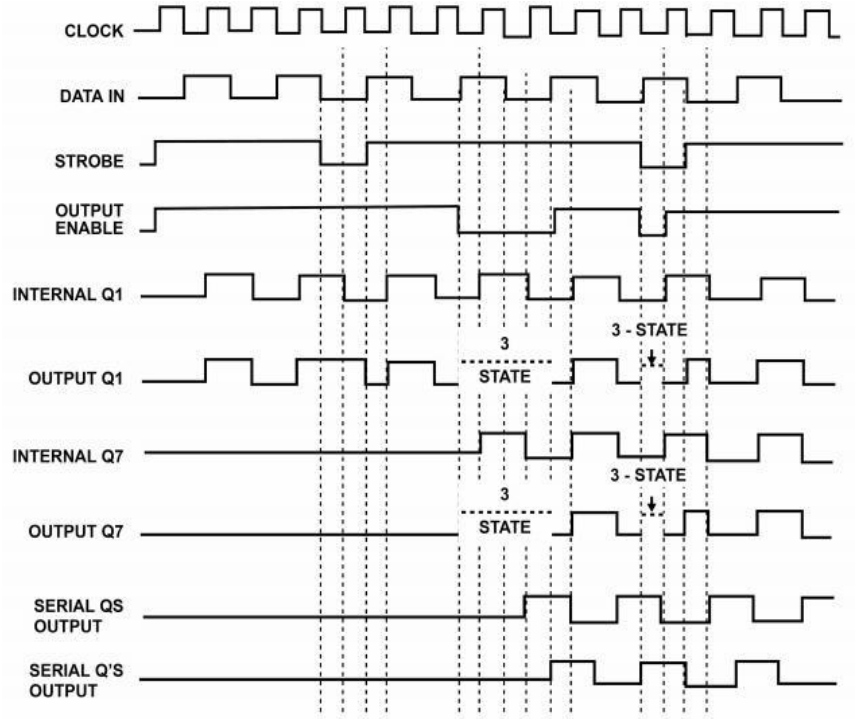
## Main application

Serial-parallel data conversion
Remote control hold register
Two-stage shift, hold and bus application

## Logic block diagram



## Time frame diagram



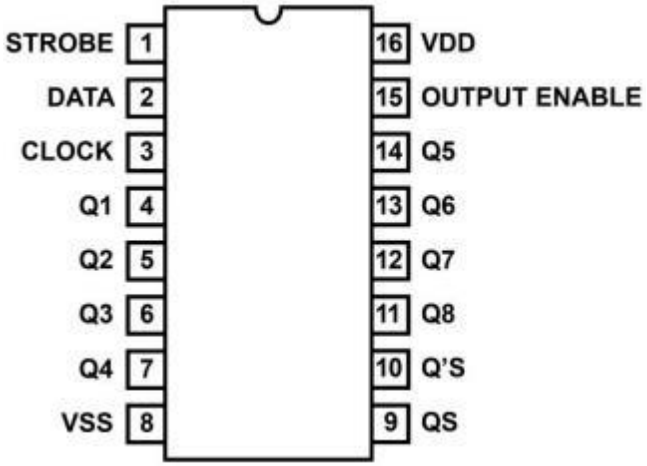

## Truth table

| CLOCK | OUTPUT ENABLE | STROBE | DATA | Parallel output | | Serial output | |
|---|---|---|---|---|---|---|---|
| | | | | Q1 | Qn | QS | Q'S |
| ↑ | L | X | X | OC | OC | Q7 | NC |
| ↓ | L | X | X | OC | OC | NC | Q7 |
| ↑ | H | L | X | NC | NC | Q7 | NC |
| ↑ | H | H | L | L | Qn-1 | Q7 | NC |
| ↑ | H | H | H | H | Qn-1 | Q7 | NC |
| ↓ | H | H | H | NC | NC | NC | Q7 |

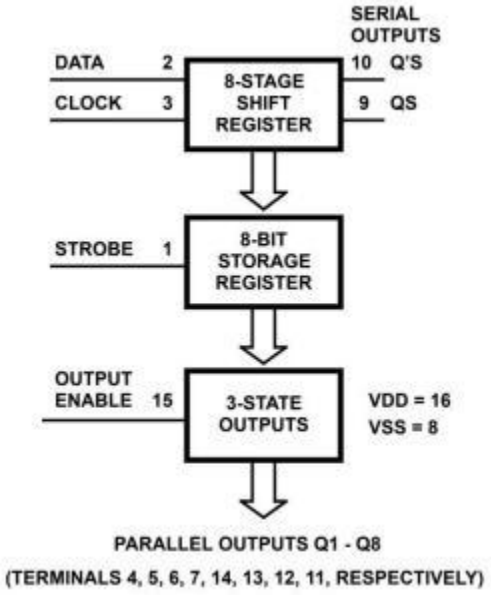
Note: H= high level voltage; L= low level voltage; X= ignore; ↑= Clock rising edge; ↓= falling edge of clock; OC= open circuit, high impedance state; NC= To remain in the same state;

Q7= The information in the 7th-bit shift register is transferred to the 8th-bit register and QS output at the clock rise edge.

## Pin diagram




## Functional block diagram




## Pin specification

| Pin number | Pin name | I/O | Description |
|---|---|---|---|
| 1 | STROBE | I | Latch input. At low voltage, the parallel output is locked |
| 2 | DATA | | Serial data input terminal |
| 3 | CLOCK | | Serial clock input |
| 15 | OUTPUT ENABLE | | Output Enables the input. At low voltage, the parallel output is in a high resistance state |
| 4－7、11-14 | Q1－ Q8 | O | Parallel output |
| 9 | QS | | Serial data output |
| 10 | Q'S | | Serial data output |
| 8 | VSS | GND | Ground (0V) |
| 16 | VDD | P | Supply voltage |

## Limiting parameter (Unless otherwise stated, Tamb=25°C;Voltage is VSS=0V(usually grounded) as reference)

| Argument | Symbol | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | -0.5 | +18 | V |
| Input voltage | $V_I$ | | -0.5 | $V_{DD}$+0.5 | V |
| Input current | $I_{IK}$ | Arbitrary input | - | ±10 | mA |
| Storage temperature | Tstg | | -65 | +150 | ℃ |
| Storage temperature | $T_{amb}$ | | -20 | +85 | ℃ |
| Welding temperature | $T_L$ | Ten seconds | 260 | | ℃ |

## Recommended working conditions

| Argument | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating voltage | $V_{DD}$ | 3 | 15 | V |
| Input voltage | $V_I$ | 0 | $V_{DD}$ | V |
| Ambient temperature | $T_{amb}$ | -20 | +85 | ℃ |

## Electrical characteristic

### Dc parameter (Unless otherwise specified, $T_{amb}$=25℃, $V_{SS}$=0V)

| Argument | Symbol | Test condition | | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| | | $V_O$ | $V_I$ | $V_{DD}$ | | | | |
| Supply current | $I_{DD}$ | - | 0, 5 | 5 | - | - | 1 | uA |
| | | - | 0, 10 | 10 | - | - | 1 | uA |
| | | - | 0, 15 | 15 | - | - | 1 | uA |
| Low level output current | $I_{OL}$ | 0.4 | 0, 5 | 5 | 0.51 | 1 | - | mA |
| | | 0.5 | 0, 10 | 10 | 1.3 | 2.6 | - | mA |
| | | 1.5 | 0, 15 | 15 | 4.5 | 11.5 | - | mA |
| | | 4.6 | 0, 5 | 5 | -0.51 | -1.2 | - | mA |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| High level output current | $I_{OH}$ | 2.5 | 0, 5 | 5 | -1.6 | -3.2 | - | mA |
| | | 9.5 | 0, 10 | 10 | -1.3 | -2.6 | - | mA |
| | | 13.5 | 0, 15 | 15 | -4 | -9.5 | - | mA |
| Low output voltage | $V_{OL}$ | - | 0, 5 | 5 | - | 0 | 0.05 | V |
| | | - | 0, 10 | 10 | - | 0 | 0.05 | V |
| | | - | 0, 15 | 15 | - | 0 | 0.05 | V |
| High level output voltage | $V_{OH}$ | - | 0, 5 | 5 | 4.95 | 5 | - | V |
| | | - | 0, 10 | 10 | 9.95 | 10 | - | V |
| | | - | 0, 15 | 15 | 14.95 | 15 | - | V |
| Low-level input voltage | $V_{IL}$ | 0.5, 4.5 | - | 5 | - | - | 1.5 | V |
| | | 1, 9 | - | 10 | - | - | 3.0 | V |
| | | 1.5, 13.5 | - | 15 | - | - | 4.0 | V |
| High resistance output leakage | $V_{IH}$ | 0.5, 4.5 | - | 5 | 3.5 | | - | V |
| | | 1, 9 | - | 10 | 7.0 | | - | V |
| | | 1.5, 13.5 | - | 15 | 11.0 | | - | V |
| Input leakage | $I_I$ | - | 0, 15 | 15 | - | - | ±1 | uA |
| High resistance output leakage | Ioz | 0, 15 | 0, 15 | 15 | - | - | ±1 | uA |

## Ac parameter (Unless otherwise specified, $T_{amb}$=25℃, $V_{SS}$=0V, $t_r/t_f$=20ns, $C_L$=50pF, $R_L$=1KΩ)

| Argument | Symbol | Test condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Transmission delay time (clock to serial output QS) | $t_{PHL}$, $t_{PLH}$ | See Figure 2 | $V_{DD}$=5V | - | 300 | 600 | ns |
| | | | $V_{DD}$=10V | - | 125 | 250 | ns |
| | | | $V_{DD}$=15V | - | 95 | 190 | ns |
| Transmission delay time (clock to serial output Q'S) | $t_{PHL}$, $t_{PLH}$ | See Figure 2 | $V_{DD}$=5V | - | 230 | 460 | ns |
| | | | $V_{DD}$=10V | - | 110 | 220 | ns |
| | | | $V_{DD}$=15V | - | 75 | 150 | ns |
| Transmission delay time | | See Figure 2 | $V_{DD}$=5V | - | 420 | 840 | ns |
| | | | $V_{DD}$=10V | - | 195 | 390 | ns |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| (Clock to parallel output Qn) | $t_{PHL}$, $t_{PLH}$ | | $V_{DD}$=15V | – | 135 | 270 | ns |
| Transmission delay time (strobe to parallel output Qn) | $t_{PHL}$, $t_{PLH}$ | See Figure 2 | $V_{DD}$=5V | – | 290 | 580 | ns |
| | | | $V_{DD}$=10V | – | 145 | 290 | ns |
| | | | $V_{DD}$=15V | – | 100 | 200 | ns |
| Transmission delay time (high level - high impedance/High impedance - high level) | $t_{PHZ}$, $t_{PZH}$ | Pin15-Qn See Figure 3 | $V_{DD}$=5V | – | 140 | 280 | ns |
| | | | $V_{DD}$=10V | – | 60 | 120 | ns |
| | | | $V_{DD}$=15V | – | 45 | 90 | ns |
| Transmission delay time (low - high impedance/ high impedance - low level) | $t_{PLZ}$, $t_{PZL}$ | Pin15-Qn See Figure 3 | $V_{DD}$=5V | – | 100 | 200 | ns |
| | | | $V_{DD}$=10V | – | 50 | 100 | ns |
| | | | $V_{DD}$=15V | – | 40 | 80 | ns |
| Pulse width (minimum gate pulse) | t | See Figure 2 | $V_{DD}$=5V | – | 100 | 200 | ns |
| | | | $V_{DD}$=10V | – | 40 | 80 | ns |
| | | | $V_{DD}$=15V | – | 35 | 70 | ns |
| Pulse width Width (minimum clock pulse) | t | See Figure 2 | $V_{DD}$=5V | – | 100 | 200 | ns |
| | | | $V_{DD}$=10V | – | 50 | 100 | ns |
| | | | $V_{DD}$=15V | – | 40 | 80 | ns |
| Data creation time (DATA-CLOCK) | $t_{SU}$ | See Figure 2 | $V_{DD}$=5V | – | 60 | 120 | ns |
| | | | $V_{DD}$=10V | – | 30 | 60 | ns |
| | | | $V_{DD}$=15V | – | 20 | 40 | ns |
| Maximum clock pulse rise and fall time | $t_{THL}$, $t_{TLH}$ | – | $V_{DD}$=5V | 15 | – | – | us |
| | | | $V_{DD}$=10V | 5 | – | – | us |
| | | | $V_{DD}$=15V | 5 | – | – | us |
| Maximum clock frequency | fmax | See Figure 2 | $V_{DD}$=5V | 1.25 | 2.5 | – | MHz |
| | | | $V_{DD}$=10V | 2.5 | 5 | – | MHz |
| | | | $V_{DD}$=15V | 3 | 6 | – | MHz |
| Input capacitance | $C_I$ | Arbitrary input | | – | 5 | 7.5 | pF |

## Ac test circuit

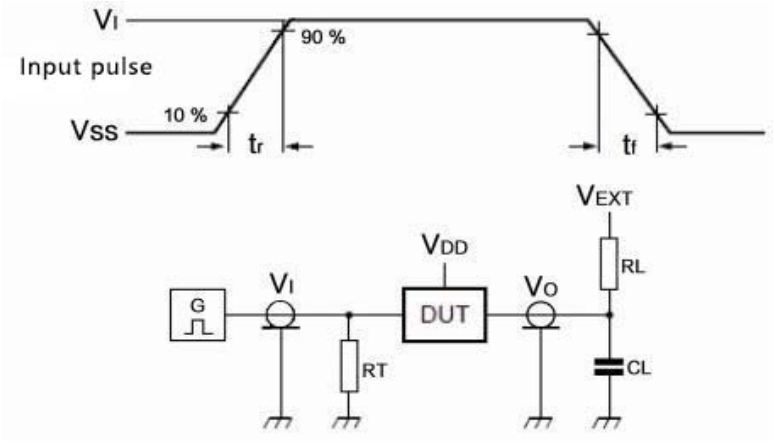



Figure 1:

Note: Equipment under test = equipment under test; CL = Loadad Capacitance; RL = load resistance

$R_T$=The output resistance is equivalent to the output impedance of the pulse generator $Z_o$

| Supply voltage | Input | | Load | |
|---|---|---|---|---|
| $V_{DD}$ | $V_I$ | $t_r$, $t_f$ | CL | RL |
| 5V~15V | $V_{SS}$ or $V_{DD}$ | ≤20ns | 50pF | 1kΩ |

## Ac test waveform

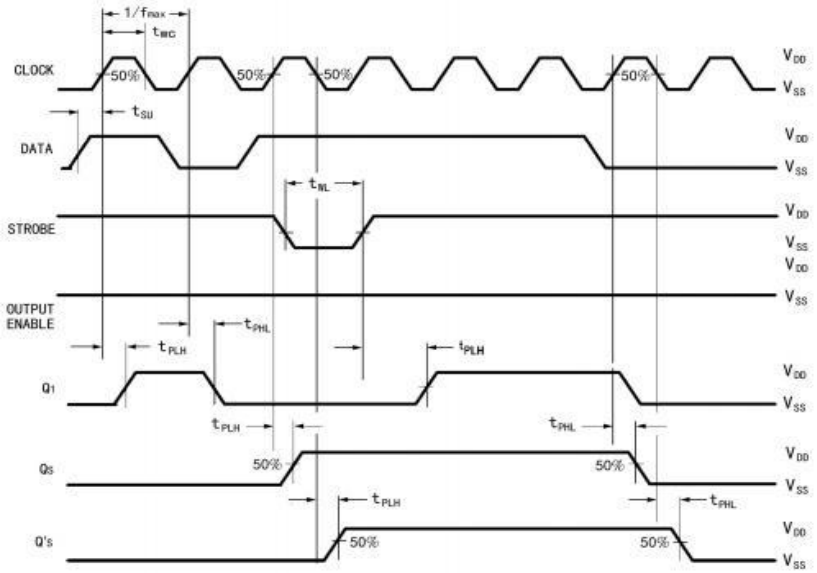



Figure 2: Clock - Output transmission delay, pulse width, maximum frequency

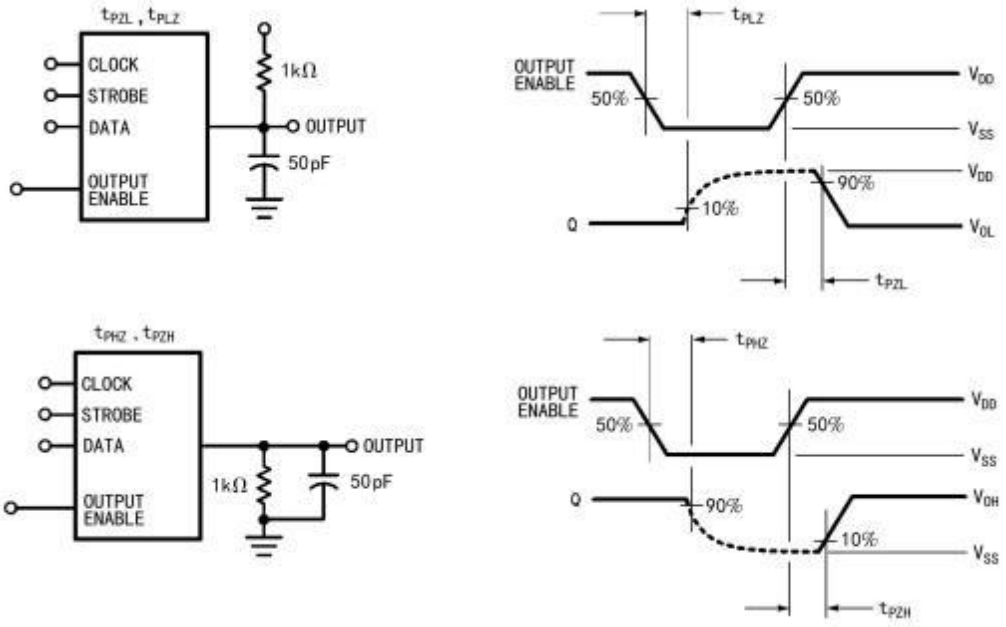



Figure 3: Stored input-output transmission delay

## Apply

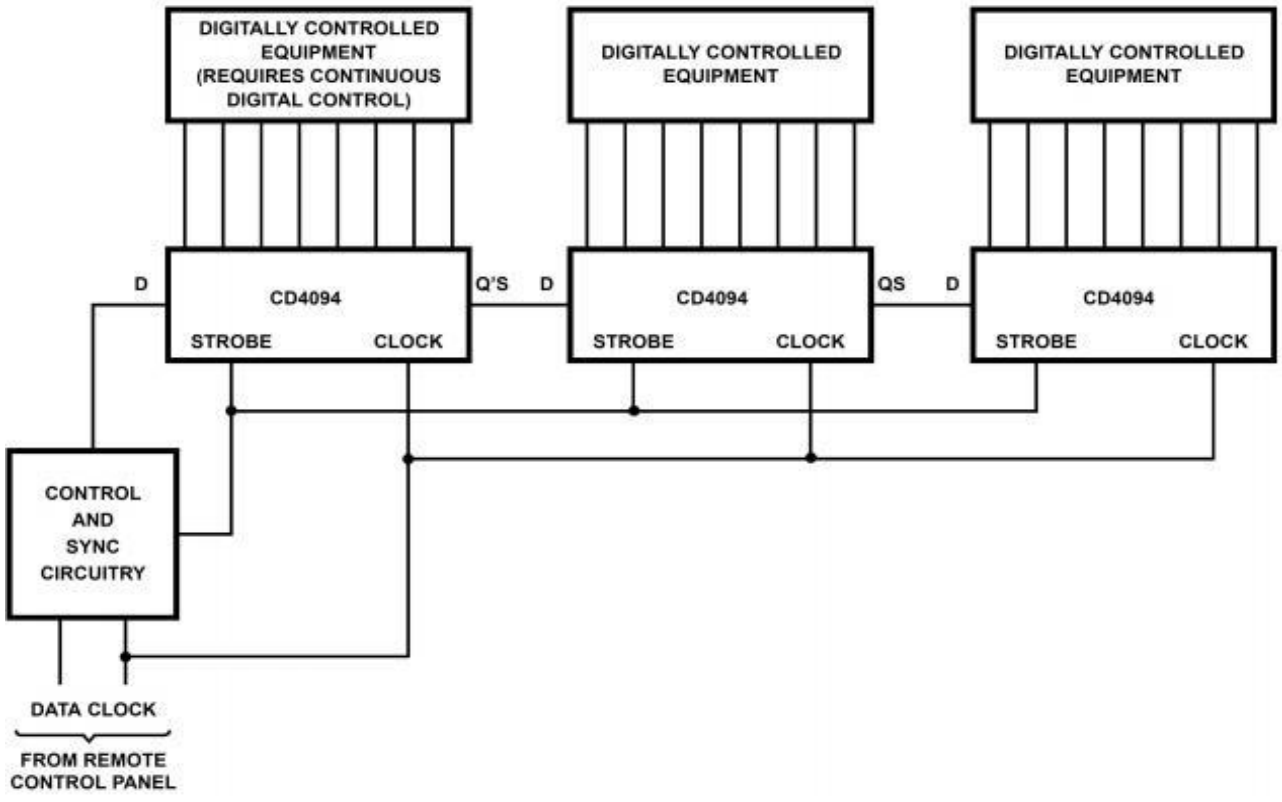
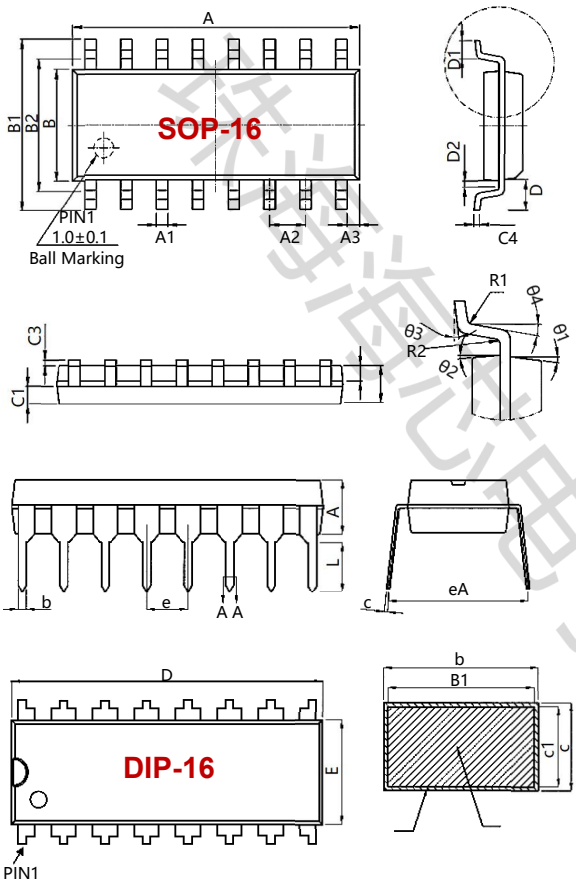



Figure 4: Remote control hold register

## Encapsulation information




| Mark \ Size | Min(mm) | Max(mm) | Mark \ Size | Min(mm) | Max(mm) |
|---|---|---|---|---|---|
| A | 9.80 | 10.00 | C4 | 0.203 | 0.233 |
| Al | 0.356 | 0.456 | D | 1.05TYP | |
| A2 | 1.27TYP | | D1 | 0.40 | 0.70 |
| A3 | 0.302TYP | | D2 | 0.15 | 0.25 |
| B | 3.85 | 3.95 | R1 | 0.20TYP | |
| B1 | 5.84 | 6.24 | R2 | 0.20TYP | |
| B2 | 5.00TYP | | θ1 | 8°~ 12° TYP4 | |
| C | 1.40 | 1.60 | θ2 | 8°~ 12° TYP4 | |
| Cl | 0.61 | 0.71 | θ3 | 0°~ 8° | |
| Cp | 0.54 | 0.64 | θ4 | 4°~12° | |
| C3 | 0.05 | 0.25 | | | |

| Symbol | millimeter | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | 3.20 | 3.30 | 3.40 |
| b | 0.44 | | 0.53 |
| bl | 0.43 | 0.46 | 0.49 |
| C | 0.25 | | 0.30 |
| cl | 0.24 | 0.25 | 0.26 |
| D | 18.95 | 19.05 | 19.15 |
| E | 6.25 | 6.35 | 6.45 |
| e | 2.54BSC | | |
| eA | 8.30 | 8.80 | 9.30 |
| L | 3.00 | | |

| Part Number | Package Type | Package | quantity |
|---|---|---|---|
| HX4094-S | SOP-16 | Taping | 2500 |