60V, 5A Non-Synchronous Step-Down DCDC Converter With High Efficiency Sleep Mode

FEATURES

- Wide Input Range: 4.5V-60V
- Up to 5A Continuous Output Current
- 0.8V ± 1% Feedback Reference Voltage
- Integrated 83mΩ High-Side Power MOSFET
- Adjustable Frequency 100KHz to 2.5MHz
- Synchronizes to external clock
- ±6% Frequency Spread Spectrum (FSS)
- High Efficiency at Light Load With Pulse Skipping Mode (PSM)
- 120uA Quiescent Current in Sleep Mode
- Available in an eSOP-8L Package

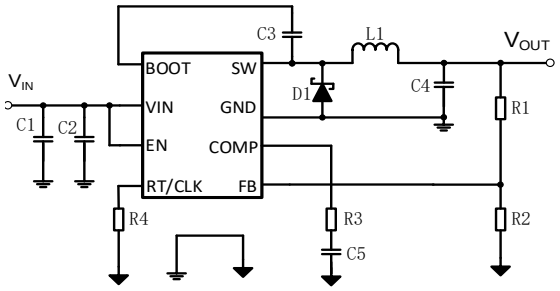
APPLICATIONS

- 12-V, 24-V, 48-V Industry Power System
- Industrial Automation and Motor Control
- Vehicle Accessories
- USB dedicated charging ports and battery chargers

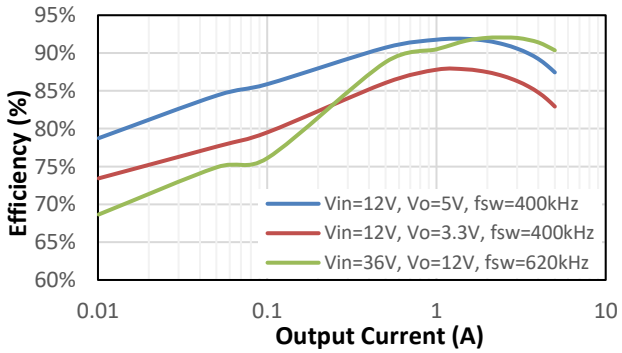
ORDERING INFORMATION

TYPE	MARKING	PACKAGE
TPS54540BDDAR	TPS54540	eSOP-8

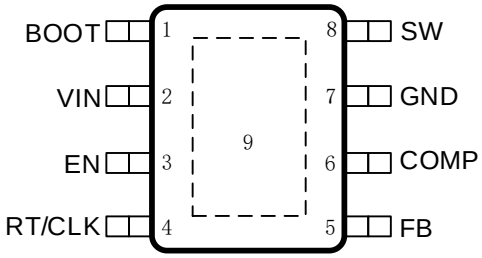
TYPICAL APPLICATION



Simplified Schematic



PIN CONFIGURATION AND FUNCTIONS



Top View: TPS54540BDDAR eSOP-8L

PIN OUT		I/O	PIN FUNCTION
NAME	NO.		
BOOT	1	O	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BOOT pin and SW pin.
VIN	2	I	Power supply input. Must be locally bypassed.
EN	3	I	Enable logic input. Floating the pin enables the device. This pin supports high voltage up to VIN supply. The device has precision enable thresholds 1.21V rising / 1.05V falling for programmable UVLO threshold. The hysteresis is programmable by external resistor network.
RT/CLK	4	I	Resistor timing and external clock synchronization. An internal amplifier holds this terminal at a fixed voltage when using an external resistor to ground to set the switching frequency. If the terminal is pulled above the PLL upper threshold, a mode change occurs and the terminal becomes a synchronization input. The internal amplifier is disabled and the terminal is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the operating mode returns to resistor frequency programming.
FB	5	I	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT node to FB pin and from FB pin to GND to set up output voltage. The device regulates FB to the internal reference of 0.8V typically.
COMP	6	O	Connect RC network to ground to realize the external loop compensation.
GND	7	-	Ground.
SW	8	I	Switching node of the buck converter.
Thermal Pad	9	-	Must be grounded in PCB layout.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted

DESCRIPTION	PARAMETER	MIN	MAX	UNIT
Input Voltage	VIN, EN to GND	-0.3	65	V
	FB to GND	-0.3	6.5	V
	COMP to GND	-0.3	6.5	V
	RT/CLK to GND	-0.3	3.6	V
Output Voltage	SW to GND	-3	65	V
	BOOT to SW	-0.3	6.5	V
Junction temperature	T_J	-40	150	°C
Storage temperature	T_{STG}	-65	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)		±2000	V
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins (1)		±1000	V

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Supply voltage range	4.5	60	V
V_O	Output voltage	0.8	58	V
I_O	Output current	0	5	A
V_{EN}	EN pin voltage	0	60	V
f_{SW}	Switching frequency range at RT mode	100	2500	kHz
T_J	Operating junction temperature	-40	150	°C

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	eSOP-8L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance	42	°C/W
$R_{\theta JC(top)}$	Junction to case (top) thermal resistance	45.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.1	°C/W

ELECTRICAL CHARACTERISTICS

V_{IN}=EN=4.5V~60V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		4.5		60	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising	4.03	4.2 350	4.35	V mV
I_{SHDN}	Shutdown current	EN=0V, No load, 4.5V≤ V_{IN}≤60V		3.8	16.8	uA
I_Q	Quiescent current	EN=floating, No load, No switch, 4.5V≤V_{IN}≤60V, BOOT-SW=5V		120	183	uA
Enable and Feedback						
V_{EN_H}	Enable high threshold		1.16	1.21	1.27	V
V_{EN_L}	Enable low threshold		0.96	1.05	1.10	V
Error Amplifier						
V_{FB}	Voltage reference		0.792	0.8	0.808	V
I_{FB}	Input current			25		nA
g_m	Error amplifier transconductance (gM)	−2μA < I_{COMP} < 2 μA, V_{COMP} = 1 V		240		uA/V
T_{ran}	COMP to SW current transconductance			14		A/V
Timing Resistor and External Clock						
V_{CLK_H} *	RT/CLK High			2.8	3	V
V_{CLK_L} *	RT/CLK Low		0.5	1.6		V
High-side MOSFET						

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
R_{DSON_H}	High side FET on-resistance			83	156	mΩ
Switching Characteristics						
f_{SWRT}	Switching frequency	R_T=200k w/o frequency spread	440	500	560	kHz
	Switching frequency range using RT mode		100		2500	kHz
f_{jitter}	Frequency spread band using RT mode	f_{SW} =500kHz		±6%		
f_{SWSYN}	Switching frequency range using CLK mode		100		2500	kHz
t_{ON_MIN}	Minimum on-time			100		ns
Protection						
I_{LIM_HSD}	HSD peak current limit	All temperatures and V_{IN}=12V	7.3	8	8.7	A
T_{SD}	Thermal shutdown threshold			165		°C
	Hysteresis			40		
Output Voltage Protection						
V_{OVP_H}	Output over voltage protection rising			110		%
V_{OVP_L}	Output over voltage protection falling			105		%
Internal Soft-start time						
T_{ss1}	Soft-start time	f_{SW}=500kHz, 10% to 90%		2.1		ms

*Guaranteed by design

TYPICAL CHARACTERISTICS

V_{IN}=24V, L=6.8uH,T_A= 25°C, unless otherwise noted

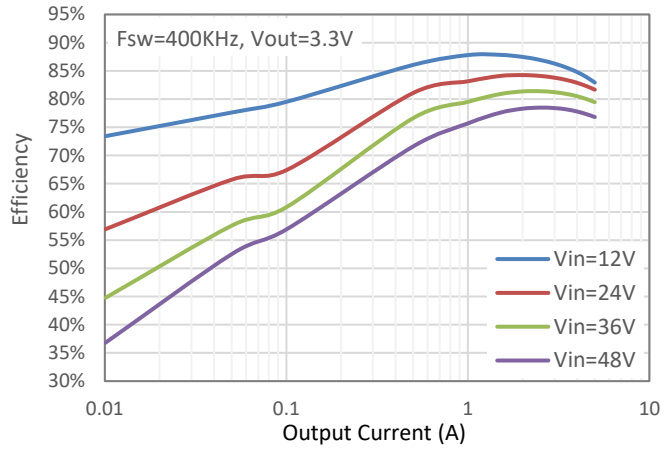


Figure 1. Power Efficiency, Vout=3.3V

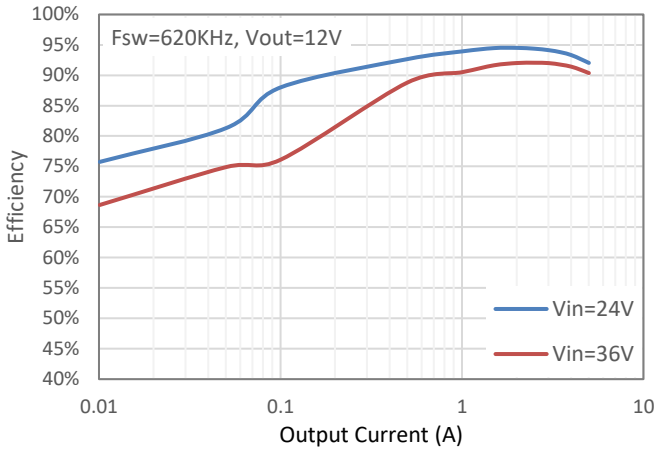


Figure 2. Power Efficiency, Vout=12V

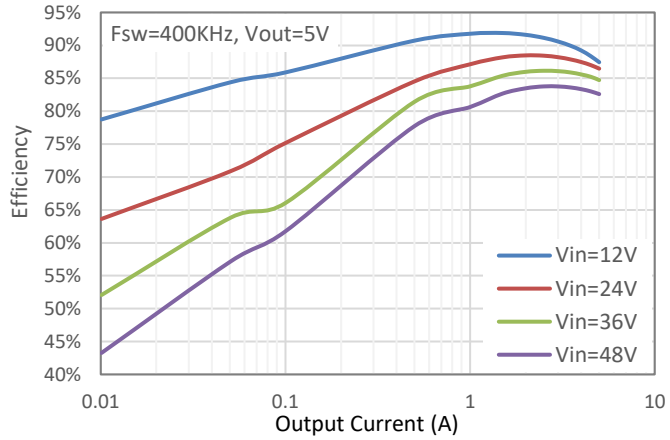


Figure 3. Power Efficiency, Vout=5V

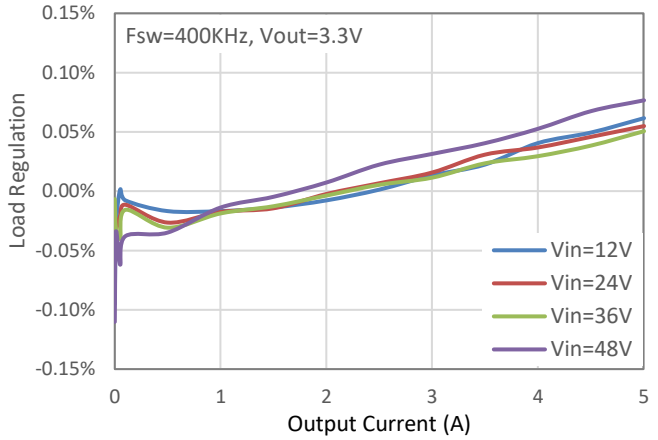


Figure 4. V_{OUT} Vs. Load Regulation

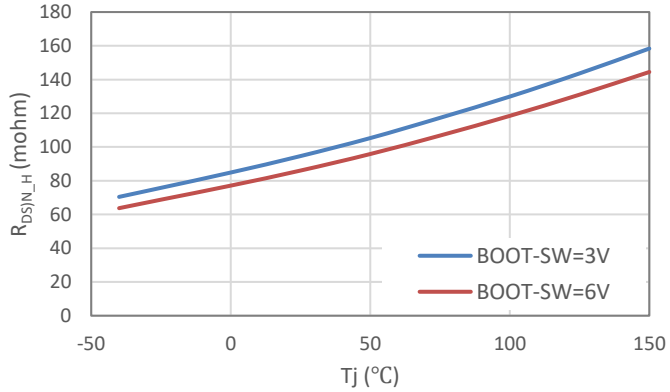


Figure 5. .On Resistance vs Junction Temperature

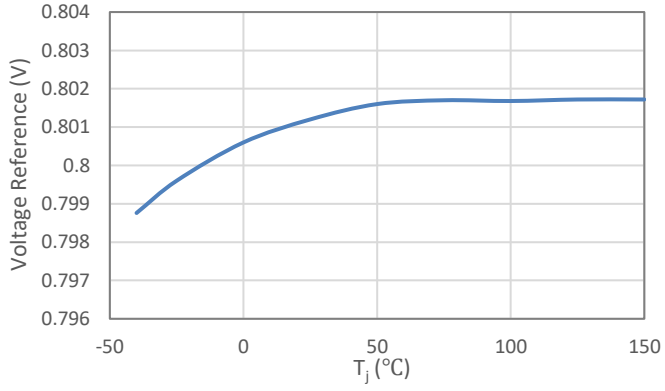


Figure 6. Voltage Reference vs Junction Temperature

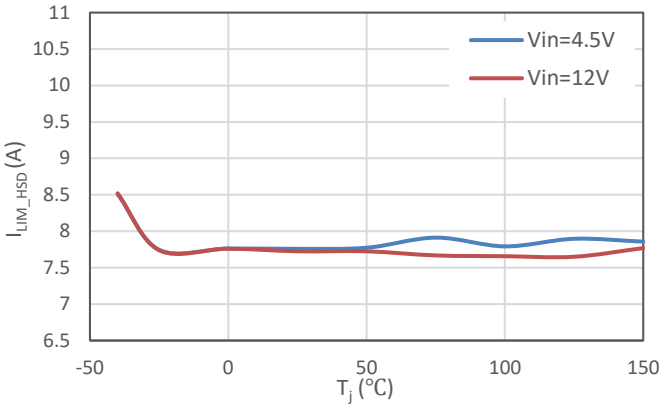


Figure 7. Switch Current Limit vs Junction Temperature

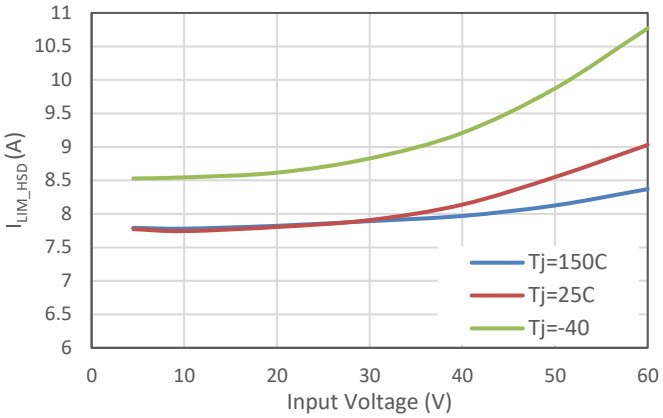


Figure 8. Switch Current Limit vs Input Voltage

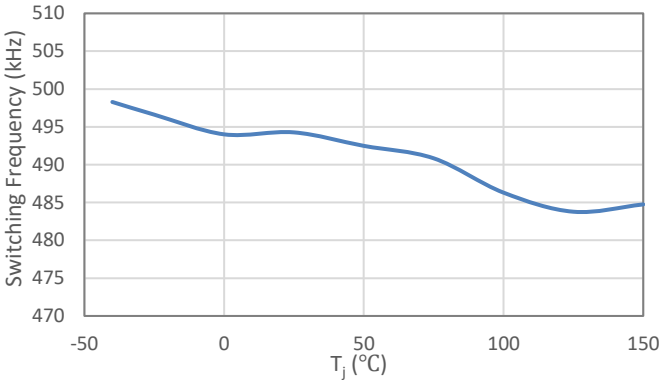


Figure 9. Switching Frequency vs Junction Temperature

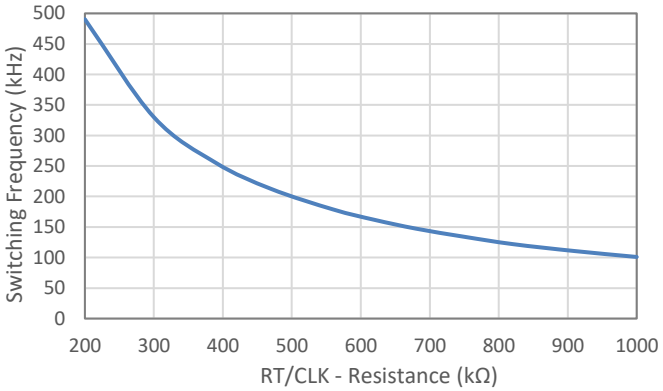


Figure 10. Switching Frequency vs RT/CLK Resistance Low Frequency Range

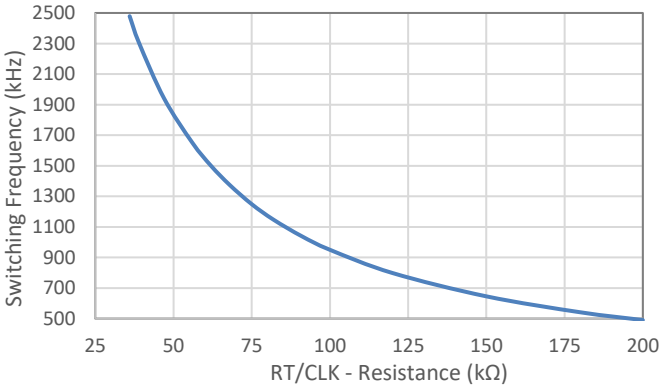


Figure 11. Switching Frequency vs RT/CLK Resistance High Frequency Range

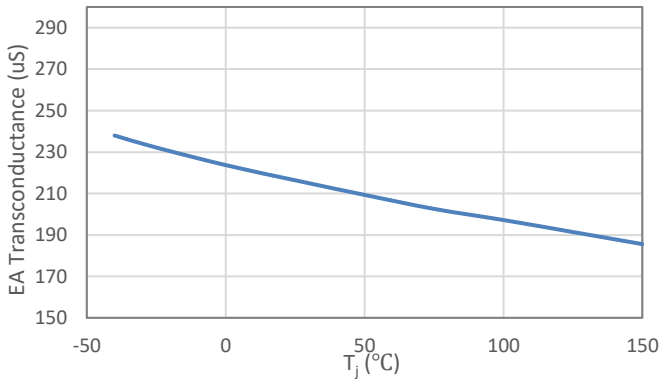


Figure 12. EA Transconductance vs Junction Temperature

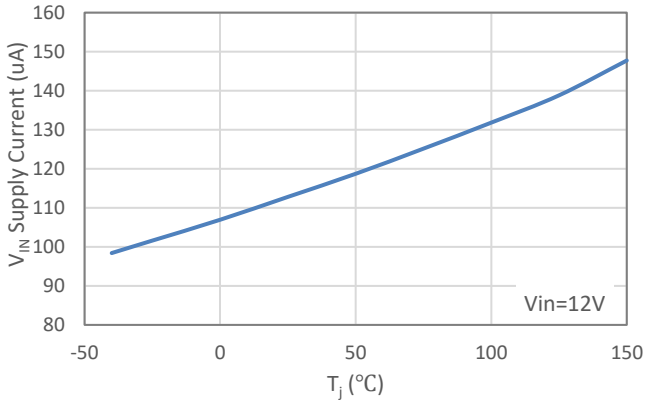


Figure 13. VIN Supply Current vs Junction Temperature

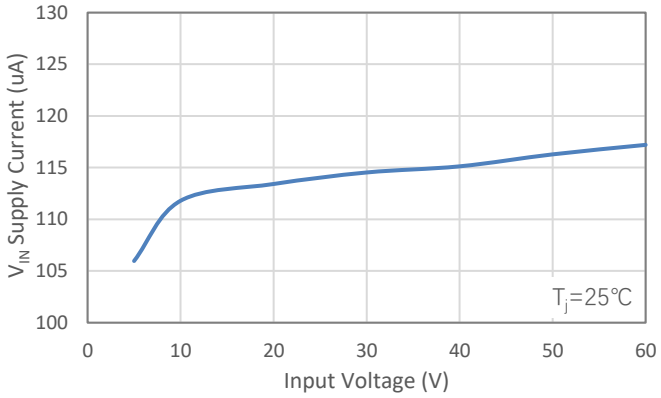


Figure 14. VIN Supply Current vs Input Voltage

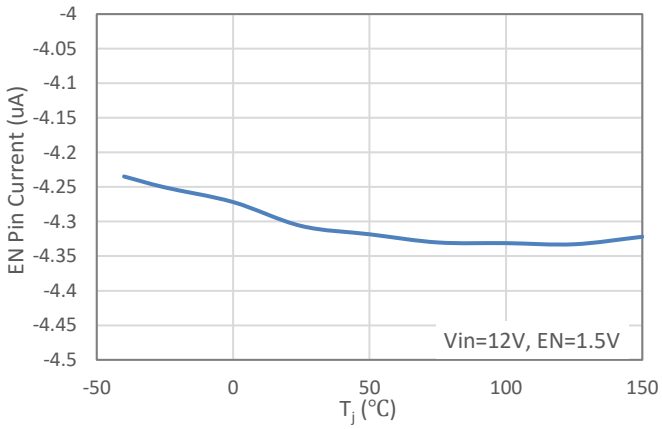


Figure 15. EN Pin Current vs Junction Temperature

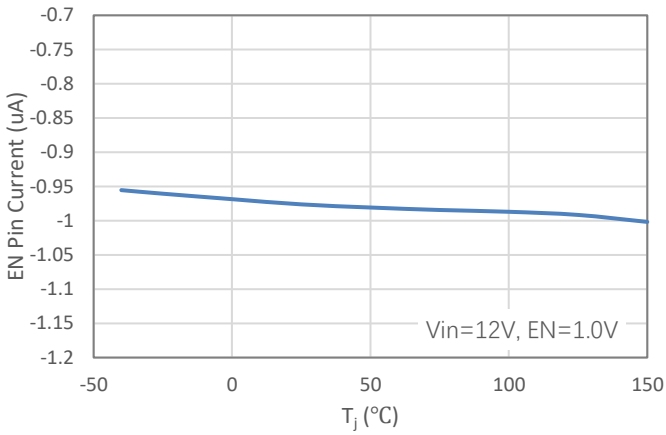


Figure 16. EN Pin Current vs Junction Temperature

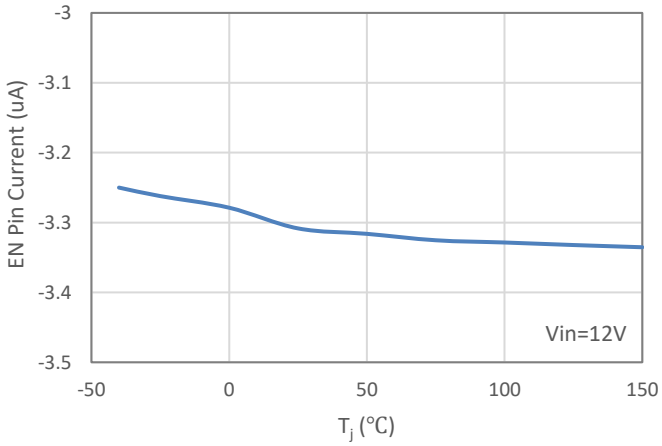


Figure 17. EN Pin Current Hysteresis vs Junction Temperature

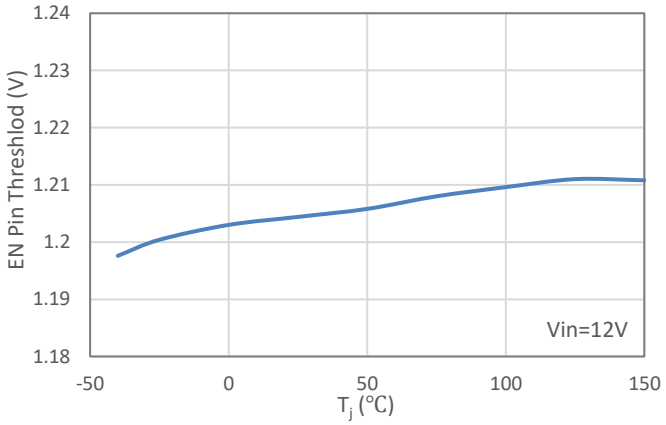


Figure 18. EN Pin Voltage vs Junction Temperature

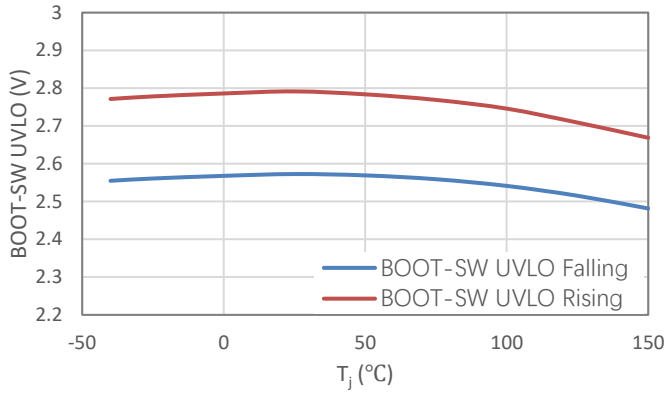


Figure 19. BOOT-SW UVLO vs Junction Temperature

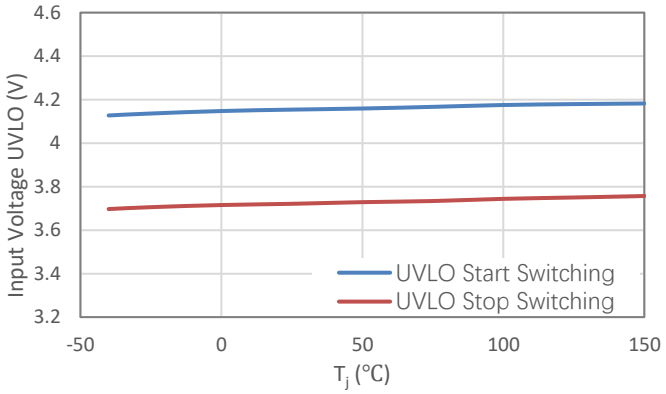


Figure 20. Input Voltage UVLO vs Junction Temperature

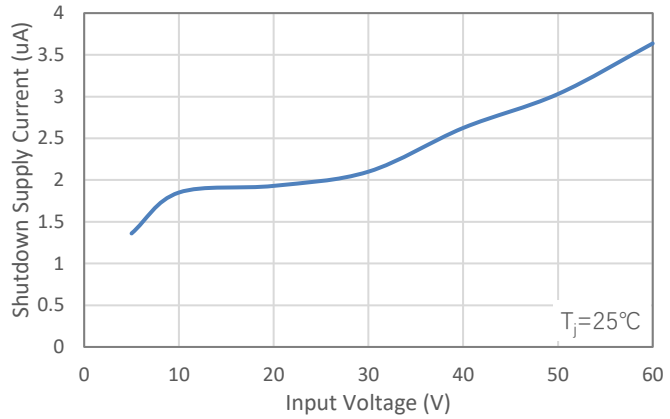


Figure 21. Shutdown Supply Current vs Input Voltage

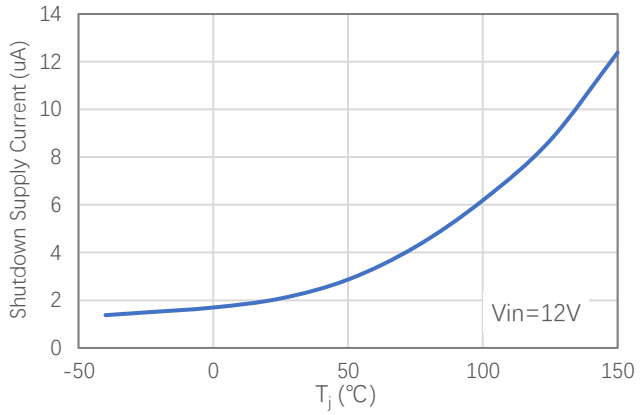


Figure 22. Shutdown Supply Current vs Junction Temperature

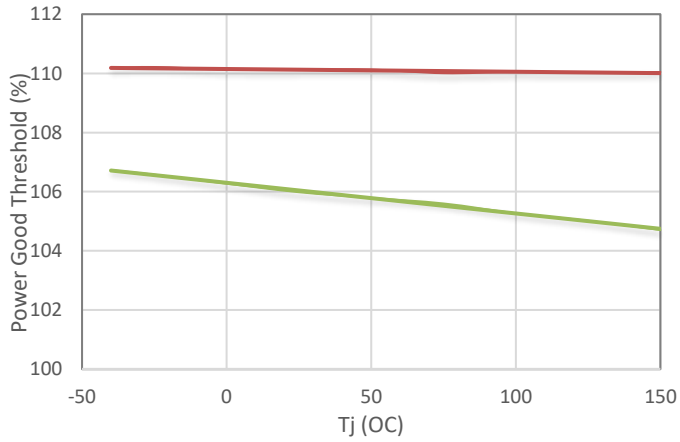


Figure 23. OVP Threshold vs Junction Temperature

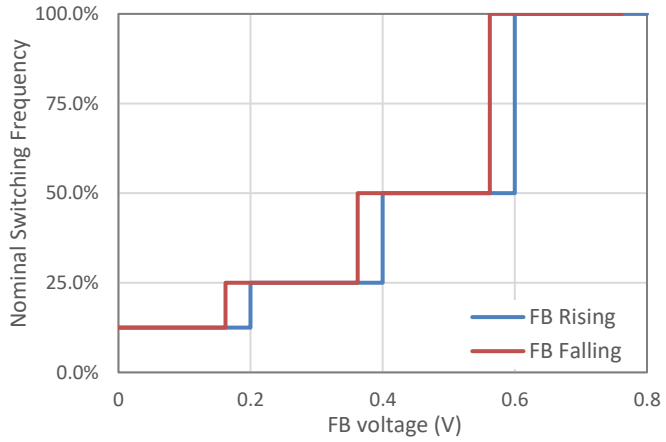


Figure 24. Switching Frequency vs FB voltage

FUNCTION BLOCK DIAGRAM

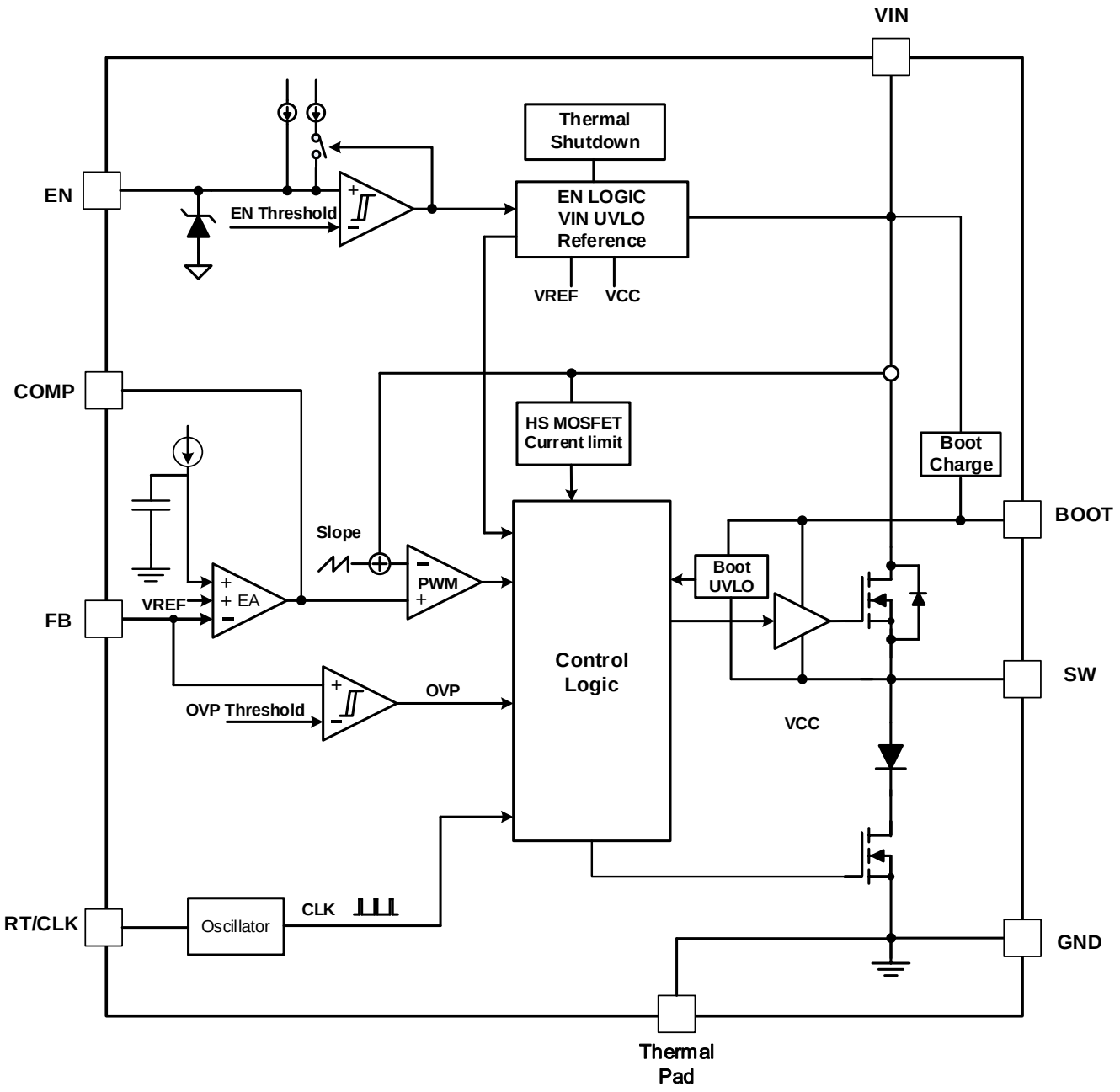


Figure 25 Block Diagram of TPS54540BDDAR

DISCRIPTION

Overview

The TPS54540 is a 60V, 5A buck converter with an integrated 83mΩ high-side MOSFET. With a wide input range from 4.5V to 60V, the device adopts peak current mode and supports a wide adjustable switching frequency range from 100kHz to 2.5MHz setting by external resistor. The switching frequency is adjusted using a resistor to ground connected to the RT/CLK pin. The device has an internal phase-locked loop (PLL) connected to the RT/CLK pin that will synchronize the power switch turn on to a falling edge of an external clock signal.

The quiescent current of this device is 120uA in sleep mode and the shutdown current is 3.8uA. The TPS54540 adopts internal soft-start time, whose typical value is 2.1ms.

The device has a default input start-up voltage of 4.2V with 450mV hysteresis. The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device. Connecting EN pin to VIN directly starts up the device automatically.

The TPS54540 implements the Frequency Spread Spectrum (FSS) modulation spreading of ±6% centered 500kHz switching frequency. FSS improves EMI performance by not allowing emitted energy to stay in any one receiver band for a significant length of time. The converter has optimized gate driver scheme to achieve switching node voltage ringing-free without sacrificing the MOSFET switching time to further damping high frequency radiation EMI noise.

The device integrates protections, like cycle-by-cycle current limit, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device also supports monolithic startup with pre-biased output condition.

It's available in an 8-pin eSOP package.

Peak Current Mode Control

The TPS54540 employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the compensation voltage of the error amplifier' s comp pin, the high-side MOSFET turns off. When the high-side MOSFET turns off, the inductor current discharges through the external diode till the next clock cycle begins.

The integrated error amplifier and the external compensation builds up the feedback loop to regulates the output voltage to the reference. The error amplifier comparing the voltage of the FB pin with an internal

reference voltage of 0.8V. The load current increasement reduces the feedback voltage which is relative to a voltage raise of the error amplifier output till the average inductor current matches the increased load current.

The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

Pulse Skipping Mode (PSM)

The TPS54540 operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. A decrease of the load current leads an increasement in the feedback voltage which yields down the compensation voltage. When the compensation voltage drops to a low clamp threshold, the PSM is triggered. During the skipping period, the discharge of output capacitor leads the output voltage drop which makes the FB voltage decay. Once the FB voltage drops lower than the reference voltage and the compensation voltage rises above the low clamp threshold, the integrated high-side MOSFET turns on in next clock pulse. After several switching cycles with typical 0.35A peak inductor current, the compensation voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded.

This PSM helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. Regarding to improve efficiency further, the quiescent current is 120uA during skipping period with no switching.

VIN Power

The TPS54540 is designed to operate from an input voltage supply range between 4.5V to 60V, at least 0.1uF and 22uF decoupling ceramic cap are recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional 47uF electrolytic bulk capacitor may be required in addition to the local ceramic bypass capacitors.

Under Voltage Lockout Threshold and Enable

The EN pin of TPS54540 is a high voltage pin which can be connected to VIN directly to start-up the device. The TPS54540 is enabled when the EN pin voltage higher than the enable threshold of 1.21V and disabled when the EN pin voltage lower than 1.05V. Due to the internal 1.0uA pull-up current, the device is default enabled when the EN pin floats.

The Under Voltage Lock Out (UVLO) default startup threshold is typical 4.2V with VIN rising and shutdown threshold is 3.75V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin. Connect an external resistor divider (RL and RH) shown in Figure 26 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2

respectively.

$$\mathrm{RH} = \frac{V_{rise} - 1.15 * V_{fall}}{1.15 * 4.0uA - 1.0uA} \quad (1)$$

$$\mathrm{RL} = \frac{1.21\mathrm{V}}{\frac{V_{rise} - 1.21V}{R_H} + 1.0uA} \quad (2)$$

where

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO

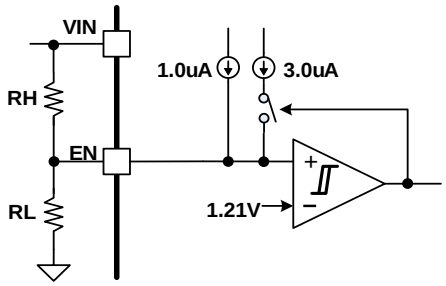


Figure 26 System UVLO by EN divider

Bootstrap Voltage Regulator

An external bootstrap capacitor between BOOT pin and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off.

The floating supply (BOOT to SW) UVLO threshold is 2.75V rising and hysteresis of 200mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.55V, BOOT UVLO occurs.

Output Voltage

The TPS54540 regulates the internal reference voltage at 0.8V with ±1% tolerance over the operating temperature and voltage range.

The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the value is higher, the regulator will be more noise sensitive. R_{FB_BOT} in the range of 10kΩ to 100kΩ is recommended for most application.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{0.8V} - 1\right) * R_{FB\_BOT} \quad (3)$$

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Switching Frequency

The switching frequency of the TPS54540 can be set by placing a resistor between RT/CLK pin and the GND or external clock signal. The RT/CLK pin is not allowed to be left floating or shorted to the GND.

In resistor setting frequency mode (RT mode), use Equation 4. to determine the resistance for a switching frequency needed.

$$RT(K\Omega) = \frac{100000}{fsw(KHz)} \quad (4)$$

where

- fsw is the switching frequency.

The TPS54540 implements the Frequency Spread Spectrum (FSS) function in RT mode, the modulation spreading frequency is±6% of set switching frequency.

The TPS54540 also can synchronize to external clock signal. To implement this synchronization feature connect a square wave to the RT/CLK pin. The square wave applied to the RT/CLK pin must switch lower than 0.5V and higher than 3V and have a pulse width greater than 15ns. The synchronization frequency range is 100kHz to 2500kHz. The external synchronization circuit should be designed such that the default frequency set resistor is connected from the RT/CLK pin to ground when the synchronization signal is off. When using a low impedance signal source, the frequency set resistor is connected in parallel with an ac coupling capacitor to a termination resistor (that is, 50 Ω). When the TPS54540 works in external clock signal mode, the FSS function is automatically disabled while PSM is still active when in light load condition.

Error Amplifier

The TPS54540 voltage-regulation loop is controlled by a transconductance error amplifier. The error amplifier compares the FB pin voltage to the lower of the internal soft-start voltage or the internal 0.8V voltage reference. The transconductance (gm) of the error amplifier is 240μA/V during normal operation.

The frequency compensation components (capacitor, and series resistor) are connected between the error amplifier output COMP pin and GND Pin.

Overcurrent and Short Circuit Protection

The TPS54540 adopts the peak current mode control. In the overcurrent momentum, the output voltage is yield down by heavy load and the error amplifier drives the compensation voltage high to increase the switching current. As the error amplifier output increases, it will be clamped internally, and the high-side current is clamped by a maximum peak current threshold. The peak current threshold is constant over the full duty cycle range.

When the output overcurrent or short circuit occurs, the device will trigger a frequency foldback by dividing the oscillator frequency with a pre-set frequency foldback factor to protect itself by increasing the switching frequency and the off time of high-side MOSFET. This will lead more time for the inductor current to ramp down. Otherwise, a lower switching frequency contributes on lower switching loss and avoiding overheating and other potential damages.

The frequency foldback factor is relative with the FB pin voltage.

Table 1. Frequency Foldback Factor vs V_{FB}

FB pin voltage	Frequency Foldback Factor
75% V_{REF}	2
50% V_{REF}	4
25% V_{REF}	8

Overvoltage Protection

The TPS54540 implements the overvoltage protection (OVP) circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. When the FB pin voltage reaches the rising OVP threshold which is typically 110% of V_{REF}, the high-side MOSFET will be turned off immediately which make the device under OVP. When the FB pin voltage drops below the falling OVP threshold, the high-side MOSFET is turned on and resumed normal operation. The falling OVP threshold is typically 105% of V_{REF}.

Thermal Shutdown

The TPS54540 features an internal thermal shutdown circuit to protect the device from the damage during excessive heat and power dissipation conditions. The thermal shutdown circuit will be asserted when the junction temperature exceeds typically 165ºC. When the junction temperature falls below 125ºC, the device restarts with internal soft start phase.

Loop Compensation

Figure 27 describes a simple small signal model that can be used to design the frequency compensation. The TPS54540 power stage can be approximated by a voltage-controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 5 and consists of a dc gain, one dominant pole, and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage is the power stage transconductance, Tran. The Tran for the TPS54540 is 14A/V. The low- frequency gain of the power stage is

the product of the transconductance and the load resistance as shown in Equation 6. As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with the load may seem problematic at first glance, but fortunately the dominant pole moves with the load current as shown in Equation 7. The combined effect is highlighted by the dashed line in Figure 28. As the load current decreases, the gain increases and the pole frequency decrease, keeping the 0-dB crossover frequency the same with varying load conditions. The type of output capacitor chosen determines whether the ESR zero has a profound effect on the frequency compensation design. Using high ESR aluminum electrolytic capacitors may reduce the number frequency compensation components needed to stabilize the overall loop because the phase margin is increased by the ESR zero of the output capacitor as shown in Equation 8.

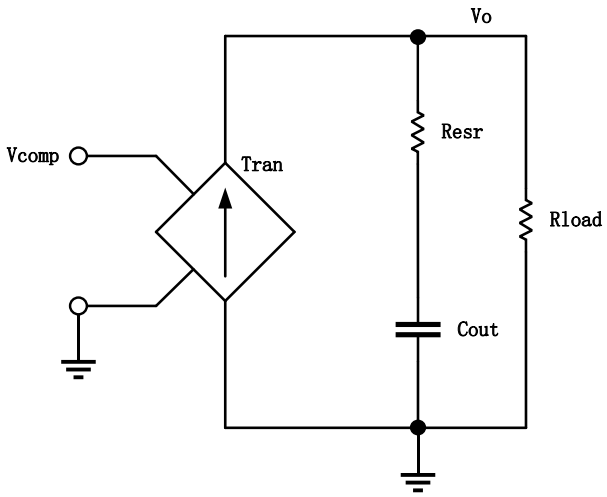


Figure 27. Simple Small Signal Model

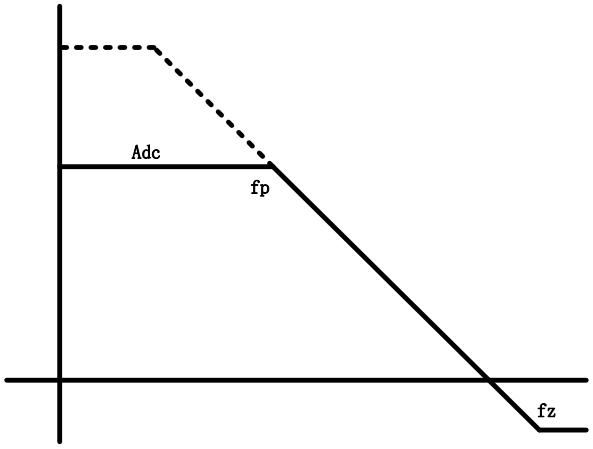


Figure 28. Frequency Response for Peak Current Mode Control

$$\frac{Vout}{Vcomp} = Adc \times \frac{\left(1 + \frac{S}{2\pi \times f_z}\right)}{\left(1 + \frac{S}{2\pi \times f_p}\right)} \quad (5)$$

$$Adc = Tran \times Rload \quad (6)$$

$$f_p = \frac{1}{2\pi \times Cout \times Rload} \quad (7)$$

$$f_z = \frac{1}{2\pi \times Cout \times Resr} \quad (8)$$

The TPS54540 uses a transconductance amplifier for the error amplifier, it can be simply treated as a voltage controlled current source. The compensation circuit of the PCM buck is shown in Figure 29. Equation 9 and Equation 10 relate the frequency response of the amplifier to the small signal model in Figure 30.

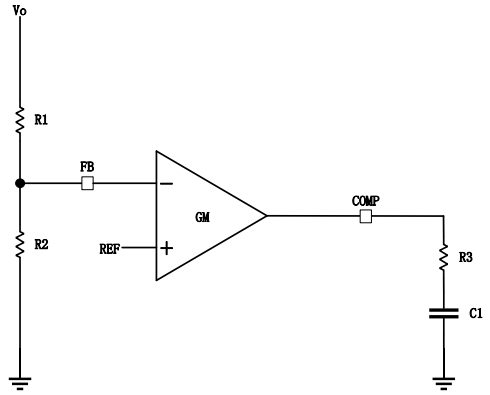


Figure 29. Loop compensation

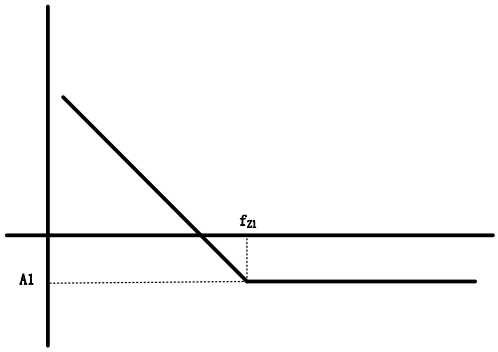


Figure 30. Frequency Response of the loop compensation

$$f(s)_{GM} = g_m \times \frac{(1 + \frac{S}{2\pi \times f_z})}{S} \quad (9)$$

$$f_{z1} = \frac{1}{2\pi \times R3 \times C1} \quad (10)$$

APPLICATION INFORMATION

Typical Application

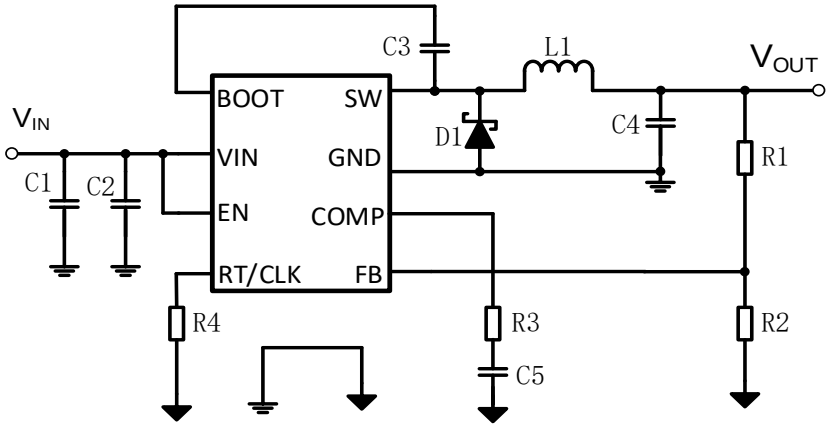


Figure 31. 24V INPUT, 5V 5A OUTPUT

Table 2. Design Parameters

Design Parameters	Example Value
Input Voltage	24V typical, 20~28V
Output Voltage	5V
Output Current	5A
Output voltage ripple (peak to peak)	<50mV
Overshoot/Undershoot range (1.25~3.75A)	5%
Input Voltage ripple (peak to peak)	<400mV
Switching Frequency	300kHz

Set Output Voltage

The TPS54540 output voltage can be easily set up using a resistor divider network R1 and R2 as shown in the typical application circuit Figure 31. Use Equation 11 to calculate the resistor divider values.

$$R1 = \frac{(V_{OUT} - 0.8V) \times R2}{0.8V} \quad (11)$$

In this design example the Vout is 5V. Set the resistor R2 value to be approximately 10k.

$$R1 = \frac{(V_{OUT} - 0.8V) \times R2}{0.8V} = \frac{(5V - 0.8V) \times 10k\Omega}{0.8V} = 52.5k\Omega \quad (12)$$

In this design, use two resistor serial to get the calculated value: 51kΩ and 1.5kΩ for example

Set Switching Frequency

The TPS54540 switching frequency is able to be set-up by placing a local resistor from RT/CLK pin to GND. Use following equation to calculate the resistor value.

$$R4(K\Omega) = \frac{100000}{fsw(KHz)} = \frac{100000}{300kHz} \approx 330k \quad (13)$$

For 300kHz switching frequency, the R4 is 330kΩ.

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. The high voltage rating X7R ceramic capacitors 2.2uF to 10μF are recommended for the decoupling capacitor and a 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin. These capacitors must be rated for 50V or above.

For this design, three 4.7uF X7R capacitors and one 0.1uF capacitor rated 50V is recommended.

The input voltage ripple can be calculated by using Equation 14 to calculate the input voltage ripple:

$$\Delta V_{IN} = \frac{I_{OUT}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) = \frac{5A}{14.1uF \times 300kHz} \times \frac{5V}{24V} \times \left(1 - \frac{5V}{24V}\right) = 194\,mV \quad (14)$$

Where:

- C_{IN} is the input capacitor value
- f_{sw} is the converter switching frequency
- I_{OUT} is the maximum load current

Inductor Selection

The performance of inductor affects the power supply' s steady state operation, transient behavior, loop stability, and buck converter efficiency. The critical parameters of inductor is the inductance, the DC resistance (DCR), the saturation current and the RMS current.

Use following equation to calculate the minimum inductance:

$$L_{MIN} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times K_{IND} \times I_{OUT} \times f_{SW}} \quad (15)$$

Where

- V_{OUT} is output voltage
- K_{IND} is the Ripple Ration of the inductor ripple current ($\Delta iL/I_{OUT}$), 0.4 is recommended here
- V_{INMAX} is the maximum input voltage
- f_{SW} is the converter switching frequency
- I_{OUT} is the output current

In this design example:

$$L > L_{MIN} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times K_{IND} \times I_{OUT} \times f_{SW}} = \frac{5V \times (28V - 5V)}{28V \times 0.4 \times 5A \times 300kHz} = 6.85uH \quad (16)$$

Generally, the Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current larger than its RMS current and saturation current larger than short circuit current I_{LIM_HSD} during the operation. The peak switching current of inductor is calculated in equation 17:

$$I_{LPEAK} = I_{OUT} + K_{IND} \times \frac{I_{OUT}}{2} = 5A + 0.4 \times \frac{5A}{2} = 6A \quad (17)$$

With a minimum inductance of 6.85uH and the saturation current of 8A, the inductor of 10uH inductance, >8A saturation current is selected here.

Output Capacitor

The output capacitor must be chosen carefully with the reason that this capacitor value determines the regulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. Generally, choose a low-ESR output capacitor like a ceramic capacitor from X5R or X7R family to get small output voltage ripple.

From the required output voltage ripple (<50mV), use the Equation 18 to calculate the minimum required effective capacitance, C_{OUT}.

$$C_{OUT} > \frac{\Delta I_{LPP}}{8 \times V_{OUT\_Ripple} \times f_{SW}} = \frac{K_{IND} \times I_{OUT}}{8 \times V_{OUT\_Ripple} \times f_{SW}} \quad (18)$$

The allowed maximum ESR of the output capacitor is calculated by the equation 19.

$$R_{ESR} < \frac{V_{OUT\_Ripple}}{k_{IND} \times I_{OUT}} \quad (19)$$

Where

- V_{OUT_Ripple} is output voltage ripple caused by charging and discharging of the output capacitor.
- k_{IND} is the Ripple Ration of the inductor ripple current ($\Delta iL/I_{OUT}$), 0.4 is recommended here
- I_{OUT} is the maximum output current
- f_{SW} is the converter switching frequency.

In this design, V_{OUT_Ripple} is smaller than 50mV, f_{SW} is 300kHz, I_{OUT} is 5A and K_{IND} is 0.4:

$$C_{OUT} > \frac{0.4 \times 5A}{8 \times 50mV \times 300kHz} = 16.7uF \quad (20)$$

$$R_{ESR} < \frac{50mV}{0.4 \times 5A} = 25m\Omega \quad (21)$$

In buck converter, higher capacitor values can be used to improve the load transient response. Normally the converter control loop needs to take some switching clock cycles to respond to the output voltage changes. The output capacitors must be relatively large enough to charge or discharge current to maintain the output voltage within the specified range in 2 clock cycles. The following two Equations are used to calculate the minimum capacitance to keep the undershoot and overshoot voltages within a specified range.

$$C_{OUT} > \frac{2 \times (I_{TOH} - I_{TOL})}{f_{SW} \times V_{OUS}} \quad (22)$$

$$C_{OUT} > \frac{I_{TOH}^2 - I_{TOL}^2}{(V_{OUT} + V_{OOS})^2 - V_{OUT}^2} \times L \quad (23)$$

Where

- I_{TOH} is the high level of output current during load transient
- I_{TOL} is the low level of output current during load transient
- V_{OUS} is the undershoot voltage
- V_{OOS} is the overshoot voltage
- L is the inductance of inductor in design
- f_{SW} is the converter switching frequency.

For this design example:

$$C_{OUT} > \frac{2 \times (I_{TOH} - I_{TOL})}{f_{SW} \times V_{OUS}} = \frac{2 \times (3.75A - 1.25A)}{300kHz \times 250mV} = 66.7uF \quad (24)$$

$$C_{OUT} > \frac{3.75A^2 - 1.25A^2}{(5V + 250mV)^2 - 5V^2} \times 10uH = 48.5uF \quad (25)$$

Therefore, X7R capacitors of 3x47uF with 16V DC rating and 2mΩ ESR is selected, the derated capacitance is 110 µF, well above the minimum required capacitance of 66.7 µF.

Catch Diode

The TPS54540 requires an external catch diode between the SW pin and GND. The critical parameters of this catch diode are the reverse voltage, the peak current, the forward voltage and the junction capacitance. Generally, the reverse voltage rating equal to or greater than the maximum input voltage. The peak current must be greater than the maximum inductor current. Lower forward voltage and smaller junction capacitance yields higher efficiency and lower power dissipation. The Schottky diodes are typically good choose as the catch diode.

In this design example, the PDS760 is selected with 60V reverse voltage, 7A average current, 0.56V forwards voltage and 200pF junction capacitance.

The power dissipation is calculated as in following equation

$$P_{DMAX} = \frac{(V_{INMAX} - V_{OUT}) \times I_{OUT} \times V_{fd}}{V_{INMAX}} + \frac{C_j \times f_{SW} \times (V_{INMAX} + V_{fd})^2}{2} \quad (26)$$

Where

- V_{INMAX} is the maximum input voltage
- I_{OUT} is the output current
- V_{OUT} is the output voltage
- f_{SW} is the switching frequency
- V_{fd} is the forward voltage

In this design example:

$$P_{DMAX} = \frac{(28V - 5V) \times 5A \times 0.56V}{28V} + \frac{200pF \times 300kHz \times (28V + 0.56V)^2}{2} = 2.32\ W$$

Bootstrap Capacitor

For proper operation of the device, a 0.1uF ceramic capacitor of X5R or X7R must be placed between the SW pin to the BOOT pin. The DC rating of this capacitor is must be 10V or higher voltage level.

Compensation

There are several methods to design compensation for DC/DC regulators. The method presented here is easy to calculate and ignores the effects of the slope compensation that is internal to the device. Because the slope compensation is ignored, the actual crossover frequency is lower than the crossover frequency used in the calculations. This method assumes the crossover frequency is between the modulator pole and the ESR zero and the ESR zero is at least 10 times greater the modulator pole.

To get started, the modulator pole, f_p, and the ESR zero, f_z must be calculated using Equation 27 and Equation 28. Use Equation 29 and Equation 30 to estimate a starting point for the crossover frequency, f_{co}. For the example design, f_p is 1447Hz and f_z is 2067kHz. Equation 30 is the geometric mean of the modulator pole and the ESR zero and Equation 31 is the mean of modulator pole and half of the switching frequency. Equation 29 yields 54kHz and Equation 30 gives 14.7kHz. Use the geometric mean value of Equation 29 and Equation 30 for an initial crossover frequency f_{co}.

Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero.

$$f_p = \frac{I_{OUT}}{2 \times \pi \times V_{OUT} \times C_{OUT}} = \frac{5A}{2 \times \pi \times 5V \times 110uF} = 1447Hz \quad (27)$$

$$f_z = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} = \frac{1}{2 \times \pi \times 0.7m\Omega \times 110uF} = 2067kHz \quad (28)$$

$$f_{co1} = \sqrt{f_p \times f_z} = \sqrt{1447Hz \times 2067kHz} = 54kHz \quad (29)$$

$$f_{co2} = \sqrt{f_p \times \frac{f_{sw}}{2}} = \sqrt{1447Hz \times \frac{300kHz}{2}} = 14.7kHz \quad (30)$$

$$f_{co} = \sqrt{f_{co1} \times f_{co2}} = \sqrt{54kHz \times 14.7kHz} = 28.4kHz \quad (31)$$

To determine the compensation resistor, R3, use Equation 32. Assume the power stage transconductance, T_{ran}, is 14A/V. The output voltage, V_O, reference voltage, V_{REF}, and amplifier transconductance, g_m, are 5 V, 0.8 V, and 240μA/V, respectively. R3 is calculated to be 36.49kΩ, and a standard value of 35kΩ is selected. Use Equation 33 to set the compensation zero to the modulator pole frequency. Equation 33 yields 5.6nF for compensating capacitor C5.

$$R3 = \frac{2 \times \pi \times f_{co} \times C_{OUT}}{T_{ran}} \times \frac{V_{OUT}}{V_{ref} \times g_m} = \frac{2 \times \pi \times 28.4kHz \times 110uF \times 5V}{14S \times 0.8V \times 240uS} = 36.49k\Omega \quad (32)$$

$$C5 = \frac{1}{2 \times \pi \times R3 \times f_p} = \frac{1}{2 \times \pi \times 36k\Omega \times 1447Hz} \approx 3.1nF \quad (33)$$

Application Curves

Figure 32 through Figure 46 apply to the circuit of Figure 31. V_{IN} = 24 V, T_A = 25°C unless otherwise specified

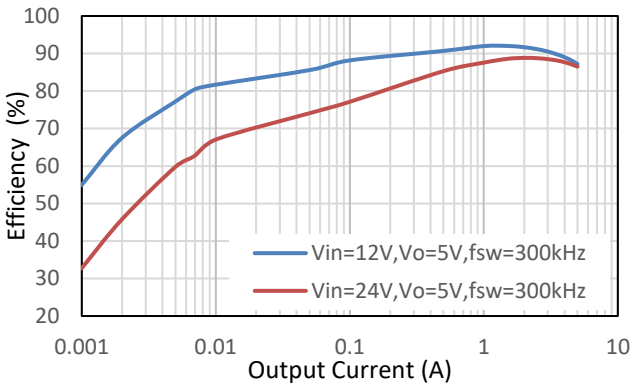


Figure 32. Power Efficiency

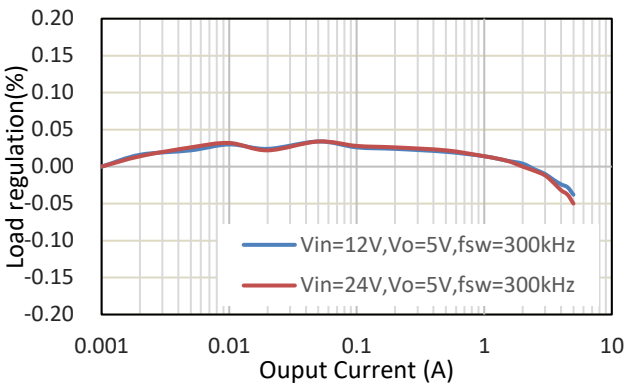


Figure 33. V_{OUT} Vs. Load Regulation

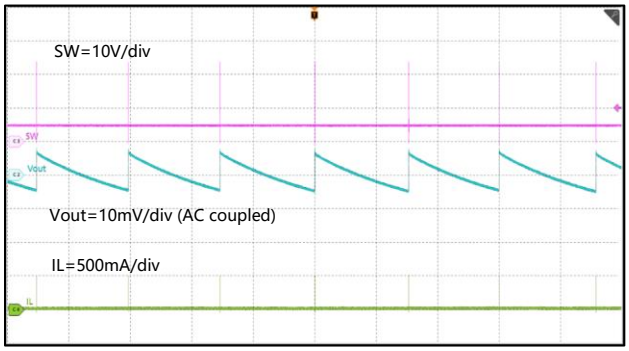


Figure 34. Output Voltage Ripple, I_{OUT}=0A

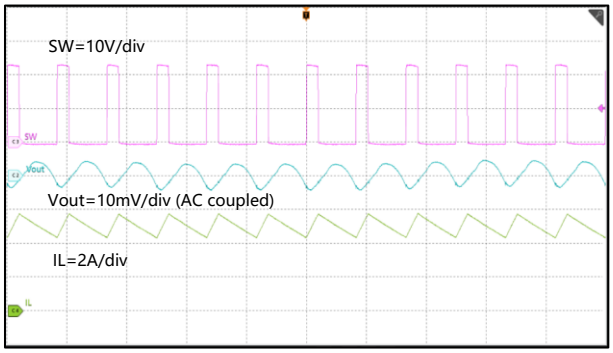


Figure 35. Output Voltage Ripple, I_{OUT}=5A

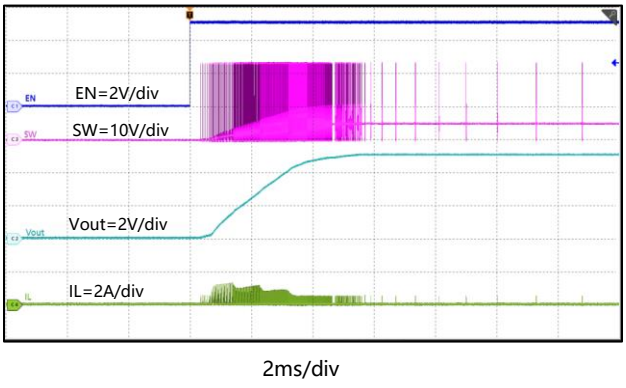


Figure 36. Start-Up with EN, I_{OUT}=0A

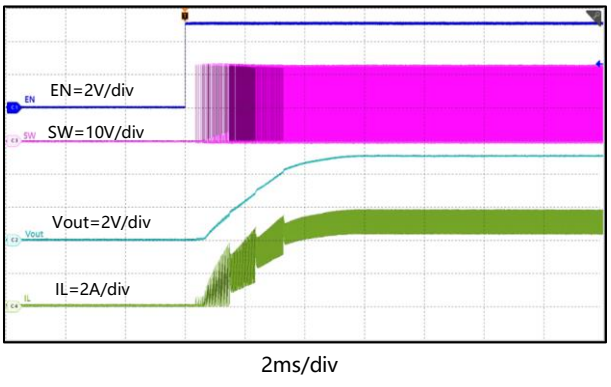


Figure 37. Start-Up with EN, I_{OUT}=5A

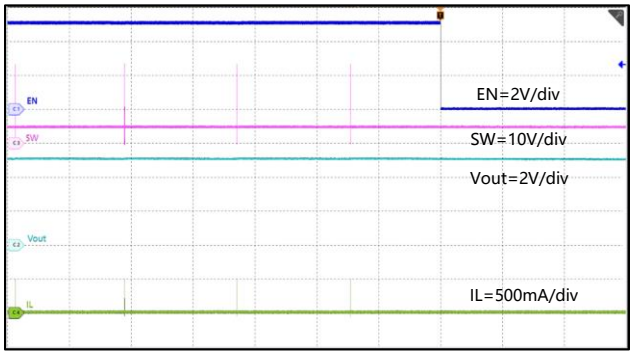


Figure 38. Shut-down with EN, I_{OUT}=0A

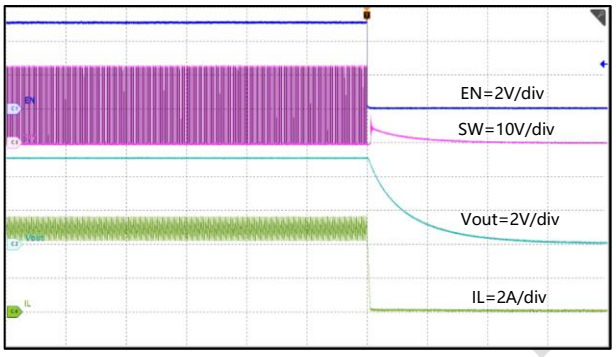


Figure 39. Shut-down with EN, I_{OUT}=5A

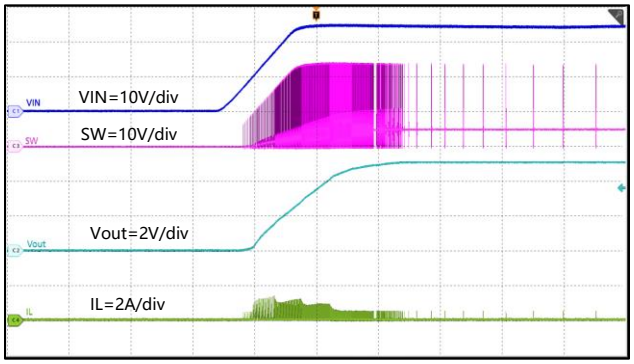


Figure 40. Start-Up with VIN rising, I_{OUT}=0A

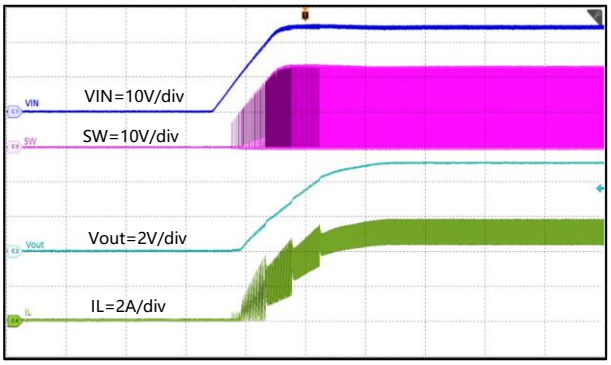


Figure 41. Start-Up with VIN Rising, I_{OUT}=5A

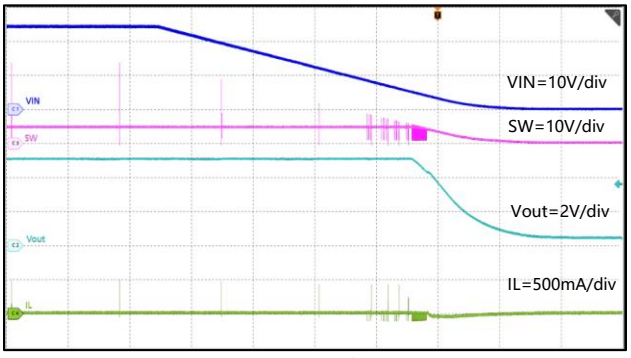


Figure 42. Shut-Down with VIN falling, I_{OUT}=0A

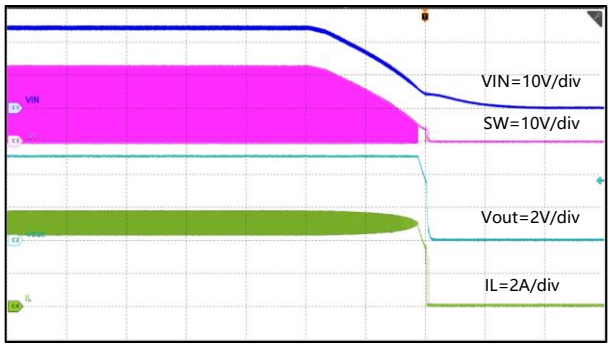
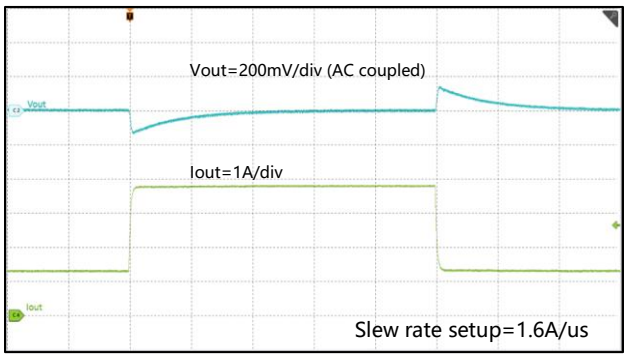
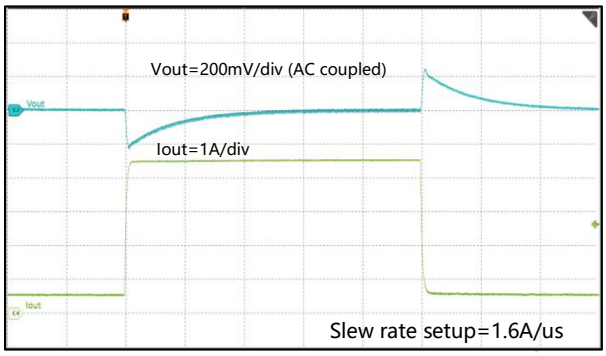


Figure 43. Shut-Down with VIN falling, I_{OUT}=5A



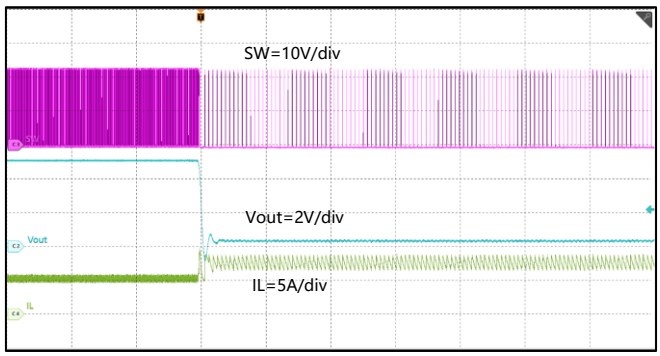
200us/div

Figure 44. Transient Response 1.25A-3.75A



200us/div

Figure 45. Transient Response 0.5A-4.5A



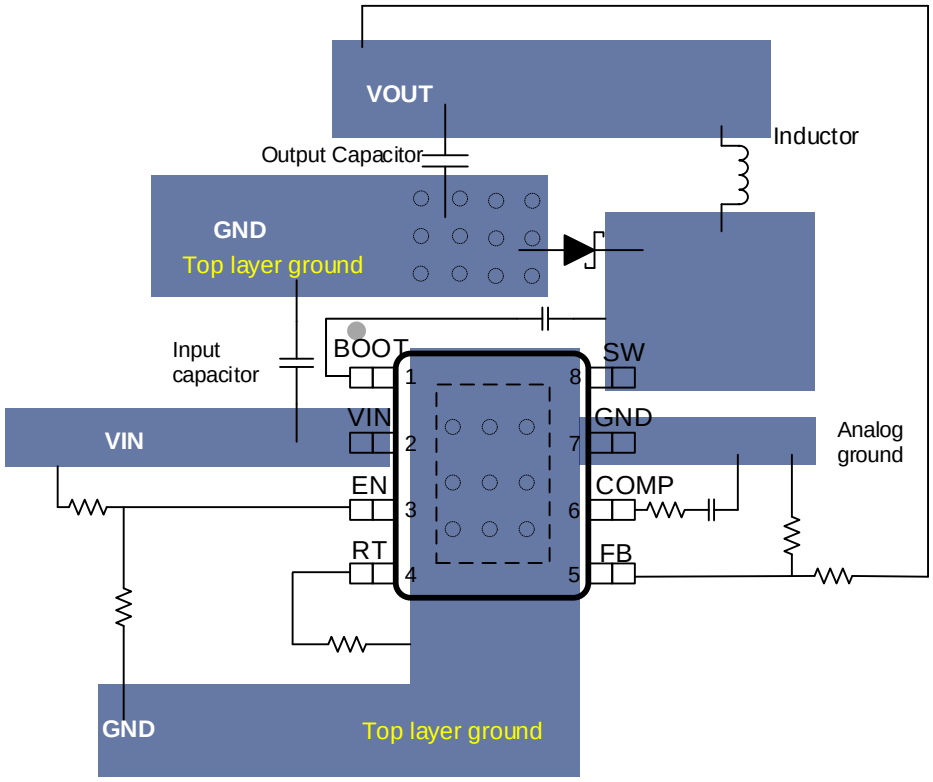
400us/div

Figure 46. Normal Operation to Hard-short I_{OUT}=5A

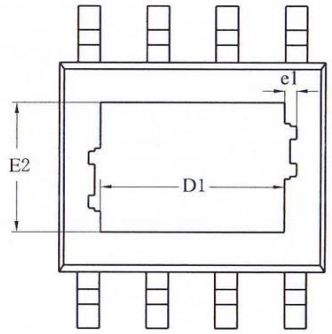
Layout Guideline

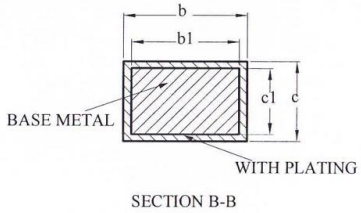
Layout is critical for proper operation. Please follow the layout guidelines.

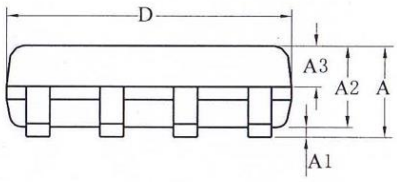
1. The power ground is very critical. The power trace should take lowest impedance as possible and the ground area should be sufficient and event to optimize thermal.
2. The GND Pin should be connected directly to the thermal pad under the IC, 8mil Max thermal via recommended.
3. Place the bypass input capacitor with low ESR as close as possible to the VIN pin and GND. The bypassing loop from VIN terminal to the GND should be as short as possible.
4. The RT/CLK is sensitive to noise. The RT/CLK resistor should be placed as close as possible to the RT/CLK pin with minimum trace length to the GND.
5. The inductor should be located as close as possible to the SW pin for reducing magnetic and electrostatic noise
6. The feedback resistor divider should be placed close to the FB pin.
7. The compensation network should be placed close to the COMP pin.
8. The ground connected to the diode, input capacitors and output capacitors should be tied to the system ground plane in only one spot to minimize conducted noise to the system ground plane
9. Four-layer layout is strongly recommended for better thermal performance.

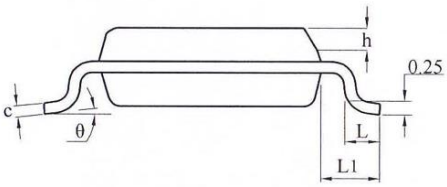


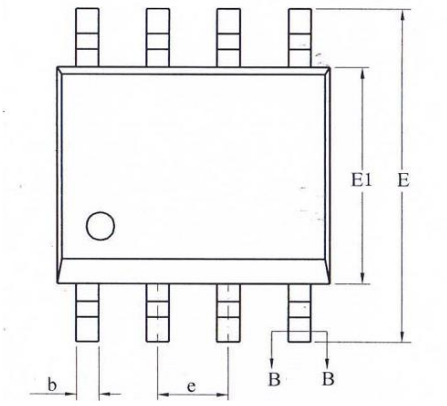
PACKAGE INFORMATION (eSOP-8L Package)











LF Size	D1	E2	e1
95*130	3.10	2.21	0.10REF

Symbol	Millimeter		
	Min	Nor	Max
A	-	-	1.65
A1	0.05	-	0.15
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.50	0.60	0.80
L1	1.05REF		
θ	0	-	8°