Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

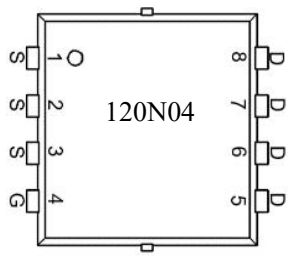
Bvdss	Rdson	ID
40V	2.1mΩ	120A

Application

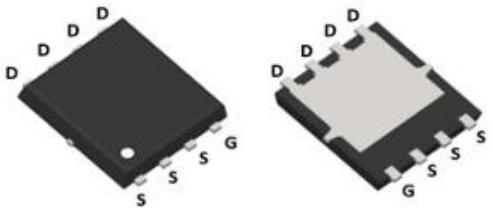
RoHS

- DC-DC Converters
- Power management functions
- High Frequency Switching and Synchronous Rectification

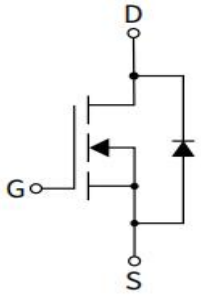
Package



Marking and pin assignment



PDFN3*3-8L top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
120N04	S120N04D	PDFN3*3-8L	5000

Absolute Maximum Ratings (T_J=25℃unless otherwise specified)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current[1]	(T_C=25℃)	I_D	120	A
Continuous Drain Current[1]	(T_C=100℃)	I_D	76	A
Pulsed Drain Current[2]		I_{DM}	480	A
Single Pulsed Avalanche Energy[3]		E_{AS}	180	mJ
Avalanche Current		I_{AS}	30	A
Power Dissipation[4]		P_D@T_C=25℃	65.7	W
Junction Temperature		T_J	-55~+150	℃
Storage Temperature		T_{STG}	-55~+150	℃

Thermal Resistance Ratings

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance,Junction-to-Case[1]	$R_{\theta JC}$	--	1.9	℃/W
Thermal Resistance,Junction-to-Ambient[1]	$R_{\theta JA}$	--	60	℃/W

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HLS120N04D	PDFN3*3-8L	4	5,6,7,8	1,2,3	Tape Reel

Electrical Characteristics (T_J=25℃,unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{DSS}	V_{GS}=0V I_D=250μA	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V,T_J=25℃	-	-	1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V,T_J=100℃	-	-	100	μA
Gate to Body Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±20V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.2	1.7	2.2	V
Static Drain-Source On-Resistance[2]	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	2.1	2.8	mΩ
		V_{GS}=4.5V, I_D=10A	-	2.8	3.8	mΩ
Forward Transconductance	gfs	V_{DS}=10V,I_D=20A	-	75	-	S
Gate Resistance	R_g	V_{DS}=0V,V_{GS}=0V,f=1MHz	-	1	-	Ω
Input Capacitance	C_{lss}	V_{DS}=20V,V_{GS}=0V, f=1.0MHz	-	2625	-	pF
Output Capacitance	C_{oss}		-	560	-	
Reverse Transfer Capacitance	C_{rss}		-	25	-	
Total Gate Charge	Q_g	V_{DS}=20V,V_{GS}=10V, I_D=20A	-	42.6	-	nC
Gate-Source Charge	Q_{gs}		-	6.6	-	
Gate-Drain(“Miller”) Charge	Q_{gd}		-	7.2	-	
Turn-on Delay Time	$T_{d(on)}$	V_{GS}=10V,V_{DD}=20V, R_G=3Ω,I_D=20A	-	9.8	-	nS
Turn-on Rise Time	t_r		-	8.7	-	
Turn-Off Delay Time	$T_{d(off)}$		-	30.8	-	
Turn-Off Fall Time	T_f		-	10.4	-	
Maximum Continuous Drain to Source Diode Forward Current[1,4]	I_S	V_G=V_D=0V,Force Current	-	-	120	A
Maximum Pulsed Drain to Source Diode Forward Current	I_{SM}	--	-	-	-	A
Diode Forward Voltage[2]	V_{SD}	V_{GS}=0V,I_S=1A,T_J=25℃	-	-	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F=20A,di/dt=100A/μs, T_J=25℃	-	46	-	nS
Body Diode Reverse Recovery Charge	Q_{rr}		-	18.4	-	nC

Notes:

1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.

3.The EAS data shows Max. rating . The test condition is T_J=25℃ ,V_{DD}=25V,V_{GS}=10V,L=0.5mH,I_{AS}=30A.

4.The power dissipation is limited by 150℃ junction temperature.

5.The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

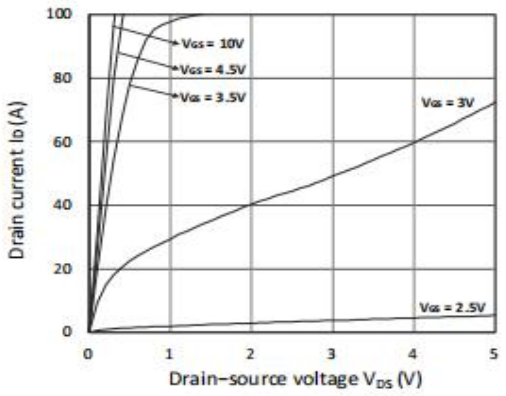


Figure 1. Output Characteristics

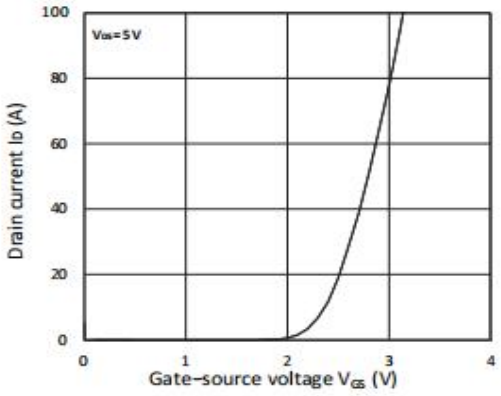


Figure 2. Transfer Characteristics

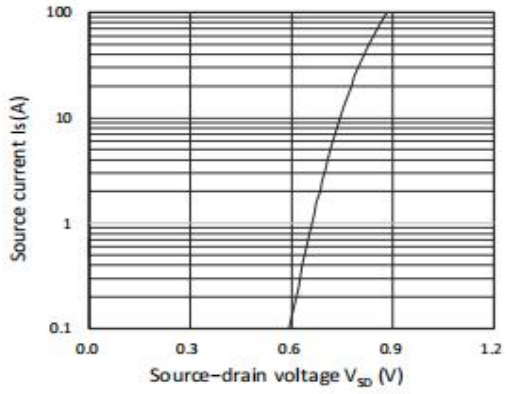


Figure 3. Forward Characteristics of Reverse

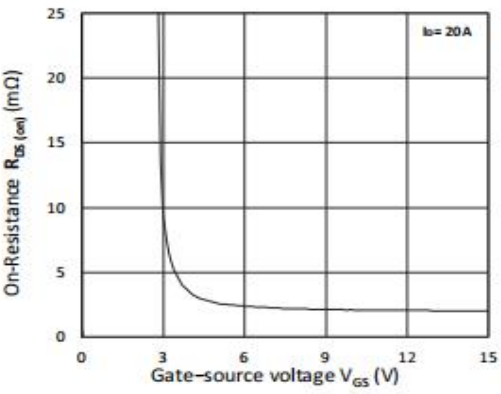


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

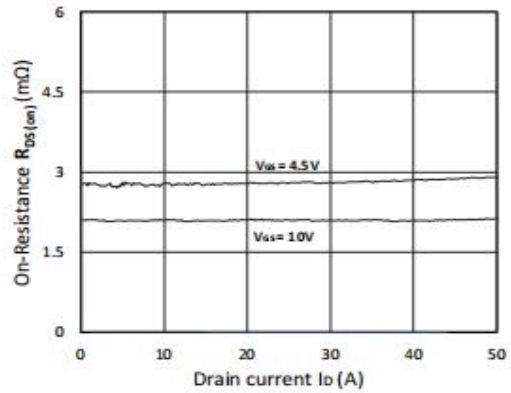


Figure 5. $R_{DS(ON)}$ vs. I_D

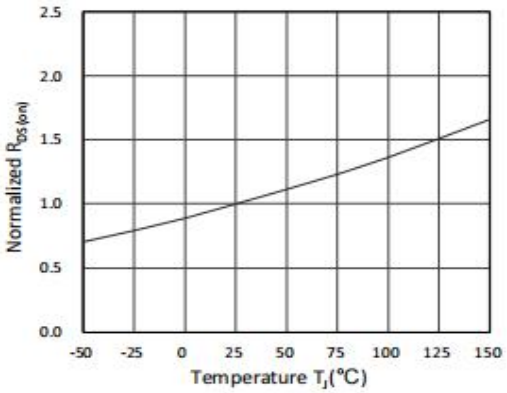


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

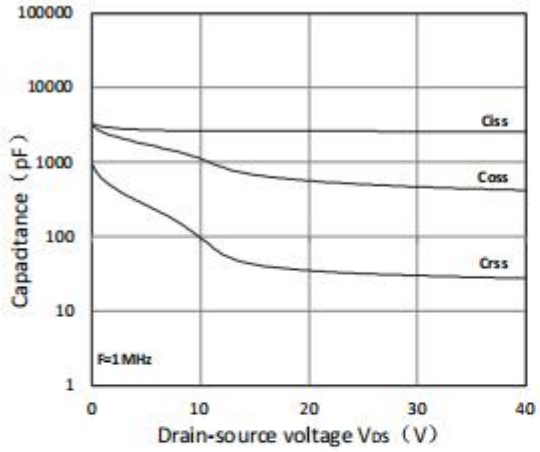


Figure 7. Capacitance Characteristics

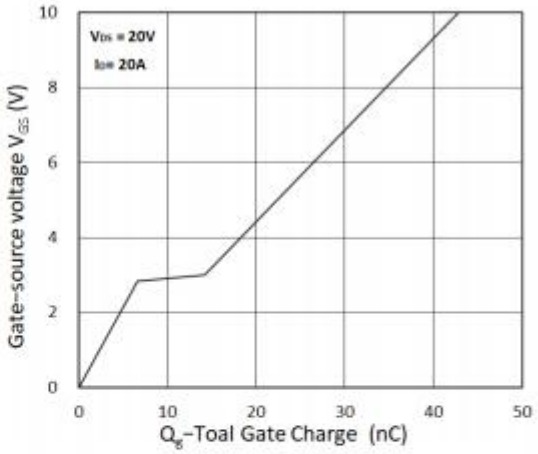


Figure 8. Gate Charge Characteristics

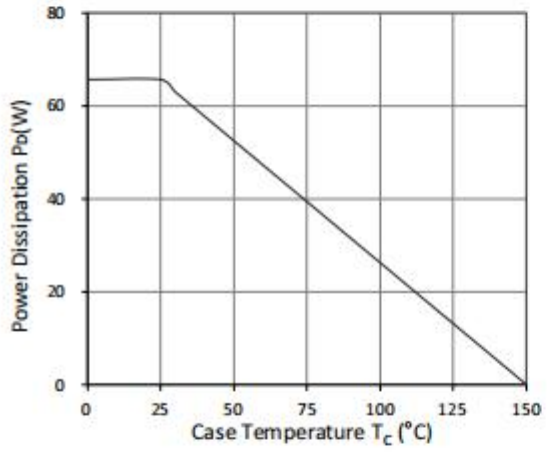


Figure 9. Power Dissipation

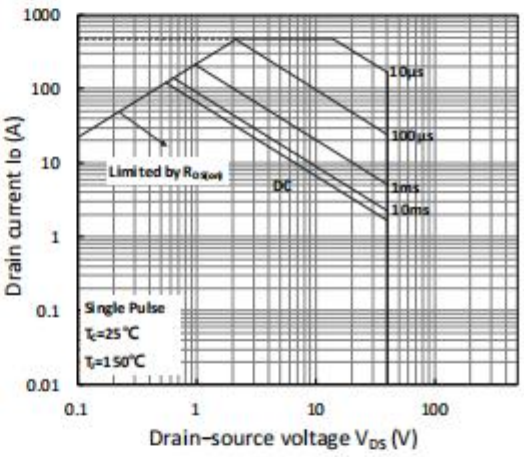


Figure10. Safe Operating Area

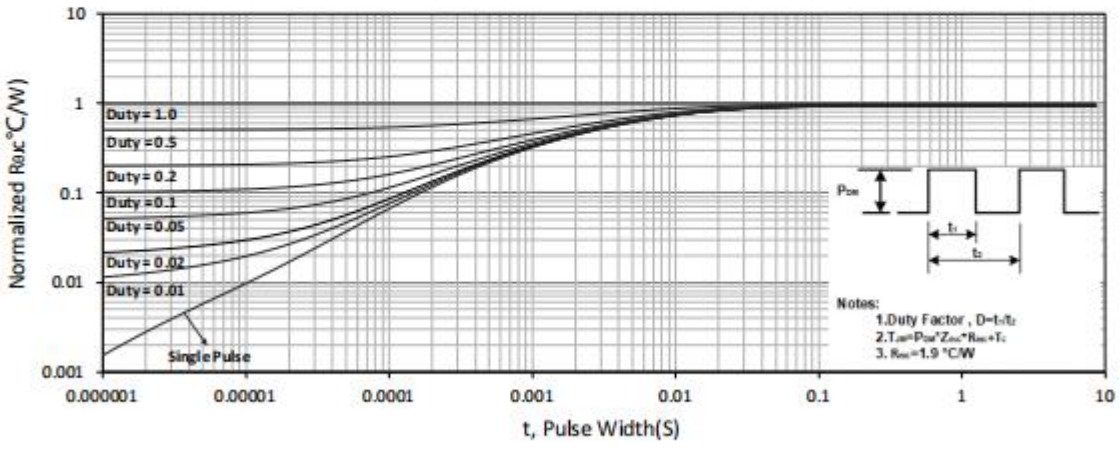


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

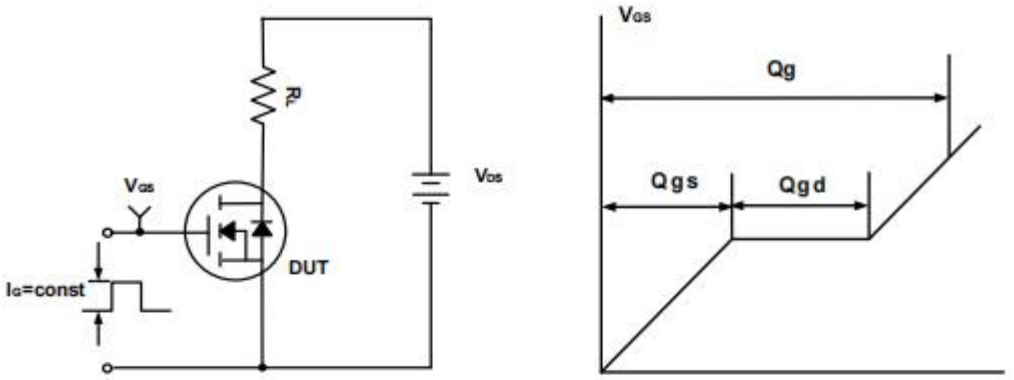


Figure A. Gate Charge Test Circuit & Waveforms

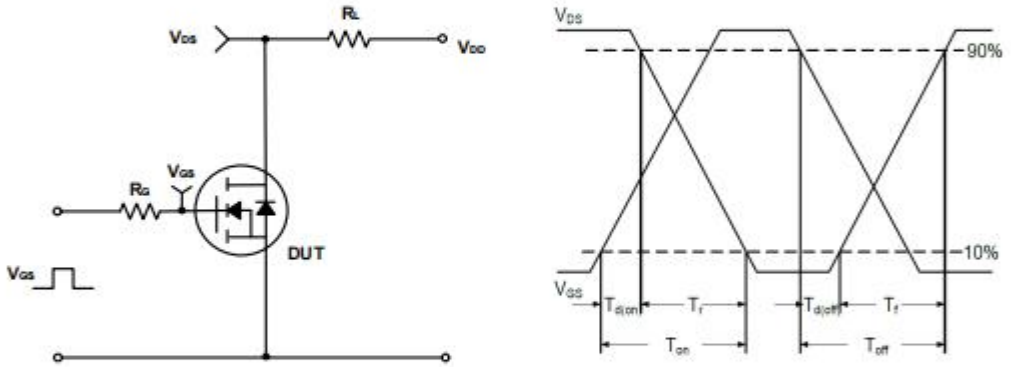


Figure B. Switching Test Circuit & Waveforms

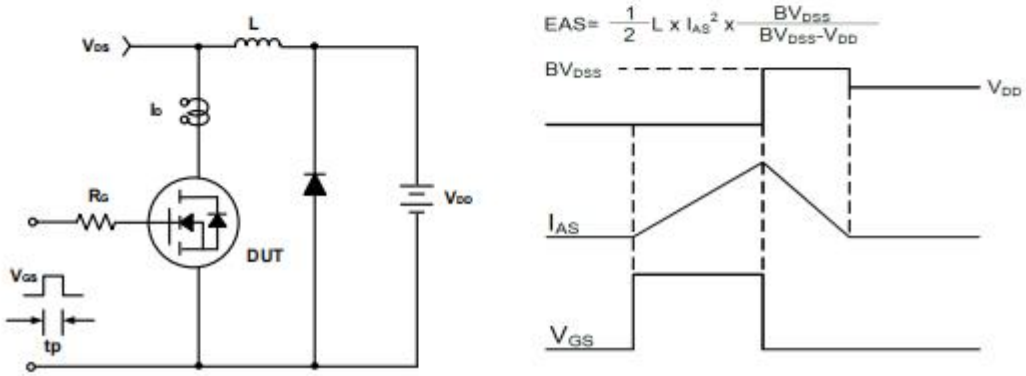
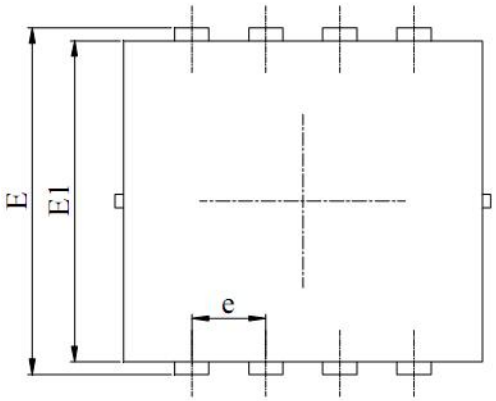
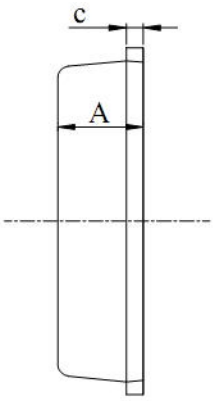


Figure C. Unclamped Inductive Switching Circuit & Waveforms

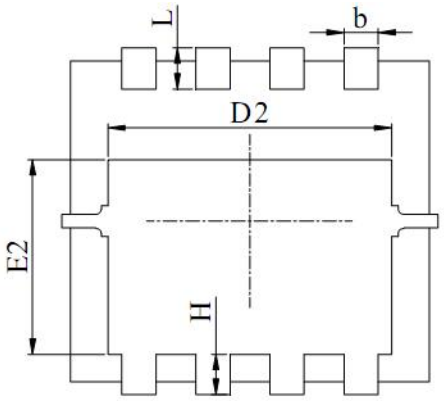
Package Dimensions PDFN3x3-8L



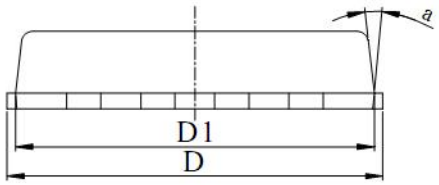
Top View



Side View



Bottom View

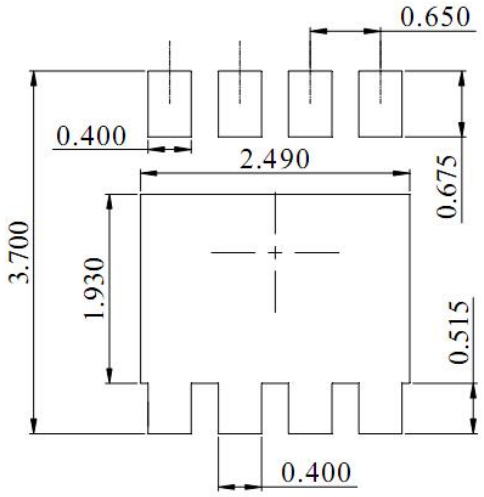


Front View

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. ALL DIMNESIONS IN MILLIMETER (ANNGLE IN DEGREE).
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.20	0.25
D	3.00	3.15	3.25
D1	2.95	3.05	3.15
D2	2.39	2.49	2.59
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	1.70	1.80	1.90
e	0.65 BSC		
H	0.30	0.40	0.50
L	0.25	0.40	0.50
a	---	---	15°



DIMENSIONS:MILLIMETERS

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