

## HMC221BETR-HX GaAs, MMIC, SPDT Switch, 10 kHz to 3 GHz

### Description

The HMC221BETR-HX is a single-pole, double-throw (SPDT) switch designed for operation within the frequency range of 10 kHz to 3 GHz, housed in a compact 6-lead SOT-23 plastic package. This switch features an exceptionally low insertion loss of less than 0.8 dB up to 3 GHz, making it particularly suitable for receiver and filter switching applications that demand both minimal insertion loss and a small form factor.

In its off state, the RF1 and RF2 pins exhibit reflective shorts, while the two control voltages—designated as the A and B pins—require only a minimal DC bias current.

### Features

- ★ Low insertion loss: 0.4 dB typical
- ★ Input third-order intercept (IP3): 55 dBm typical
- ★ Positive control: 0 V/3 V
- ★ Ultrasmall package: SOT-23

### Applications

- ★ Industrial, scientific and medical (ISM) PCMCIA wireless cards
- ★ Cellular applications

### Functional block diagram

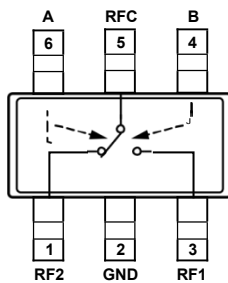


Figure 1.SOT-23

## Specifications

Table 1.  $T_A = 25^\circ\text{C}$ ,  $V_{CTL} = 0\text{ V}/3\text{ V to }8\text{ V}$ ,  $50\ \Omega$  system, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
FREQUENCY BAND			0.01		3000	MHz
INSERTION LOSS		10 kHz to 1.0 GHz		0.4	0.7	dB
		1.0 GHz to 2.0 GHz		0.45	0.8	dB
		2.0 GHz to 2.5 GHz		0.6	0.9	dB
		2.5 GHz to 3.0 GHz		0.8	1.1	dB
Flatness		20 MHz to 1.0 GHz, maximum to minimum		0.3		dB
ISOLATION		10 kHz to 1.0 GHz	24	30		dB
		1.0 GHz to 2.0 GHz	24	29		dB
		2.0 GHz to 2.5 GHz	21	25		dB
		2.5 GHz to 3.0 GHz	14	18		dB
RETURN LOSS		10 kHz to 1.0 GHz	25	33		dB
		1.0 GHz to 2.0 GHz	20	30		dB
		2.0 GHz to 2.5 GHz	20	25		dB
		2.5 GHz to 3.0 GHz	11	22		dB
GROUP DELAY <sup>1</sup>		0.5 GHz to 1.0 GHz, maximum to minimum		30		ps
INPUT LINEARITY		$V_{CTL} = 0\text{ V}/5\text{ V}$				
1 dB Power Compression	P1dB	10 kHz to 20 MHz	6	8 <sup>1</sup>		dBm
		20 MHz to 250 MHz	25	11		dBm
		250 MHz to 1.0 GHz	25	30		dBm
		1.0 GHz to 3.0 GHz	23	29		dBm
Third-Order Intercept <sup>1</sup>	IP3	Two-tone input power = 9 dBm/tone, $\Delta f = 1\text{ MHz}$				
		10 kHz to 10 MHz	9			dBm
		10 MHz to 20 MHz	12			dBm
		20 MHz to 30 MHz	15			dBm
		30 MHz to 250 MHz	18	26		dBm
		250 MHz to 1.0 GHz	40	55		dBm
		1.0 GHz to 3.0 GHz	38	54		dBm
SWITCHING CHARACTERISTICS <sup>1</sup>						
Rise and Fall Time	$t_{RISE}, t_{FALL}$	10% to 90% of RF output		3		ns
On and Off Time	$t_{ON}, t_{OFF}$	50% $V_{CTL}$ to 10%/90% of RF output		10		ns
CONTROL INPUTS		A and B pins				
Voltage <sup>2</sup>	$V_{CTL}$					
High	$V_{INH}$		3		8	V
Low	$V_{INL}$			0		V
Current	$I_{CTL}$					
High	$I_{INH}$	$V_{CTL} = 0\text{ V}/3\text{ V}$		0.1		$\mu\text{A}$
		$V_{CTL} = 0\text{ V}/5\text{ V}$		1		$\mu\text{A}$
		$V_{CTL} = 0\text{ V}/8\text{ V}$		5		$\mu\text{A}$
Low	$I_{INH}$	$V_{CTL} = 0\text{ V}/3\text{ V}$		-0.1		$\mu\text{A}$
		$V_{CTL} = 0\text{ V}/5\text{ V}$		-1		$\mu\text{A}$
		$V_{CTL} = 0\text{ V}/8\text{ V}$		-5		$\mu\text{A}$

1. Guaranteed by design but not production tested.

2. The control input voltage tolerances are  $\pm 0.2\text{ V}$  dc.

## Absolute maximum rated

Table 2.

Parameter	Rating
Control Voltage Range (A and B)	-0.2 V dc to 12 V dc
RF Input Power Level (CW Peak, $V_{CTL} = 0\text{ V}/5\text{ V}$ )	0.36 W
10 kHz to 10 MHz	8 dBm
10 MHz to 20 MHz	10 dBm
20 MHz to 30 MHz	11 dBm
30 MHz to 250 MHz	14 dBm
250 MHz to 3.0 GHz	31 dBm
Hot Switching RF Input Power Level (CW Peak, $V_{CTL} = 0\text{ V}/5\text{ V}$ )	
10 kHz to 250 MHz	6 dBm
250 MHz to 3.0 GHz	20 dBm
Continuous Power Dissipation, $P_{DISS}$ (at $T_{CASE} = 85^{\circ}\text{C}$ )	0.36 W
Junction to Case Thermal Resistance, $Q_{JC}$	178°C/W
Temperature	
Junction, $T_J$	
Storage	-65°C to +150°C
Reflow <sup>1</sup> (MSL1 Rating)	260°C
<b>HMC221BETR-HXE</b>	
ESD Sensitivity	250 V (Class 1A)
Human Body Model (HBM)	

1. See the Ordering Guide for additional information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



ESD (electrostatic discharge) sensitive device. charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD Precautions should be taken to avoid performance degradation or loss of functionality.

## Pin configuration and function description

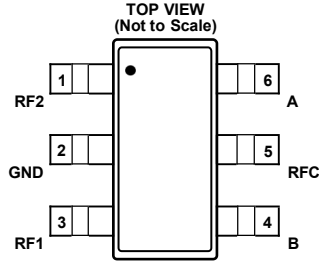


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No	Mnemonic	Description
1	RF2	RF2 Port (SeeFigure 4). This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required.
2	GND	Ground (SeeFigure 6). This pin must be connected to the RF/dc ground of the printed circuit board (PCB).
3	RF1	RF1 Port (SeeFigure 4). This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required.
4	B	Control Input A (SeeTable 4andFigure 5).
5	RFC	RF Common Port (SeeFigure 3). This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required.
6	A	Control Input B (SeeTable 4andFigure 5).

Table 4. Truth Table

Control Input Voltage		Signal Path State	
A (V dc)	B (V dc)	RFC to RF1	RFC to RF2
Low	High	On	Off
High	Low	Off	On

1.All high or all low for control inputs, A and B, are undefined states. The switch response has a high insertion loss and poor return loss on both RF paths.

### Interface schematic

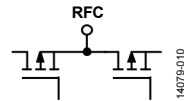


Figure 3. RFC Interface

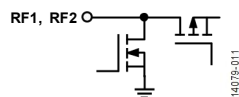


Figure 4. RF1 and RF2 Interface



Figure 5. A and B Interface



Figure 6. GND Interface

## Typical performance characteristics

### INSERTION LOSS, RETURN LOSS, AND ISOLATION

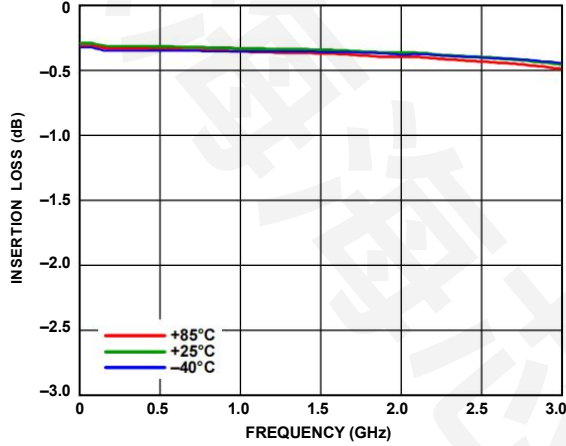


Figure 7. Insertion Loss vs. Frequency over Temperature

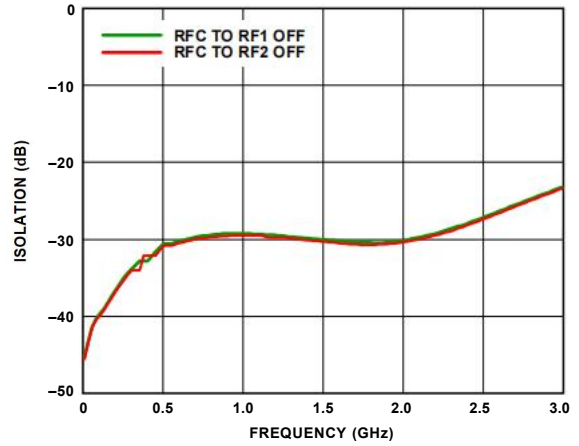


Figure 9. Isolation Between RFC and RF1/RF2 Ports vs. Frequency

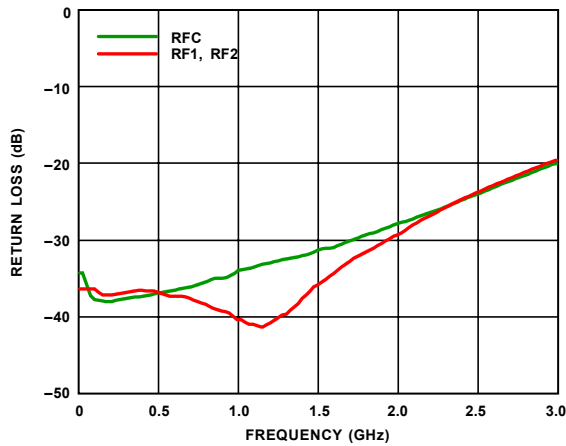


Figure 8. Return Loss vs. Frequency

## INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

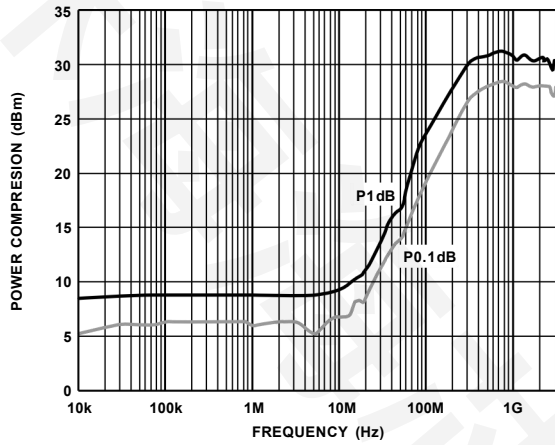


Figure 10. Input 1 dB Power Compression (P1dB) and Input 0.1dB Power Compression (P0.1dB) vs. Frequency,  $V_{CTL} = 0 V/5 V$

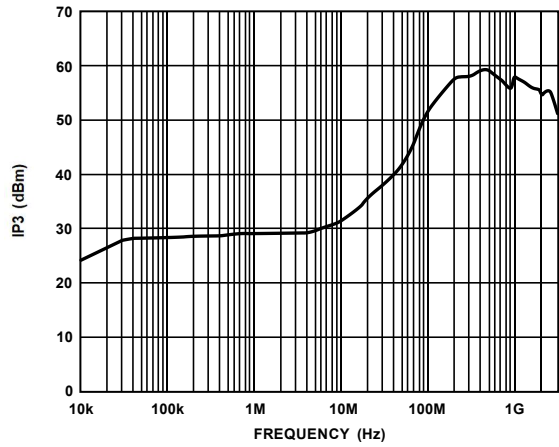


Figure 12. Input Third-Order Intercept (IP3) vs. Frequency,  $V_{CTL} = 0 V/5 V$

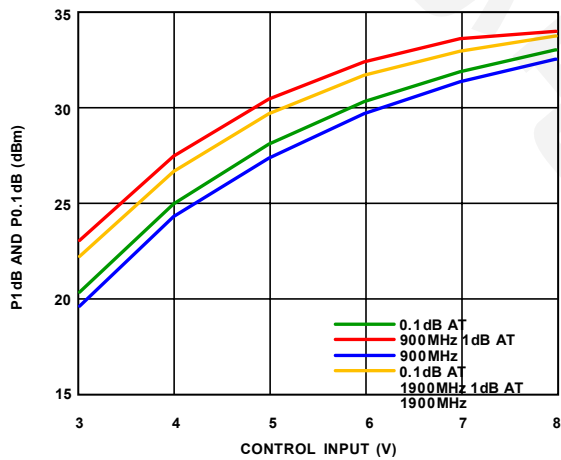


Figure 11. Input 1 dB Power Compression (P1dB) and Input 0.1dB Power Compression (P0.1dB) vs. Control Input Voltage

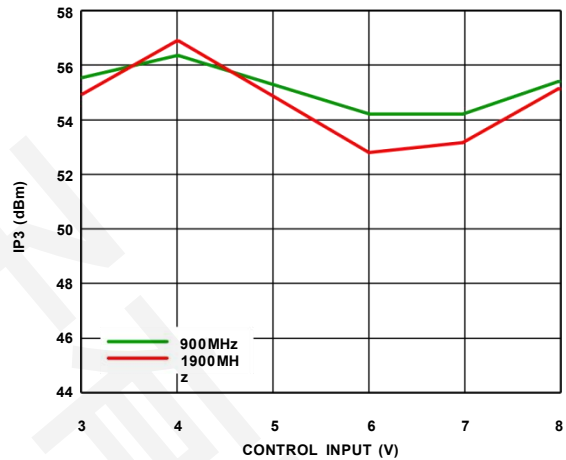


Figure 13. Input IP3 vs. Control Input Voltage

## Application information

### TYPICAL APPLICATION CIRCUIT

Two cascaded, CMOS inverters, biased with  $V_{DD} = 5\text{ V}$ , can generate complementary control voltages,  $V_{CTL} = 0\text{ V}/5\text{ V}$ , for the A and B inputs. Therefore, the HMC221BETR-HX can be controlled from a single CMOS input line (see Figure 14).

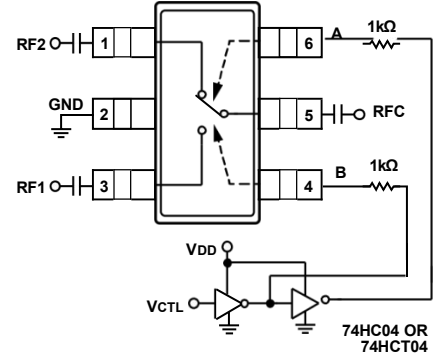


Figure 14. Typical Application Circuit

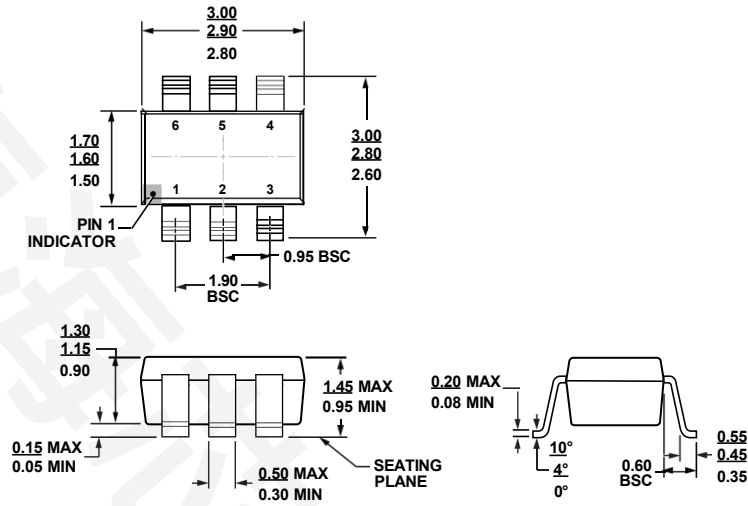
## BILL OF MATERIALS

Table 5. List of Materials for Evaluation

Item	Description
J1 to J3	PCB mount SMA RF connectors
J4 to J6	DC pins
C1 to C3	330 pF capacitors
R1, R2	1 kΩ resistors,
U1	HMC221BETR-HX SPDT switch
PCB	600-00382-00-1 evaluation PCB, circuit board material

1. References this number when ordering the evaluation PCB.

## Outline dimensions



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 15. 6-Lead Small Outline Transistor Package [SOT-23] (RJ-6)

Dimensions shown in millimeters

## Ordering guide

Model	Temperature	Description
HMC221BETR-HX	-40°C to +85°C	6-Lead Small Outline Transistor Package [SOT-23]