钍地半导体
Tudi Semiconductor

Product Specification

TUDI-93xx46/56/66

Three-wire Serial EEPROM

网址 www.sztdbdt.com

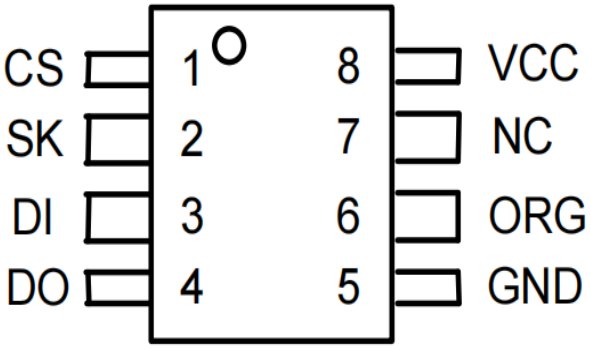
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- READY/ BUSY signal during programming
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 40 Years
- Three-wire Serial Interface
- 2MHz (2.5V) and 1MHz (1.7V) Compatibility
- Dual organization: by word (x16) or byte (x8)
- Low-voltage and Standard-voltage Operation 1.7V～5.5V
- Self-timed Write Cycle (5 ms max)
- Sequential read operation
- Programming instructions that work on: byte, word or entire memory



Pin Diagram

Description

93xx46/56/66 provides 1k/2k/4k bits of serial electrically erasable programmable read-only memory (EEPROM), organized as 64/128/256 words of 16 bits each (when the ORG pin is connected to VCC), and 128/256/512 words of 8 bits each (when the ORG pin is connected to ground).The 93xx46/56/66 is enabled through the Chip Select pin (CS) and accessed via a three-wire serial interface consisting of Data Input (DI), Data Output (DO), and Serial Clock (SK). Upon receiving a read instruction at DI,the address is decoded and the data is clocked out serially on the data output pin DO. The write cycle is completely self-timed and no separate erase cycle is required before write.The write cycle is only enabled when the part is in the Erase/Write Enable State. When CS is brought " high " following ___ nitiation of a write cycle, The DO pin outputs the Ready/ Busy status of the part.The device is the best choice for use in many industrial and commercial applications where low-power and low-voltage operations are essential.

Pin Configurations

Pin Name	Function	Pin Name	Function
CS	Chip Select	GND	Ground
SK	Serial Clock	ORG	Organization Select
DI	Serial Data Input	NC	No connect
DO	Serial Data Output	VCC	Power Supply

Absolute Maximum Ratings

Operating Temperature	-55℃ ~+125℃
Storage Temperature	65℃~+150℃
Voltage on Any Pin with Respect to Ground	-1.0V ~ +7.0V
Maximum Operating Voltage	6.25V
DC output current	5.0 mA

*NOTICE:Stresses beyond those listed under “ Absolute Maximum Ratings ” may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

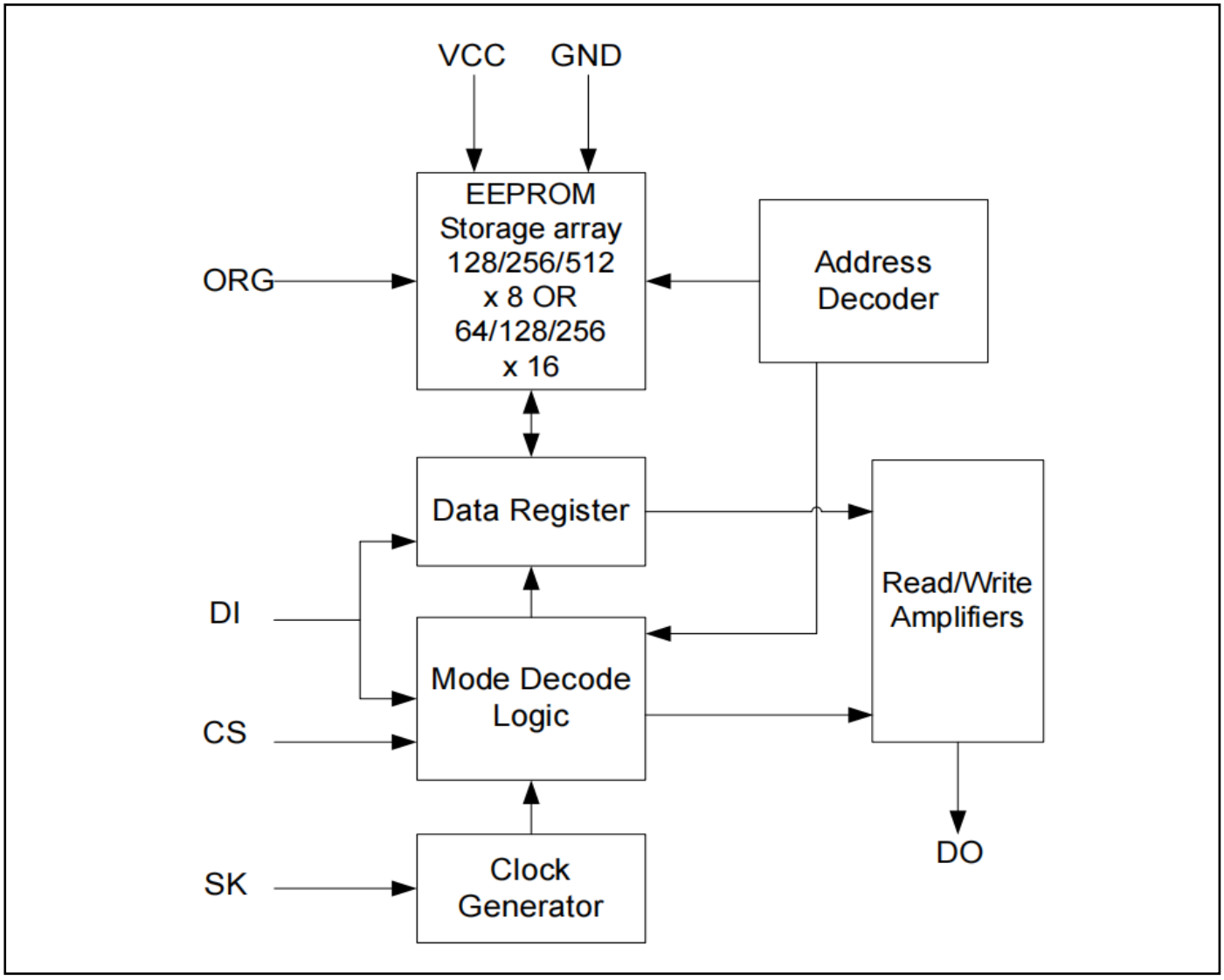


Figure 1 Block Diagram

Timing Diagrams

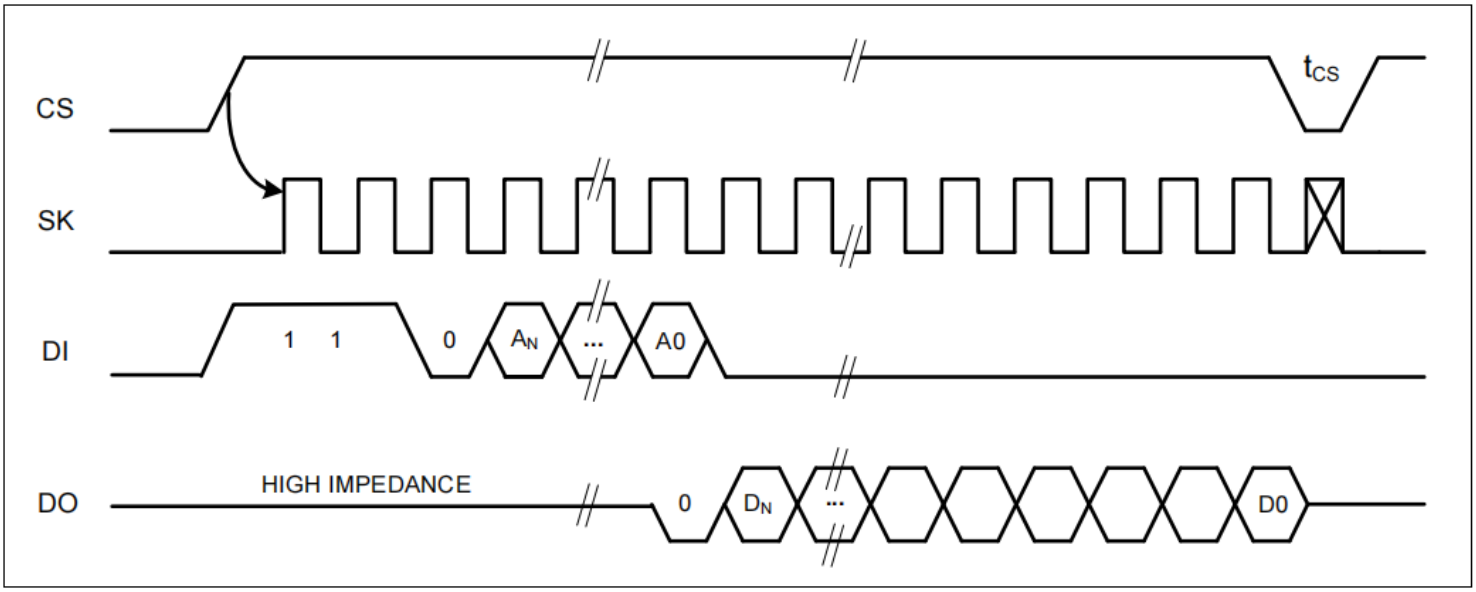


Figure 2 READ Timing

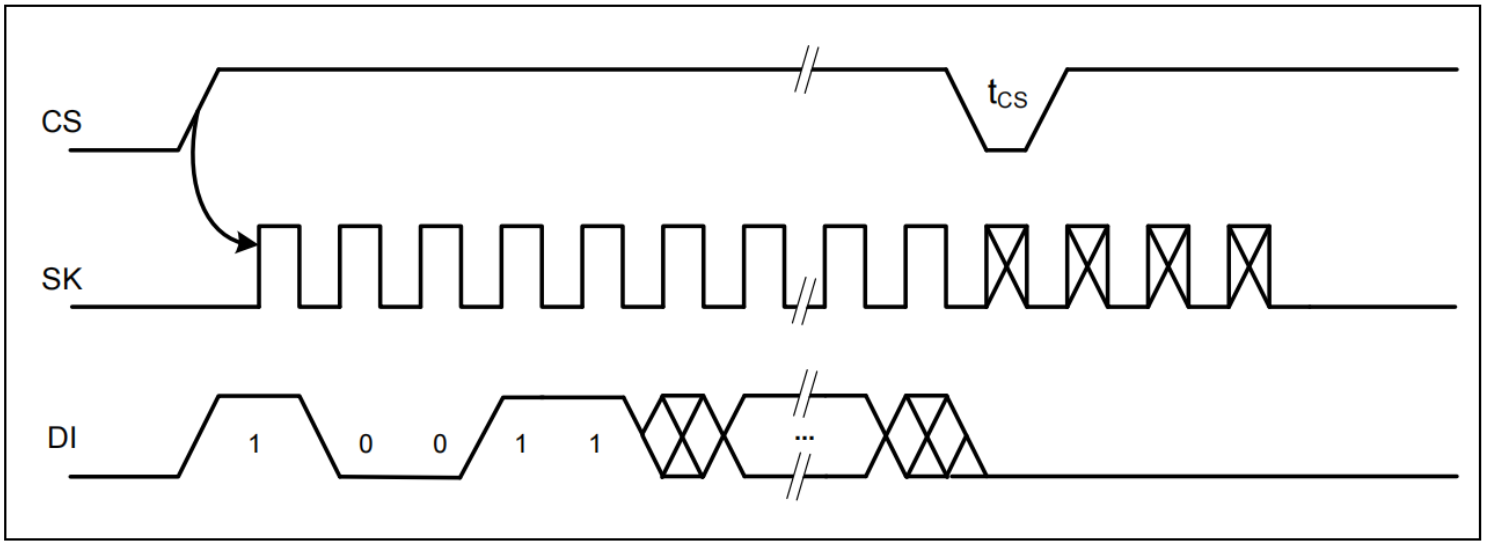


Figure 3 EWEN Timing

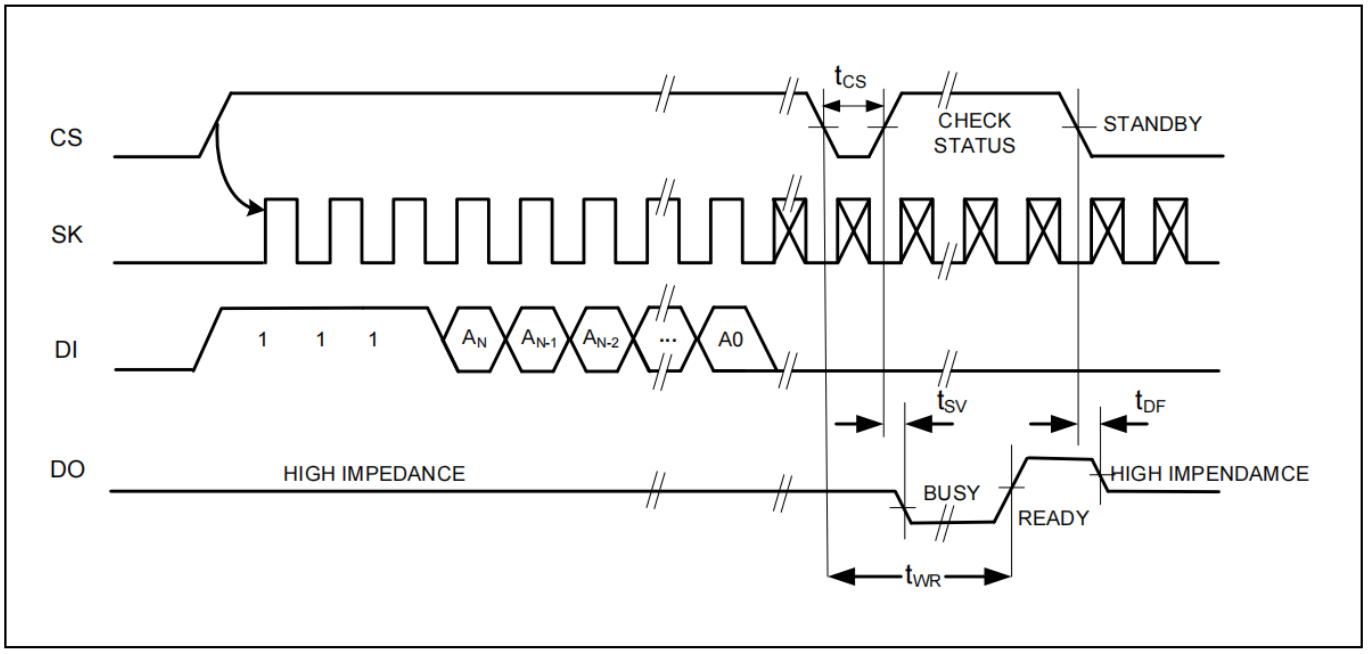


Figure 4 ERASE Timing

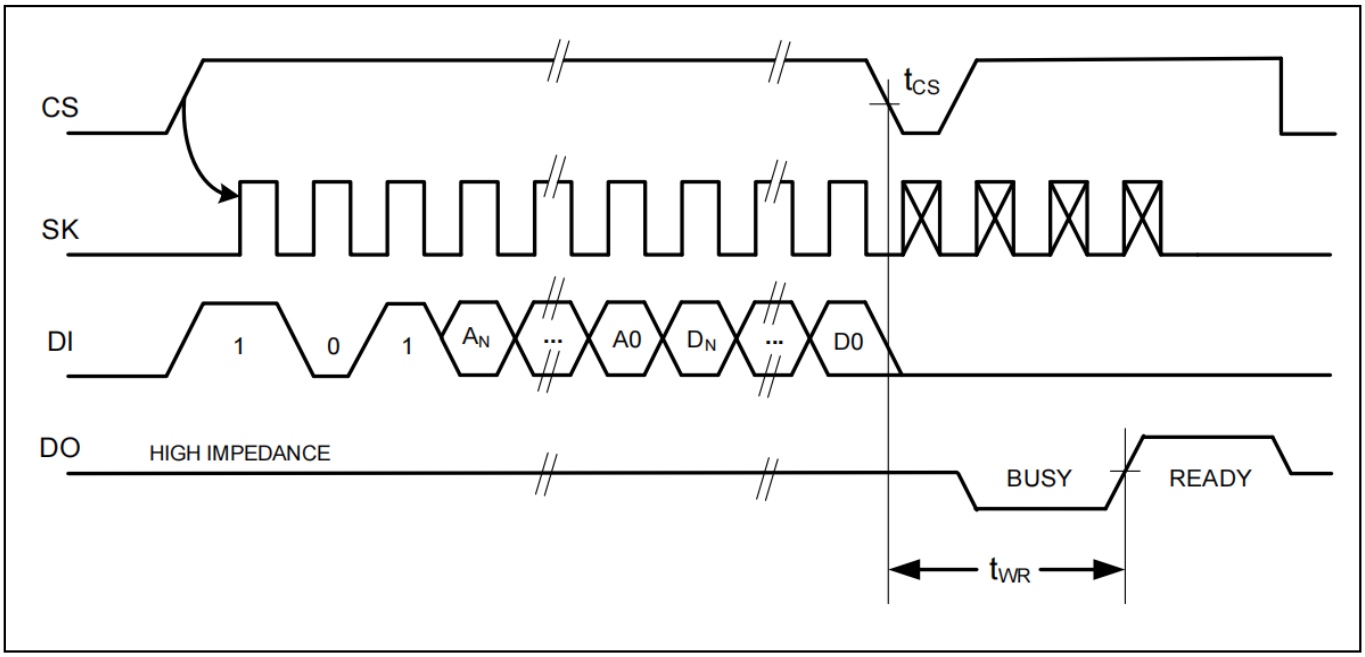


Figure 5 WRITE Timing

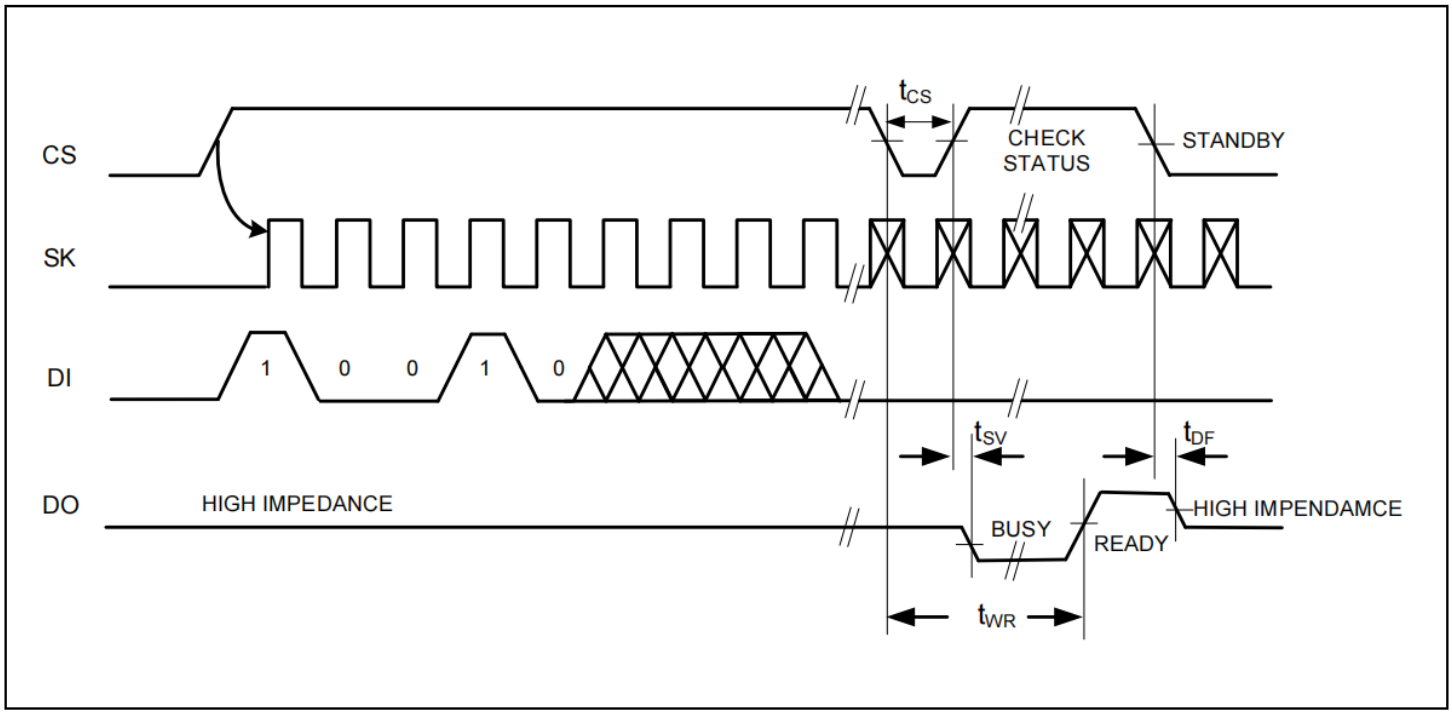


Figure 6 ERAL Timing

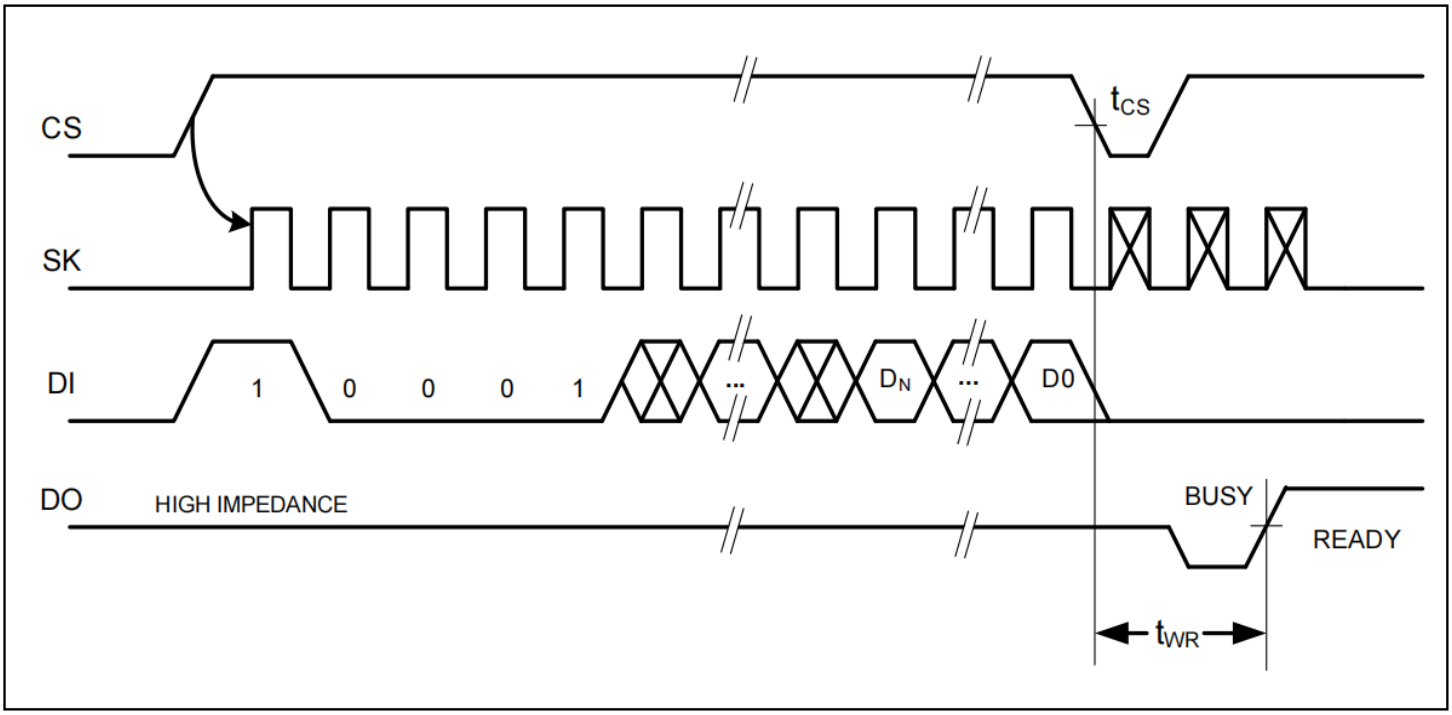


Figure 7 WRAL Timing

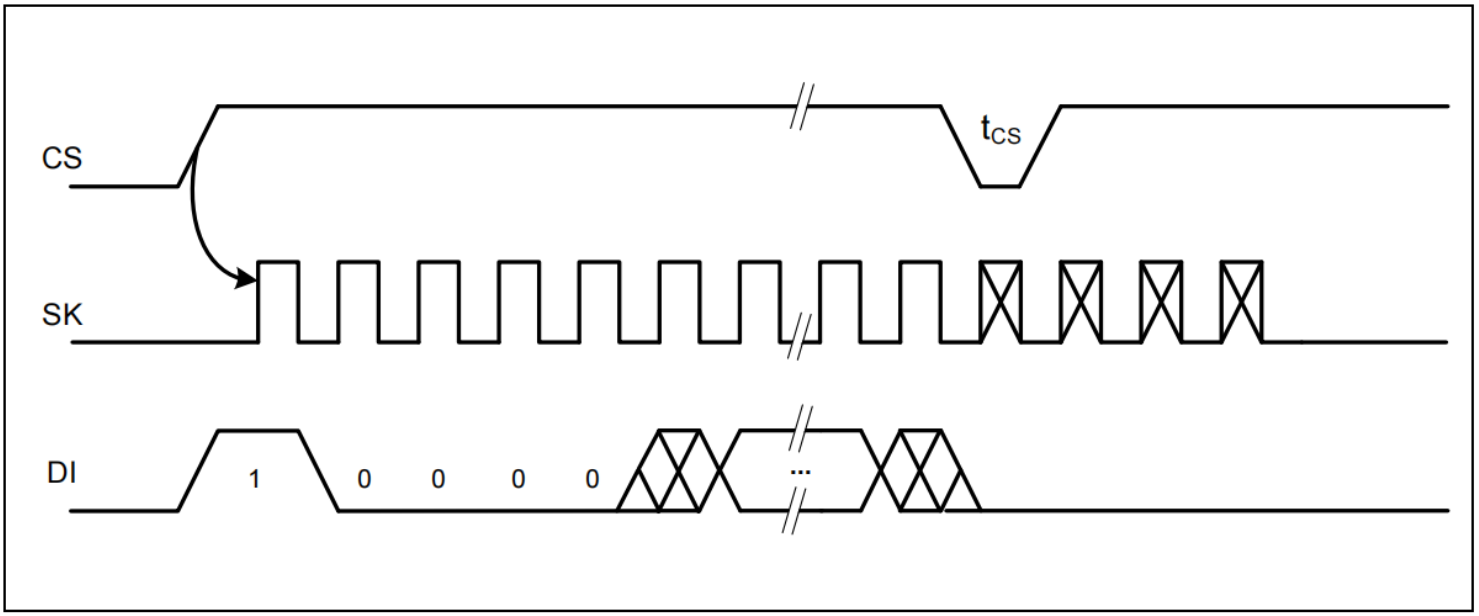


Figure 8 EWDS Timing

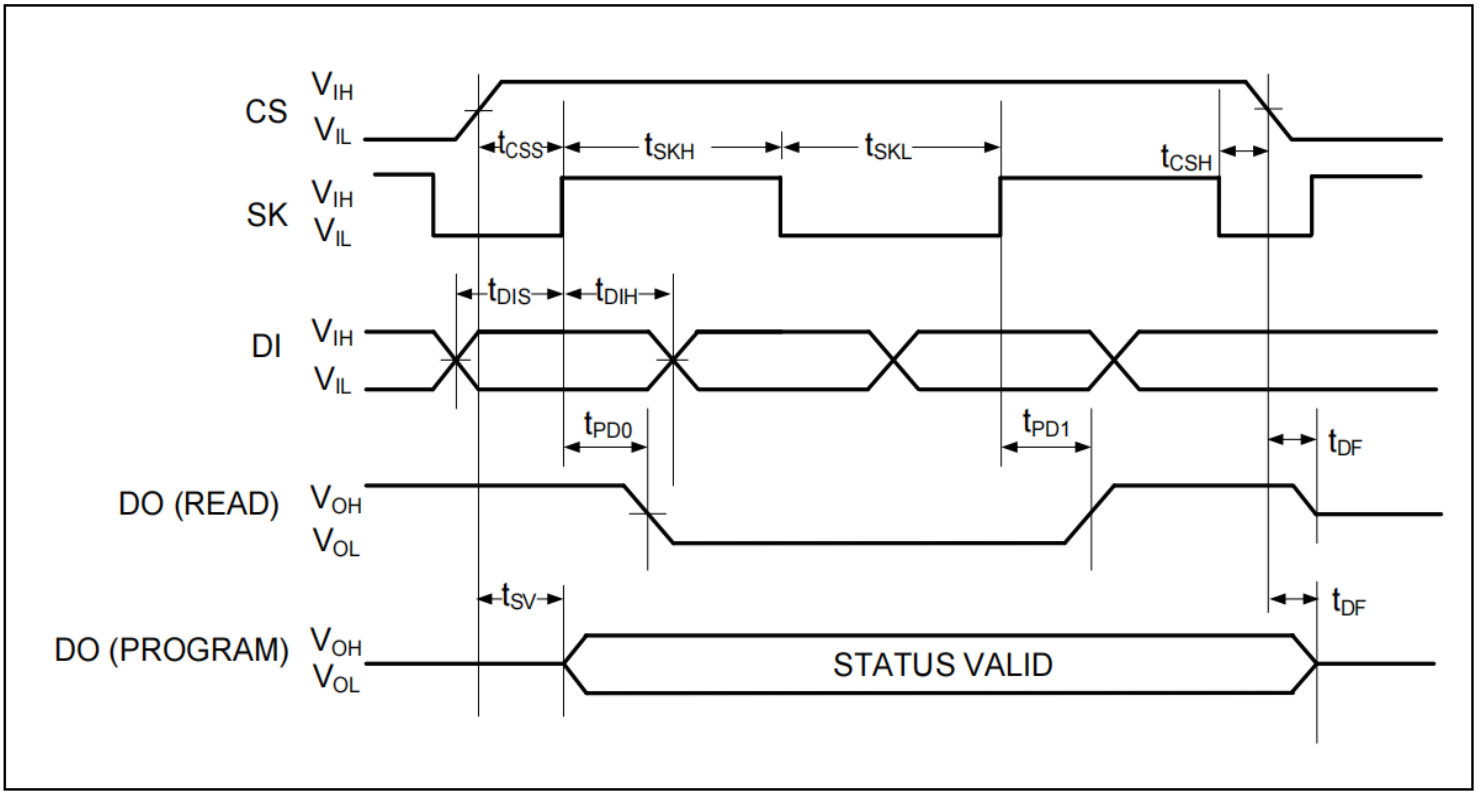


Figure 9 BUS Timing

Memory Organization

The 93xx46/56/66memory is organized either as bytes (x8) or as words (x16). If Organization Select (ORG) is left unconnected (or connected to VCC) the x16 organization is selected; when Organization Select (ORG) is connected to Ground (VSS) the x8 organization is selected. When the 93xx46/56/66is in Standby mode, Organization Select (ORG) should be set either to VSS or VCC for minimum power consumption. Any voltage between VSS and VCC applied to Organization Select (ORG) may increase the Standby current.

Device	Number of bits	Number of 8-bit bytes	Number of 16-bit words
93xx66	4096	512	256
93xx56	2048	256	128
93xx46	1024	128	64

Memory size versus organization

Functional Description

The 93xx46/56/66 is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. A valid instruction starts with a rising edge of CS and consists of a start bit (logic “ 1 ”) followed by the appropriate op code and the desired memory address location.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable(EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

READ (READ): The Read (READ) instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock (SK).. It should be noted that a dummy bit (logic “ 0 ”) precedes the 8- or 16 -bit data output string.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable(EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the EWEN state, programming remains enabled until an EWDS instruction is executed or VCC power is removed from the part.

READY/ BUSY status: While the Write or Erase cycle is underway, for a WRITE, ERASE, WRAL or ERAL instruction, the Busy signal (DO=0) is returned whenever Chip Select input (CS) is driven high. (Please note, though, that there is an initial delay, of t_{CS}, before this status information becomesavailable).Inthisstate,the93xx46/56/66ignores any data on the bus. When the Write cycle is completed, and Chip Select Input (CS) is driven high, the Ready signal (DO=1) indicates that the 93xx46/56/66is ready to receive the next instruction. Serial Data Output (DO) remains set to 1 until the Chip Select Input (CS) is brought low or until a new start bit is decoded.

ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic " 1 " state and is primarily used for testing purposes. The DO pin outputs the Ready/ Busy status of the part if CSis brought high after being kept low for a minimum of 250 ns (tCS). The ERAL instruction is valid only at Vcc =2.5V ~5 .5V

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/ Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (tCS). The WRAL instruction is valid only at Vcc = 2.5V ~5 .5V.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable(EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the EWEN state, programming remains enabled until an EWDS instruction is executed or VCC power is removed from the part.

ERASE (ERASE): The Erase (ERASE) instruction programs all bits in the specified memory location to the logical " 1 " state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the Ready/ Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (tCS).A logic " 1 " at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specifiedmemorylocation.Theself-timedprogrammingcycle tWP starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the Ready/ Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (tCS). A logic " 0 " at DO indicates that programming is still in progress. A logic " 1 " indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. A Ready/ Busy status cannot be obtained if the CS is brought high after the end of the selftimed programming cycle, t_{WP}.

Instruction Set

Instruction	DeviceType	SB	OpCode	Address		Data		Comments
				x8(1)(2)	x16(1)(3)	x8	x16	
READ	93xx46 93xx56 93xx66	1 1 1	101010	A6-A0 A8-A0 A8-A0	A5-A0 A7-A0 A7-A0			Read Address AN-A0
EWEN	93xx46 93xx56 93xx66	1 1 1	000000	11XXXXX 11XXXXXXX 11XXXXXXX	11XXXX 11XXXXXX 11XXXXXX			Write Enable
ERASE	93xx46 93xx56 93xx66	1 1 1	111111	A6-A0 A8-A0 A8-A0	A5-A0 A7-A0 A7-A0			Clear Address AN-A0
WRITE	93xx46 93xx56 93xx66	1 1 1	010101	A6-A0 A8-A0 A8-A0	A5-A0 A7-A0 A7-A0	D7-D0 D7-D0 D7-D0	D15-D0 D15-D0 D15-D0	Write Address AN-A0
ERAL	93xx46 93xx56 93xx66	1 1 1	000000	10XXXXX 10XXXXXXX 10XXXXXXX	10XXXX 10XXXXXX 10XXXXXX			Clear All Addresses
WRAL	93xx46 93xx56 93xx66	1 1 1	000000	01XXXXX 01XXXXXXX 01XXXXXXX	01XXXX 01XXXXXX 01XXXXXX	D7-D0 D7-D0 D7-D0	D15-D0 D15-D0 D15-D0	Write All Addresses
EWDS	93xx46 93xx56 93xx66	1 1 1	000000	00XXXXX 00XXXXXXX 00XXXXXXX	00XXXX 00XXXXXX 00XXXXXX			Write Disable

Note:●.X = Don't Care bit.●.Address bit A8 is not decoded by the 93xx56 .
●.Address bit A7 is not decoded by the 93xx56 .

The instruction set of the 93xx46/56/66 devices contains seven instructions,as summarized in the table below.

- Each instruction is preceded by a rising edge on Chip Select Input (CS)with Serial Clock (SK) being held low.
- A start bit,which is the first "1" read on Serial Data Input (DI) during the rising edge of Serial Clock (SK).
- Two op-code bits, read on Serial Data Input (DI) during the rising edge of Serial Clock (SK). (Some instructions also use the first two bits of the address to define the op-code).
- The address bits of the byte or word that is to be accessed. For the 93xx46,the address is made up of 6 bits for the x16 organization or 7 bits for the x8 organization. For the 93xx56nd 93xx66 , the address is made up of 8 bits for the x16 organization or 9 bits for the x8 organization.

Pin Capacitance

Symbol	Parameter	Test Condition	Max	Units
C_{IN} ①	Input Capacitance	VIn=0V,f=1 MHz	6	pF
C_{OUT} ①	Output Capacitance	VouT=OV,f=1 MHz	8	pF

Note: 1.This parameter is characterized and is not 100% tested.

AC Characteristics

Applicable over recommended operating range from: T_A= -40°C to +85 °C , V_{CC}= 1.7V to 5.5V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	1.7V≤Vcc≤2.5V		2.5V<Vcc≤5.5V		Units
		Min	Max	Min	Max	
fsk	SK Clock Frequency		1		2	MHz
tsKL	SK Low Time	250		200		ns
tsKH	SK High Time	250		200		ns
tcs	Minimum CS Low	250		200		ns
tcss	CS Setup Time	50		50		ns
tcsH	CS Hold Time	0		0		ns
tDIs	DI Setup Time	100		50		ns
tDIH	DI Hold Time	100		50		ns
tpD1	Output Delay to "1"		400		200	ns
tpDo	Output Delay to "0"		400		200	ns
tsv.	CS to Status Valid		400		200	ns
tDF.	CS to DO in High		200		100	ns
twR	Write Cycle		5		5	ms
Endurance (1)	3.3V,25℃	1,000,000				Write Cycles

Notes:
1.This parameter is characterized and is not 100% tested.
2.AC measurement conditions:
Input pulse voltages: 0.2 $V_{CC}$to 0.8 V_{CC}
Input rise and fall times: ≤ 50 ns
Input and output timing reference voltages: 0.3 V_{CC}~ 0.7 V_{CC}

DC Characteristics

Applicable over recommended operating range from: TA = -40 ° C to +85 ° C, V_{CC}= +1.7V to +5 .5V, (unless otherwise noted).

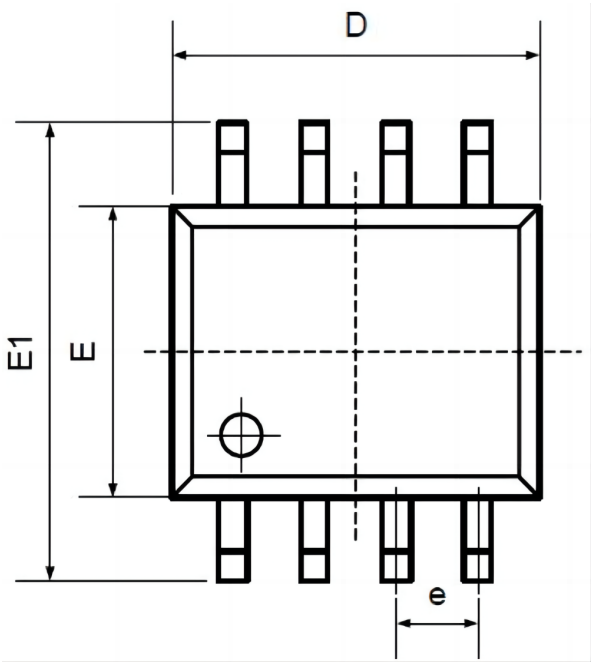
Symbol	Parameter	Test Condition		Min	Max	Units
V_{CC}	Supply Voltage			1.7	5.5	V
I_{CC}	Supply	Vcc=5.0V,fsk=2.0 MHz	CS=VH, DO=open		2.0	mA
		Vcc=1.7V,fsk=1.0 MHz			1.0	mA
I_{SB}	Standby Current	Vcc=5V	CS=SK=GND, ORG=Vcc/GND		15.0	μA
		Vcc=1.7V			2.0	μA
I_{LI}	Input Leakage	OV≤VIn≤Vcc		-1.0	1.0	μA
I_{LO}	Output Leakage	OV≤VouT≤Vcc;DO=Hi-Z		-1.0	1.0	μA
V_{IL} ①	Input Low Voltage			-0.45	0.2Vcc	V
V_{IH} ①	Input High Voltage			0.8Vcc	Vcc+0.5	V
V_{OL}	Output Low Voltage	Vcc=5V	IoL=2.1 mA		0.4	V
		Vcc=1.7V	IoL=100 μA		0.2	V
V_{OH}	Output High Voltage	Vcc=5V	IoH=-400 μA	0.8Vcc		V
		Vcc=1.7V	IoH=-100 μA	Vcc-0.2		V

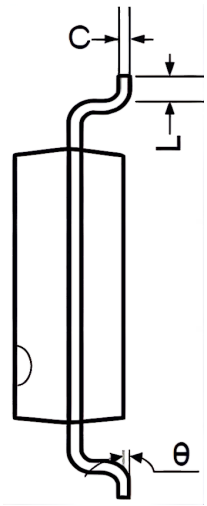
Note: 1.V_{IL} min and V_{IH} max are reference only and are not tested.

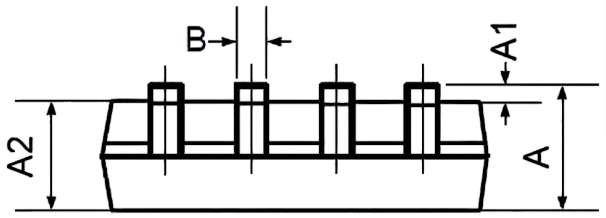
Order information

Order Number	Package	Package Quantity	Word Size	Operating Voltage	ORG Pin	Marking On The park	Temperature
93AA46AT-I/SN-TUDI	SOP8	Tape,Reel,2500	8-bit	1.8-5.5	No	93AA46AI/SN	-40℃ to 85℃
93AA46BT-I/SN-TUDI	SOP8	Tape,Reel,2500	16-bit	1.8-5-5	No	93AA46BI/SN	
93LC46AT-I/SN-TUDI	SOP8	Tape,Reel,2500	8-bit	2.5-5.5	No	93LC46AI/SN	
93LC46BT-I/SN-TUDI	SOP8	Tape,Reel,2500	16-bit	2.5-5.5	No	93LC46BI/SN	
93C46AT-I/SN-TUDI	SOP8	Tape,Reel,2500	8-bit	4.5-5.5	No	93C46AI/SN	
93C46BT-I/SN-TUDI	SOP8	Tape,Reel,2500	16-bit	4.5-5.5	No	93C46BI/SN	
93AA46CT-I/SN-TUDI	SOP8	Tape,Reel,2500	8-or 16-bit	1.8-5.5	Yes	93AA46CI/SN	
93LC46CT-I/SN-TUDI	SOP8	Tape,Reel,2500	8-or 16-bit	2.5-5.5	Yes	93LC46CI/SN	
93C46CT-I/SN-TUDI	SOP8	Tape,Reel,2500	8-or 16-bit	4.5-5.5	Yes	93C46CI/SN	

Package SOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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