

Description

This single 2-input positive-NAND gate is designed for 1.65V to 5.5V V_{CC} operation.

The SN74AHC1G00 performs the Boolean function $Y = A \times B$ or $Y = A + B$ in positive logic.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

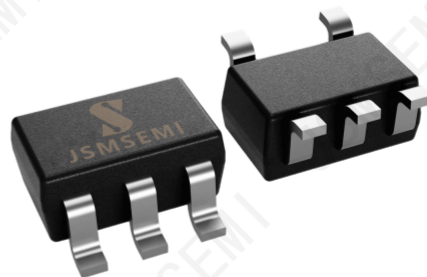
The SN74AHC1G00 is available in Green SOT23-5 and SOT-353 packages. It operates over an ambient temperature range of -40°C to +125°C.

Features

- Low Power Consumption, 1μA Max I_{CC}
- Supports 5V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Provides Down Translation to V_{CC}
- Typ t_{pd} of 5.7ns at 3.3 V
- Low Power Consumption, 1μA Max I_{CC}
- ±24mA Output Drive at 3.0V
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back Drive Protection
- Latch-Up Performance Exceeds 100 mA
- ESD Protection Exceeds JESD 22
 - 2000V Human-Body Model
 - 1000V Charged-Device Model

Applications

- AV Receiver
- Audio Dock: Portable
- Blu-ray Player and Home Theater
- Embedded PC
- MP3 Player/Recorder (Portable Audio)
- Personal Digital Assistant (PDA)



Simplified Schematic



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	H	H
H	L	H
L	L	H

H=High Voltage Level

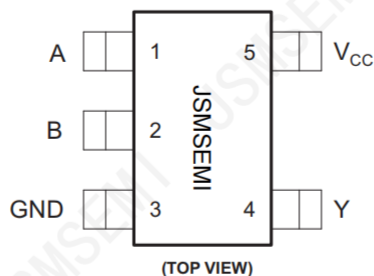
L=Low Voltage Level

- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drive (SSD): Client and Enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Video Analytics: Server
- Wireless Headset, Keyboard, and Mouse

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship,Quantity	Green
SN74AHC1G00DBVR-JSM	SOT-23-5L	C00K	-40 to 125°C	3	TR&3000	Rohs
SN74AHC1G00DCKR-JSM	SOT-353	CA5	-40 to 125°C	3	TR&3000	Rohs

Pin Configuration and Functions



Pin Functions

PIN		DESCRIPTION
NAME	SOT23-5 SOT-353	
A	1	Input
B	2	Input
GND	3	Ground
Y	4	Output
V _{CC}	5	Power pin

Specifications

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	6.5	V
V _I	Input voltage range ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high or low state ^{(2) (3)}	-0.5	V _{CC} +0.5	V
I _{IK}	Input clamp current		-50	mA
I _{OK}	Output clamp current		-50	mA
I _O	Continuous output current		±50	mA
	Continuous current through V _{CC} or GND		±100	mA
T _J	Junction temperature	-65	150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the Recommended Operating Conditions table.

Handling Ratings

			MIN	MAX	UNIT
T _{stg}	Storage temperature range		−65	150	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM)	0	2000	V
		Charged device model (CDM)	0	1000	

Thermal Information

THERMAL METRIC		SN74AHC1G00		UNIT
		5PINS		
		SOT23-5	SOT-353	
R _{ΘJA}	Junction-to-ambient thermal resistance	273.8	214.7	°C/W
R _{ΘJC(top)}	Junction-to-case(top) thermal resistance	126.8	127.1	°C/W
R _{ΘJB}	Junction-to-board thermal resistance	85.9	60.0	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	10.9	33.4	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	84.9	59.8	°C/W
R _{ΘJC(bot)}	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

Recommended Operating Conditions ⁽¹⁾

 over recommended operating free-air temperature range (TYP values are at T_A = +25°C, unless otherwise noted.) ⁽¹⁾

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage	V _{CC}	Operating	1.65	5.5	V
		Data retention only	1.5	5.5	
High-level input voltage	V _{IH}	V _{CC} =1.65V to 1.95V	0.65xV _{CC}		V
		V _{CC} =2.3V to 2.7V	1.7		
		V _{CC} =3V to 3.6V	2.2		
		V _{CC} =4.5V to 5.5V	0.7xV _{CC}		
Low-level input voltage	V _{IL}	V _{CC} =1.65V to 1.95V		0.15xV _{CC}	V
		V _{CC} =2.3V to 2.7V		0.3	
		V _{CC} =3V to 3.6V		0.4	
		V _{CC} =4.5V to 5.5V		0.15xV _{CC}	
Input voltage	V _I		0	5.5	V
Output voltage	V _O		0	V _{CC}	V
Input transition rise or fall	t _r , t _f	V _{CC} =1.8V±0.15V, 2.5V±0.2V		20	ns/V
		V _{CC} =3.3V±0.3V		10	
		V _{CC} =5V±0.5V		5	
Operating temperature	T _A		-40	+125	°C

 (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Electrical Characteristics—DC Limit Changes

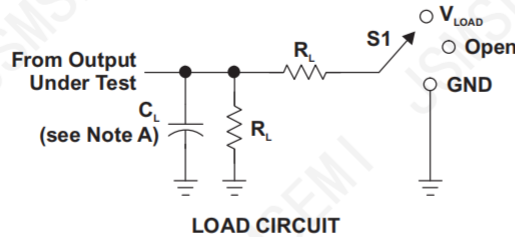
over recommended operating free-air temperature range (Full=-40°C to +125°C, typical values are at T_A= +25°C, unless otherwise noted.)

PARAMETER		TEST CONDITIONS	V _{CC}	TEMP	MIN	TYP	MAX	UNIT
V _{OH}		I _{OH} = -100μA	1.65V to 5.5V	Full	V _{CC} -0.1			V
		I _{OH} = -4mA	1.65V		1.2			
		I _{OH} = -8mA	2.3V		1.9			
		I _{OH} = -16mA	3V		2.4			
		I _{OH} = -24mA			2.3			
		I _{OH} = -32mA	4.5V		3.8			
V _{OL}		I _{OL} = 100μA	1.65V to 5.5V	Full			0.1	V
		I _{OL} = 4mA	1.65V				0.45	
		I _{OL} = 8mA	2.3V				0.3	
		I _{OL} = 16mA	3V				0.4	
		I _{OL} = 24mA					0.55	
		I _{OL} = 32mA	4.5V				0.55	
I _I	A or B inputs	V _I =5.5V or GND	0V to 5.5V	+25°C		±0.1	±1	μA
				Full			±5	
I _{off}		V _I or V _O =5.5V	0	+25°C		±0.1	±1	μA
				Full			±10	
I _{CC}		V _I =5.5V or GND, I _O =0	1.65V to 5.5V	+25°C		0.1	1	μA
				Full			10	
ΔI _{CC}		One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND	3V to 5.5V	Full			500	μA

Electrical Characteristics—AC Limit Changes

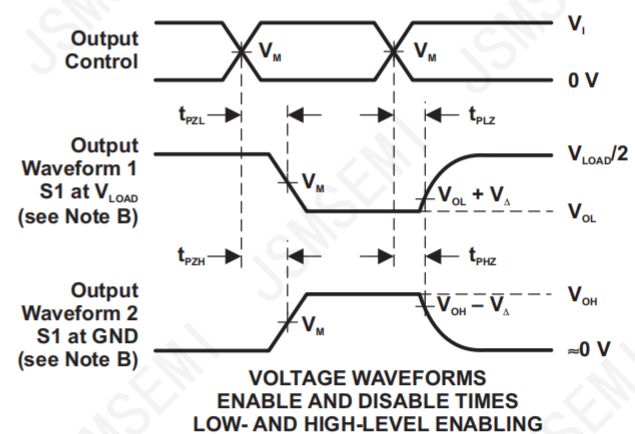
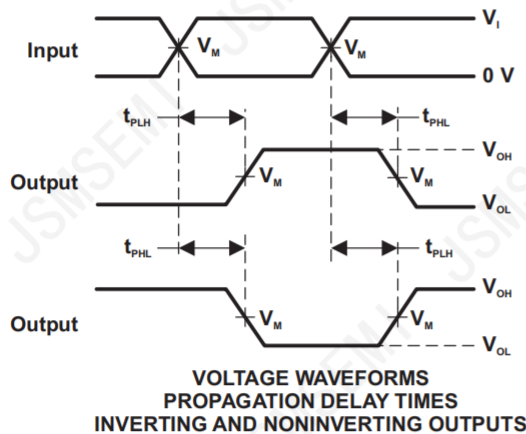
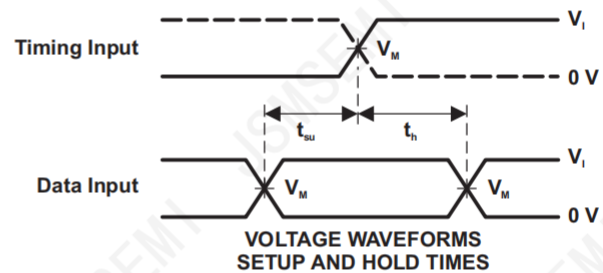
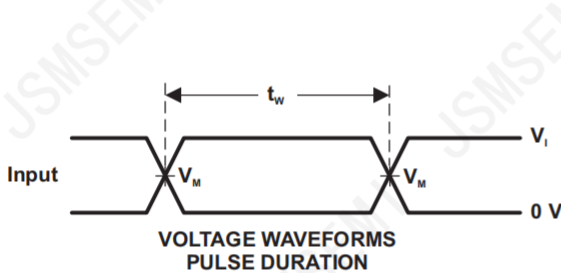
PARAMETER	SYMBOL	TEST CONDITIONS		TEMP	MIN	TYP	MAX	UNIT
Propagation Delay	t _{pd}	V _{CC} =1.8V±0.15V	C _L =30pF, R _L =500Ω	Full		21		ns
		V _{CC} =2.5V±0.2V	C _L =30pF, R _L =500Ω	Full		7.8		
		V _{CC} =3.3V±0.3V	C _L =50pF, R _L =500Ω	Full		5.7		
		V _{CC} =5V±0.5V	C _L =50pF, R _L =500Ω	Full		4.2		
Input Capacitance	C _i	V _{CC} =3.3V	V _I =V _{CC} or GND	+25°C		4		pF
Power dissipation capacitance	C _{pd}	V _{CC} =1.8V	f=10MHz	+25°C		21		pF
		V _{CC} =2.5V				22		
		V _{CC} =3.3V				22		
		V _{CC} =5V				25		

Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L		R_L		V_{Δ}
	V_I	t_r/t_f							
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	15pF	30pF	1M Ω	1k Ω	0.15V
$2.5V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	15pF	30pF	1M Ω	500 Ω	0.15V
$3.3V \pm 0.3V$	3V	$\leq 2.5ns$	1.5V	6V	15pF	50pF	1M Ω	500 Ω	0.3V
$5V \pm 0.5V$	V_{CC}	$\leq 2.5ns$	$V_{CC}/2$	$2 \times V_{CC}$	15pF	50pF	1M Ω	500 Ω	0.3V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dS} .
 - t_{PZL} and t_{PZH} are the same as t_{dM} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

Detailed Description

Overview

The SN74AHC1G00 device contains one 2-input positive-NAND gate and performs the Boolean function $Y = A \times B$ or $Y = \overline{A + B}$. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Functional Block Diagram



Feature Description

- Wide operating voltage range.
 - Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

Device Functional Modes

Function Table

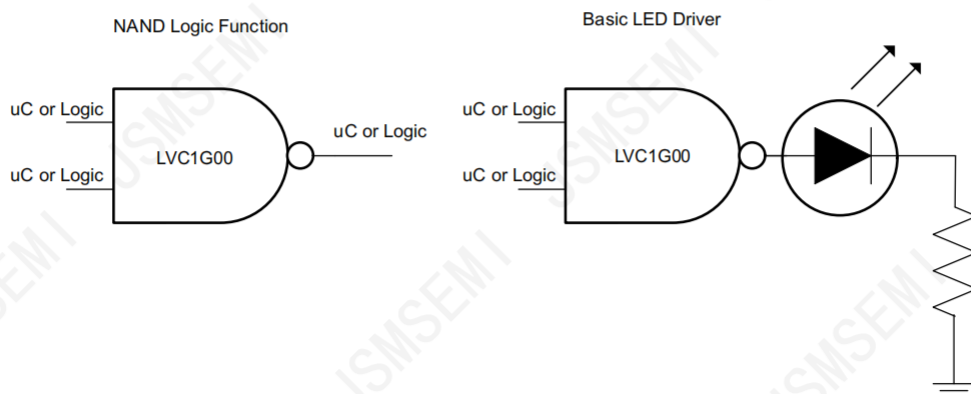
INPUTS		OUTPUT Y
A	B	
H	H	L
L	X	H
X	L	H

Application and Implementation

Application Information

The SN74AHC1G00 is a high drive CMOS device that can be used for implementing NAND logic with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate down to V_{CC} .

Typical Application



Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the Recommended Operating Conditions table.

Each Vcc pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply a 0.1 μ F capacitor is recommended and if there are multiple Vcc pins then a 0.01 μ F or 0.022 μ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1 μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

Layout

Layout Guidelines

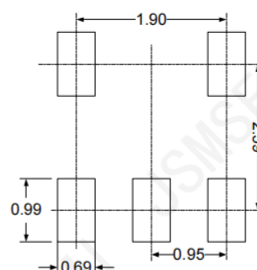
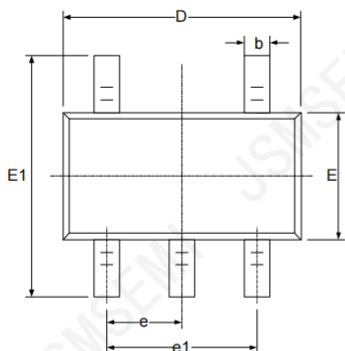
When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to Gnd or Vcc whichever make more sense or is more convenient.

Layout Example

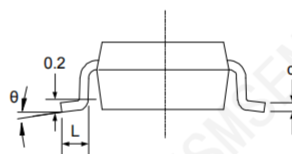
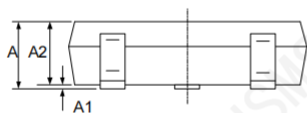


Package Information

SOT-23-5L



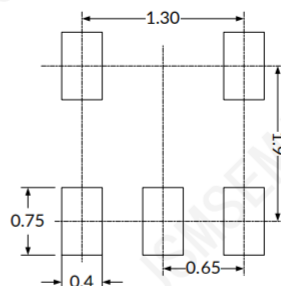
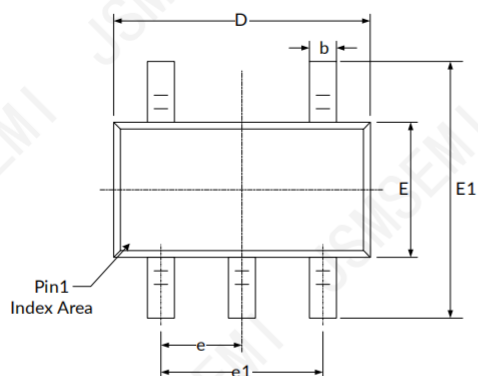
RECOMMENDED LAND PATTERN (Unit: mm)



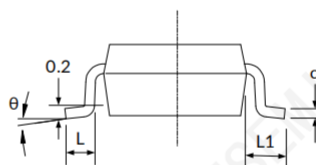
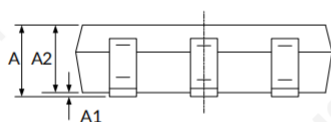
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Package Information

SOT-353(SC70-5)



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D ⁽¹⁾	2.000	2.200	0.079	0.087
E ⁽¹⁾	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650(BSC)		0.026(BSC)	
e1	1.300(BSC)		0.051(BSC)	
L	0.260	0.460	0.010	0.018
L1	0.525		0.021	
θ	0°	8°	0°	8°

Revision History

Rev.	Change	Date
V1.0	Initial version	3/17/2023

Important Notice

JSMSEMI Semiconductor (JSMSEMI) PRODUCTS ARE NEITHER DESIGNED NOR INTENDED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS UNLESS THE SPECIFIC JSMSEMI PRODUCTS ARE SPECIFICALLY DESIGNATED BY JSMSEMI FOR SUCH USE. BUYERS ACKNOWLEDGE AND AGREE THAT ANY SUCH USE OF JSMSEMI PRODUCTS WHICH JSMSEMI HAS NOT DESIGNATED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS IS SOLELY AT THE BUYER' S RISK.

JSMSEMI assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using JSMSEMI products.

Resale of JSMSEMI products or services with statements diferent from or beyond the parameters stated by JSMSEMI for that product or service voids all express and any implied warranties for the associated JSMSEMI product or s ervice. JSMSEMI is not responsible or liable for any such statements.

JSMSEMI All Rights Reserved. Information and data in this document are owned by JSMSEMI wholly and may not be edited, reproduced, or redistributed in any way without the express written consent from JSMSEMI.

Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the JSMSEMI product that you intend to use.

For additional information please contact Kevin@jsmsemi.com or visit www.jsmsemi.com