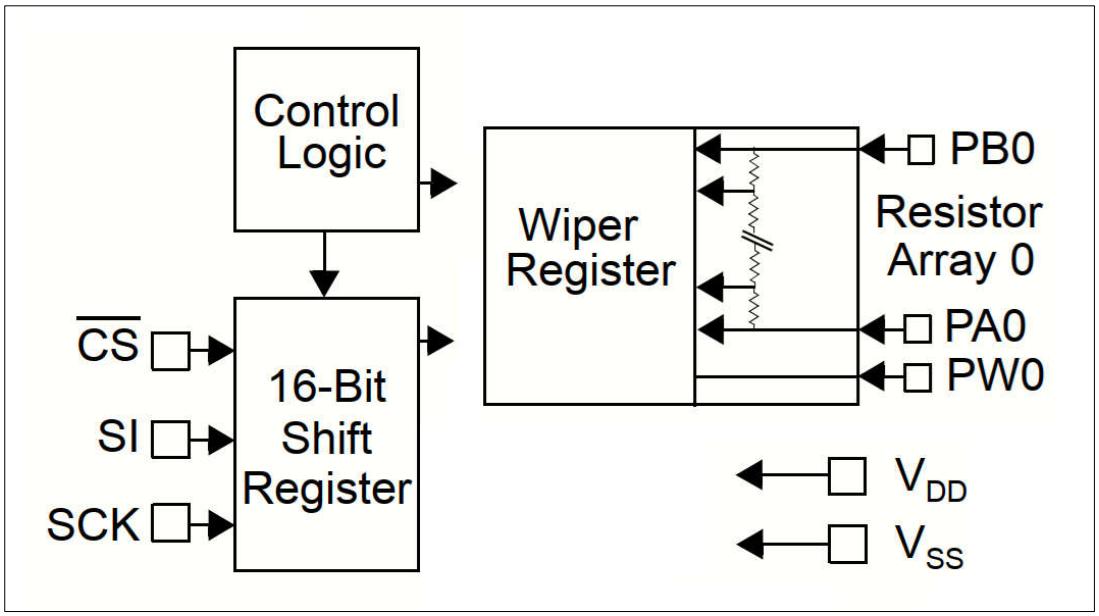
1. DESCRIPTION

The chip XLMCP41010 is a single channel digital potentiometer with 3-wires SPI interface, available in 10 kΩ resistance and 256-positions. The wiper position of the XLMCP41010 varies linearly and is controlled via a 3-wires SPI interface. The device consumes less 1 μA during static operation. A software shut down feature is provided that disconnects the "A" terminal from the resistor stack and simultaneously connects the wiper to the "B" terminal. During shutdown mode, the contents of the wiper register can be changed and the potentiometer returns from shutdown to the new value. The wiper is reset to the mid-scale position (80h) upon power-up. The chip XLMCP41010 operate from a single 2.7V - 5.5V supply and available in DIP8 or SOP8 package.

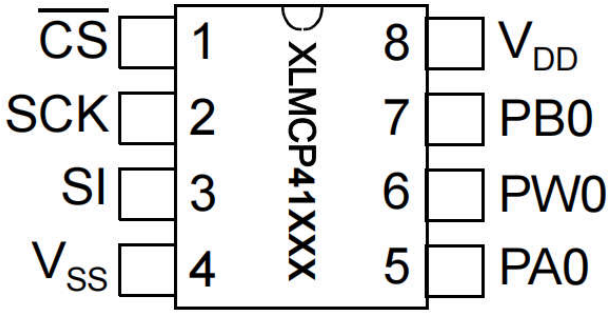
2. FEATURES

- 256 taps
- Potentiometer values for 10 kΩ
- Single channel
- SPI serial interface (mode 0,0 and mode 1,1)
- ±2 LSB max INL & DNL
- Low power CMOS technology
- 1 μA maximum supply current in static operation
- Shutdown feature open circuits of all resistors for maximum power savings
- Single supply operation (2.7V - 5.5V)
- 8-pin PDIP or 8-pin SOIC package option.
- Industrial temperature range: -40°C to +85°C

3. BLOCK DIAGRAM



4. PACKAGE AND PINS DEFINED



(Top view for DIP8 and SOP8 , more details see TABLE 1)

5. ABSOLUTE MAXIMUM RATINGS

V_{DD}.....7.0V

All inputs and outputs w.r.t. VSS ..... -0.6V to V_{DD} +1.0V

Storage temperature .....-60°C to +150°C

Ambient temp. with power applied .....-40°C to +85°C

ESD protection on all pins.....≥ 2 kV

NOTE: Stresses above those listed under "maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

6. ELECTRICAL CHARACTERISTICS

6.1. DC CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.7V to 5.5V, T_A = -40°C to +85°C. Typical specifications represent values for V_{DD} = 5V, V_{SS} = 0V, V_B = 0V, T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Rheostat Mode						
Nominal Resistance	R	8	10	12	kΩ	T_A = +25°C **(Note 1)**
Rheostat Differential Non-Linearity	R-DNL	-2	±1	+2	LSB	**Note 2**
Rheostat Integral Non-Linearity	R-INL	-2	±1	+2	LSB	**Note 2**
Rheostat Tempco	$\Delta R_{AB}/\Delta T$	—	1000	—	ppm/°C	
Wiper Resistance	RW	—	50	105	Ω	V_{DD} = 5.5V, I_W = 1 mA, code 00h
	RW	—	70	130	Ω	V_{DD} = 2.7V, I_W = 1 mA, code 00h
Wiper Current	IW	-1	—	+1	mA	
Potentiometer Divider						
Resolution	N	8	—	—	Bits	
Monotonicity	N	8	—	—	Bits	
Differential Non-Linearity	DNL	-2	±1	+2	LSB	**Note 3**
Integral Non-Linearity	INL	-2	±1	+2	LSB	**Note 3**
Voltage Divider Tempco	$\Delta V_W/\Delta T$	—	1	—	ppm/°C	Code 80h
Full Scale Error	V_{WFSE}	-2	-0.8	0	LSB	Code FFh, V_{DD} = 5V, see Figure 22
	V_{WFSE}	-2	-0.8	0	LSB	Code FFh, V_{DD} = 3V, see Figure 22
Zero Scale Error	V_{WZSE}	0	+0.8	+2	LSB	Code 00h, V_{DD} = 5V, see Figure 22
	V_{WZSE}	0	+0.8	+2	LSB	Code 00h, V_{DD} = 3V, see Figure 22
Resistor Terminals						
Voltage Range	$V_{A,B,W}$	0	—	V_{DD}		**Note 4**
Capacitance (CAor CB)		—	20	—	pF	f = 1 MHz, Code = 80h, see Figure 27
Capacitance	C_W	—	8	—	pF	f = 1 MHz, Code = 80h, see Figure 27
Dynamic Characteristics (All dynamic characteristics use V_{DD} = 5V)						
Bandwidth -3dB	BW	—	1	—	MHz	V_B = 0V, Measured at Code 80h, Output Load = 30pF
Settling Time	t_S	—	5	—	µS	V_A = V_{DD}, V_B = 0V, ±1% Error Band, Transition from Code 00h to Code 80h, Output Load = 30pF
Resistor Noise Voltage	e_{NWB}	—	20	—	nV/√Hz	V_A = Open, Code 80h, f =1 kHz
Crosstalk	C_T	—	-90	—	dB	V_A = V_{DD}, VB = 0V **(Note 5)**
Power Requirements						
Operating Voltage Range	V_{DD}	2.7	—	5.5	V	
Supply Current, Active	I_{DDA}	—	300	600	µA	V_{DD} = 5.5V, $\overline{CS}$ = V_{SS}, f_{SCK} = 10 MHz, SO = Open, Code FFh **(Note 6)**
Supply Current, Static	I_{DDS}	—	0.1	1	µA	$\overline{CS}$ = V_{DD}= 5.5V,SO = Open **(Note 6)**
Power Supply Sensitivity	PSS	—	0.003	0.006	%/%	V_{DD} = 4.5V - 5.5V, V_A = 4.5V, Code 80h
	PSS	—	0.003	0.006	%/%	V_{DD} = 2.7V - 3.3V, V_A = 2.7V, Code 80h

Note

1: VAB = VDD, no connection on wiper.

2: Rheostat position non-linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. IW = 50 µA for VDD = 3V and IW = 400 µA for VDD = 5V for 10 kΩ version. See Figure 23 for test circuit.

3: INL and DNL are measured at VW with the device configured in the voltage divider or potentiometer mode. VA = VDD and VB = 0V. DNL specification limits of ±1 LSB max are specified monotonic operating conditions. See Figure 22 for test circuit.

4: Resistor terminals A,B and W have no restrictions on polarity with respect to each other. Full-scale and zero-scale error were measured using Figure 22.

5: Measured at VW pin where the voltage on the adjacent VW pin is swinging full-scale.

6: Supply current is independent of current through the potentiometers.

6.2. AC TIMING CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.7V to 5.5V, T_A = -40°C to +85°C.						
Parameter	**Sym**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Clock Frequency	F_{CLK}	—	—	10	MHz	V_{DD} = 5.0V
Clock High Time	t_{HI}	40	—	—	ns	
Clock Low Time	t_{LO}	40	—	—	ns	
$\overline{CS}$ Fall to First Rising CLK Edge	t_{CSSR}	40	—	—	ns	
Data Input Setup Time	t_{SU}	40	—	—	ns	
Data Input Hold Time	t_{HD}	10	—	—	ns	
SCK Rise to $\overline{CS}$ Rise Hold Time	t_{CHS}	30	—	—	ns	
SCK Rise to $\overline{CS}$ Fall Delay	t_{CS0}	10	—	—	ns	
$\overline{CS}$ Rise to CLK Rise Hold	t_{CS1}	100	—	—	ns	
$\overline{CS}$ High Time	t_{CSH}	40	—	—	ns	

6.3. Parametric Test Circuits

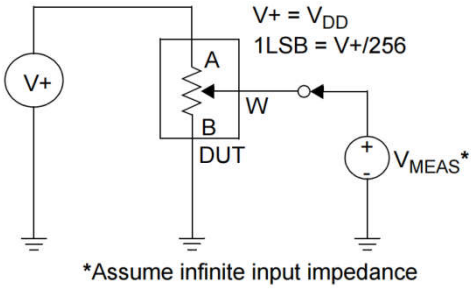


Figure 22: Potentiometer Divider Non-Linearity Error Test Circuit (DNL, INL).

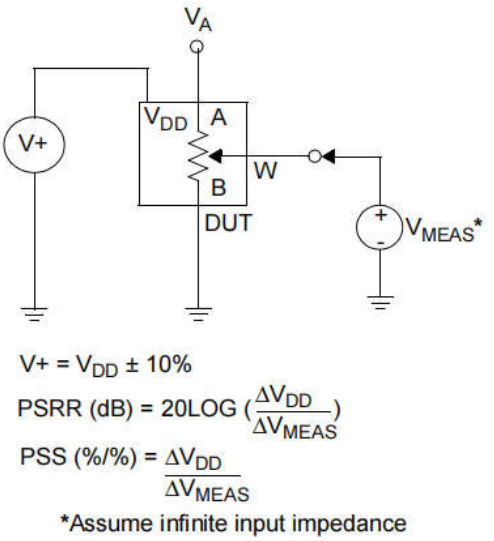


Figure 25: Power Supply Sensitivity Test Circuit (PSS, PSRR).

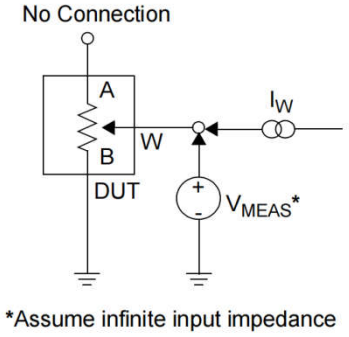


Figure 23: Resistor Position Non-Linearity Error Test Circuit (Rheostat operation DNL, INL).

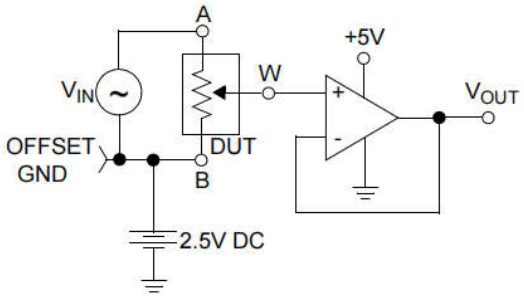


Figure 26: Gain vs. Frequency Test Circuit.

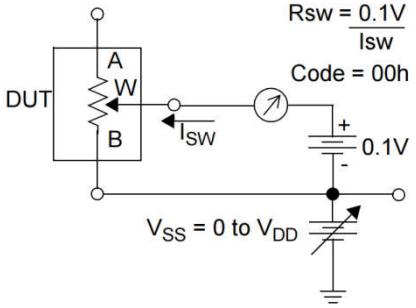


Figure 24: Wiper Resistance Test Circuit.

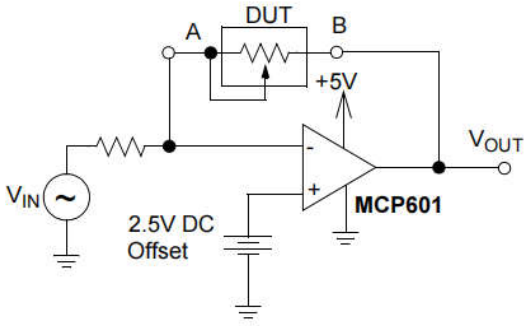


Figure 27: Capacitance Test Circuit.

7. PIN DESCRIPTIONS

7.1. PA0

Potentiometer Terminal A Connection.

7.2. PB0

Potentiometer Terminal B Connection.

7.3. PW0

Potentiometer Wiper Connection.

7.4. Chip Select ($\overline{CS}$)

This is the SPI port chip select pin and is used to execute a new command after it has been loaded into the shift register. This pin has a Schmitt Trigger input.

7.5. Serial Clock (SCK)

This is the SPI port clock pin and is used to clock-in new register data. Data is clocked into the SI pin on the rising edge of the clock and out the SO pin on the falling edge of the clock. This pin is gated to the $\overline{CS}$ pin (i.e., the device will not draw any more current if the SCK pin is toggling when the $\overline{CS}$ pin is high). This pin has a Schmitt Trigger input.

7.6. Serial Data Input (SI)

This is the SPI port serial data input pin. The command and data bytes are clocked into the shift register using this pin. This pin is gated to the $\overline{CS}$ pin (i.e., the device will not draw any more current if the SI pin is toggling when the $\overline{CS}$ pin is high). This pin has a Schmitt Trigger input.

TABLE 1: XLMCP41010 Pins

Pin #	Name	Function
1	$\overline{CS}$	Chip Select
2	SCK	Serial Clock
3	SI	Serial Data Input
4	VSS	Ground
5	PA0	Terminal A Connection Of Potentiometer
6	PW0	Wiper Connection Of Potentiometer
7	PB0	Terminal B Connection Of Potentiometer
8	VDD	Power Supply 2.7V ~ 5.5V

7.7. Modes of Operation

The XLMCP4010 digital potentiometer applications can be divided into two categories: rheostat mode and potentiometer or voltage divider mode.

7.7.1. RHEOSTAT MODE

In the rheostat mode, the potentiometer is used as a two-terminal resistive element. The unused terminal should be tied to the wiper, as shown in Figure 28. Note that reversing the polarity of the A and B terminals will not affect operation

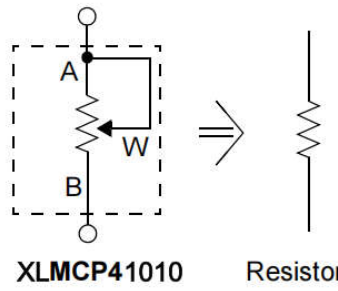


Figure 28: Two-terminal or rheostat configuration for the digital potentiometer. Acting as a resistive element in the circuit, resistance is controlled by changing the wiper setting.

Using the device in this mode allows control of the total resistance between the two nodes. The total measured resistance would be the least at code 00h, where the wiper is tied to the B terminal. The resistance at this code is equal to the wiper resistance, typically 50Ω. The LSB size would be about 39.0625Ω .The resistance would then increase with this LSB size until the total measured resistance at code FFh would be about 9985.94Ω. The wiper will never directly connect to the A terminal of the resistor stack.

In the 00h state, the total resistance is the wiper resistance. To avoid damage to the internal wiper circuitry in this configuration, care should be taken to ensure the current flow never exceeds 1 mA.

7.7.2. POTENTIOMETER MODE

In the potentiometer mode, all three terminals of the device are tied to different nodes in the circuit. This allows the potentiometer to output a voltage proportional to the input voltage. This mode is sometimes called voltage divider mode. The potentiometer is used to provide a variable voltage by adjusting the wiper position between the two endpoints as shown in Figure 29. Note that reversing the polarity of the A and B terminals will not affect operation.

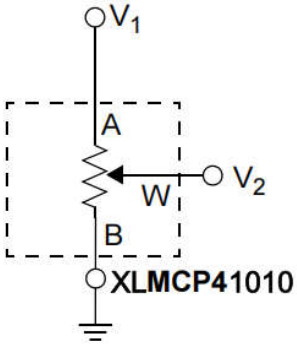
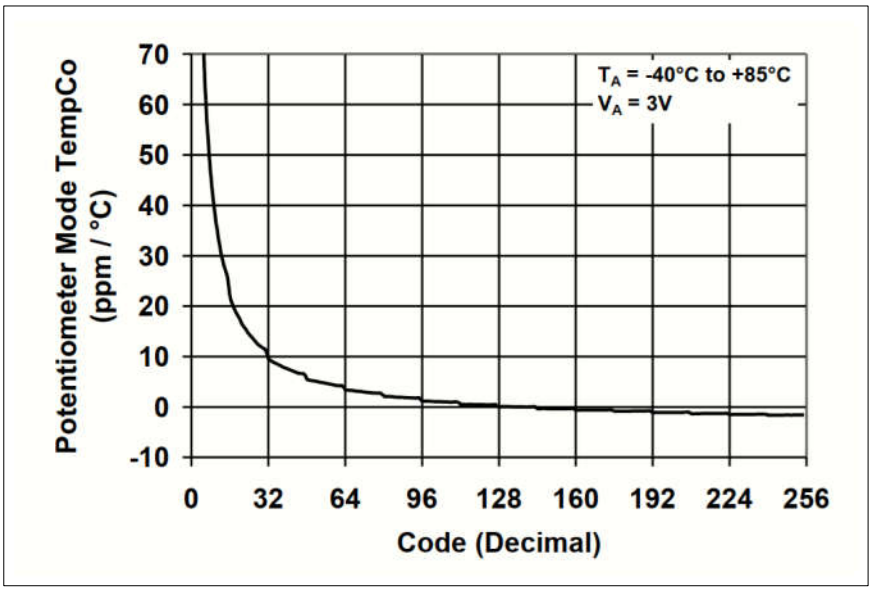


Figure 29: Three terminal or voltage divider mode.

In this configuration, the ratio of the internal resistance defines the temperature coefficient of the device. The resistor matching of the RWB resistor to the RAB resistor performs with a typical temperature coefficient of 1 ppm/°C (measured at code 80h). At lower codes, the wiper resistance temperature coefficient will dominate. The following curve shows the effect of the wiper. Above the lower codes, this Figure shows that 70% of the states will typically have a temperature coefficient of less than 5 ppm/°C. 30% of the states will typically have a ppm/°C of less than 1.



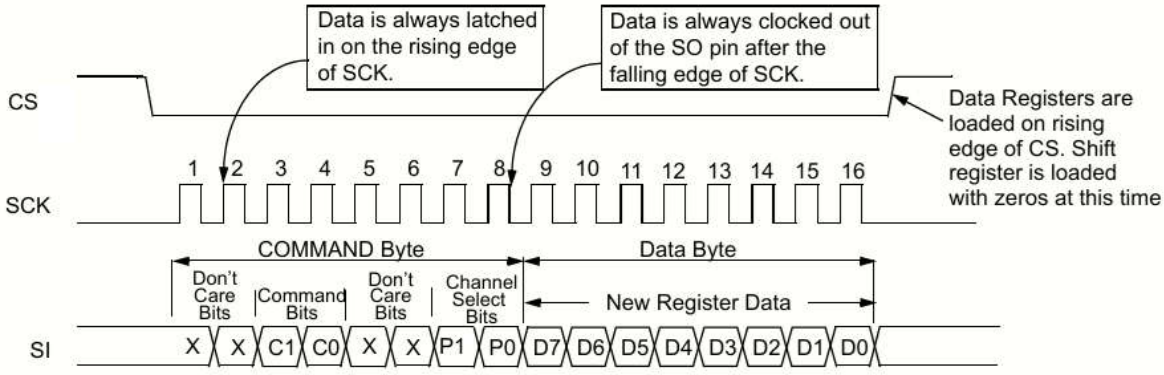
(Potentiometer Mode Tempco vs. Code)

8. SERIAL INTERFACE

Communications from the controller to the XLMCP41010 digital potentiometers is accomplished using a 3-wire SPI serial interface. This interface allows three commands:

1. Write a new value to the potentiometer data register(s).
2. Cause a channel to enter low power shutdown mode.
3. NOP (No Operation) command.

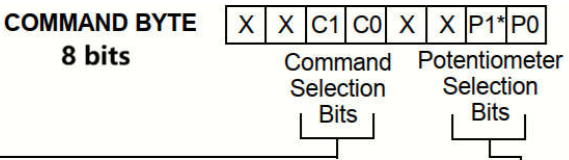
Executing any command is accomplished by setting $\overline{CS}$ low and then clocking-in a command byte followed by a data byte into the 16-bit shift register. The command is executed when $\overline{CS}$ is raised. Data is clocked-in on the rising edge of clock (see Figure 8-0). The device will track the number of clocks (rising edges) while CS is low and will abort all commands if the number of clocks is not a multiple of 16.



(Figure 8-0. Timing Diagram for Writing Instructions or Data to a Digital Potentiometer.)

8.1. Command Byte

The first byte sent is always the command byte, followed by the data byte. The command byte contains two command select bits and two potentiometer select bits. Unused bits are 'don't care' bits. The command select bits C1 and C0 (bits 4:5) of the command byte determine which command will be executed. If the command bits are both 0's or 1's, then a NOP command will be executed once all 16 bits have been loaded. When the command bits are 0,1, a write command will be executed with the 8 bits sent in the data byte. The data will be written to the potentiometer(s) determined by the potentiometer select bits. If the command bits are 1,0, then a shutdown command will be executed on the potentiometers determined by the potentiometer select bits.



C1	C0	Command	Command Summary
0	0	None	No Command will be executed.
0	1	Write Data	Write the data contained in Data Byte to the potentiometer(s) determined by the potentiometer selection bits.
1	0	Shutdown	Potentiometer(s) determined by potentiometer selection bits will enter Shutdown Mode. Data bits for this command are 'don't cares'.
1	1	None	No Command will be executed.

P1*	P0	Potentiometer Selections
0	0	Dummy Code: Neither Potentiometer affected.
0	1	Command executed on Potentiometer 0.
1	0	Command executed on Potentiometer 0.
1	1	Command executed on Potentiometer 0.

8.2. Using the XLMCP41010 in SPI Mode 1,1

It is possible to operate the devices in SPI modes 0,0 and modes 1,1. The only difference between these two modes is that, when using mode 1,1, the clock idles in the high state, while in mode 0,0, the clock idles in the low state. In both modes, data is clocked into the devices on the rising edge of SCK. Operations using mode 0,0 are shown in Figure 8-0. The example in Figure 8-2 shows mode 1,1.

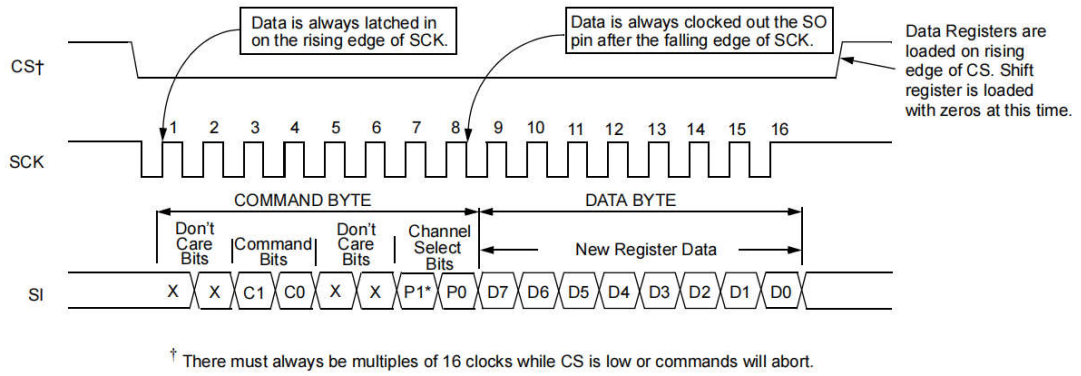


Figure 8-2: Timing Diagram for SPI Mode 1,1 Operation.

9. TYPICAL APPLICATIONS

9.1.1. PROGRAMMABLE SINGLE-ENDED AMPLIFIERS

Potentiometers are often used to adjust system reference levels or gain. Programmable gain circuits using digital potentiometers can be realized in a number of different ways. An example of a single-supply, inverting gain amplifier is shown in Figure 30. Due to the high input impedance of the amplifier, the wiper resistance is not included in the transfer function. For a single-supply, non-inverting gain configuration, the circuit in Figure 31 can be used.

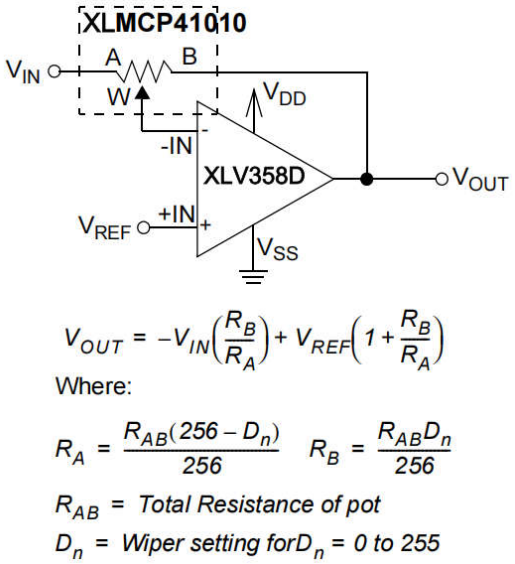


Figure 30: Single-supply, programmable, inverting gain amplifier using a digital potentiometer.

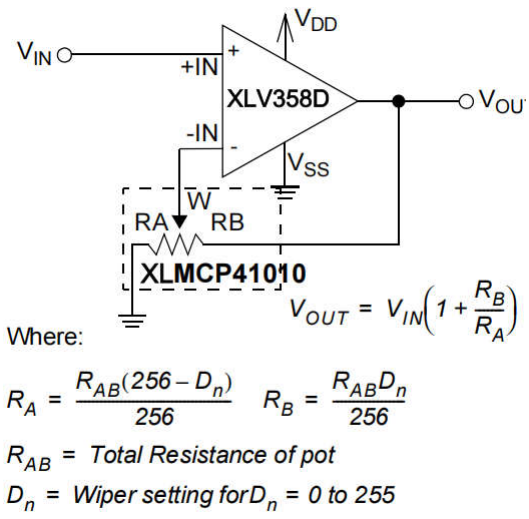


Figure 31: Single-supply, programmable, non-inverting gain amplifier.

In order for these circuits to work properly, care must be taken in a few areas. For linear operation, the analog input and output signals must be in the range of VSS to VDD for the potentiometer and input and output rails of the op-amp. The circuit in Figure 30 requires a virtual ground or reference input to the non-inverting input of the amplifier. At power-up or reset (RS), the resistance is set to mid-scale, with RA and RB matching. Based on the transfer function for the circuit, the gain is -1 V/V. As the code is increased and the wiper moves towards the A terminal, the gain increases. Conversely, when the wiper is moved towards the B terminal, the gain decreases. Figure 32 shows this relationship. Notice the pseudo-logarithmic gain around decimal code 128. As the wiper approaches either terminal, the step size in the gain calculation increases dramatically. Due to the mismatched ratio of RA and RB at the extreme high and low codes, small increments in wiper position can dramatically affect the gain. As shown in Figure 29, recommended gains lie between 0.1 and 10 V/V.

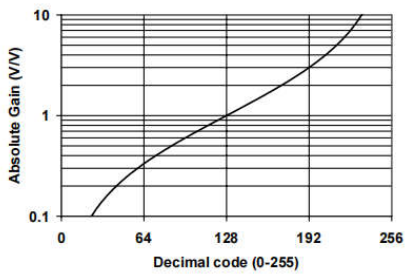


Figure 32: Gain vs. Code for inverting and differential amplifier circuits.

9.1.2. PROGRAMMABLE DIFFERENTIAL AMPLIFIER

An example of a differential input amplifier using digital potentiometers is shown in Figure 33. For the transfer function to hold, both pots must be programmed to the same code. Figure 32 also shows the relationship between gain and code for this circuit. As the wiper approaches either terminal, the step size in the gain calculation increases dramatically. This circuit is recommended for gains between 0.1 and 10 V/V.

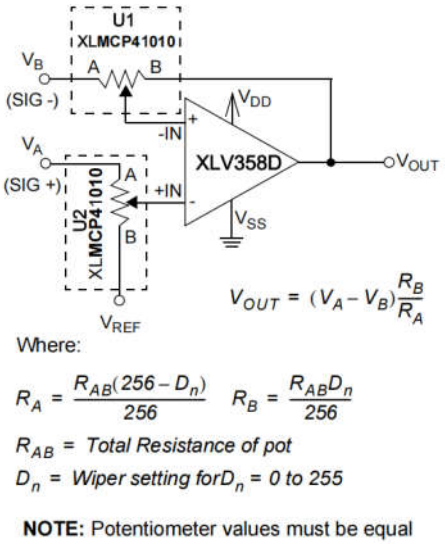


Figure 33: Single Supply programmable differential amplifier using digital potentiometers.

9.1.3. PROGRAMMABLE OFFSET TRIM

For applications requiring only a programmable voltage reference, the circuit in Figure 34 can be used. This circuit shows the device used in the potentiometer mode along with two resistors and a buffered output. This creates a circuit with a linear relationship between voltage-out and programmed code. Resistors R1 and R2 can be used to increase or decrease the output voltage step size. The potentiometer in this mode is stable over temperature. The operation of this circuit over temperature is shown in Figure 6. The worst performance over temperature will occur at the lower codes due to the dominating wiper resistance. R1 and R2 can also be used to affect the boundary voltages, thereby eliminating the use of these lower codes.

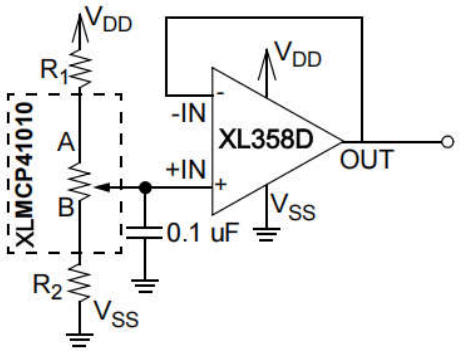
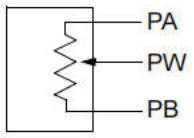


Figure 34: By changing the values of R1 and R2, the voltage output resolution of this programmable voltage reference circuit is affected

9.1.4. Calculating Resistances

When programming the digital potentiometer settings, the following equations can be used to calculate the resistances. Programming code 00h effectively brings the wiper to the B terminal, leaving only the wiper resistance. Programming higher codes will bring the wiper closer to the A terminal of the potentiometer. The equations in Figure 35 can be used to calculate the terminal resistances. Figure 36 shows an example calculation using a 10 kΩ potentiometer.

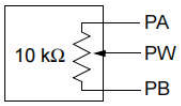


$$R_{WA}(D_n) = \frac{(R_{AB})(256 - D_n)}{256} + R_W$$

$$R_{WB}(D_n) = \frac{(R_{AB})(D_n)}{256} + R_W$$

Where:
PA is the A terminal
PB is the B terminal
PW is the wiper terminal
R_{WA} is resistance between Terminal A and wiper
R_{WB} is resistance between Terminal B and Wiper
R_{AB} is overall resistance for pot (10 kΩ, 50 kΩ or 100 kΩ)
R_W is wiper resistance
D_n is 8-bit value in data register for pot number n

Figure 35:Potentiometer resistances are a function of code. It should be noted that, when using these equations for most feedback amplifier circuits (see Figure 30 and Figure 31), the wiper resistance can be omitted due to the high impedance input of the amplifier.



Example:
R = 10 kΩ
Code = C0h = 192d

$$R_{WA}(D_n) = \frac{(R_{AB})(256 - D_n)}{256} + R_W$$

$$R_{WA}(C0h) = \frac{(10k\Omega)(256 - 192)}{256} + 52\Omega$$

$$R_{WA}(C0h) = 2552\Omega$$

$$R_{WB}(D_n) = \frac{(R_{AB})(D_n)}{256} + R_W$$

$$R_{WB}(C0h) = \frac{(10k\Omega)(192)}{256} + 52\Omega$$

$$R_{WB}(C0h) = 7552\Omega$$

Note: All values shown are typical and actual results will vary.

Figure 36: Example Resistance calculations.

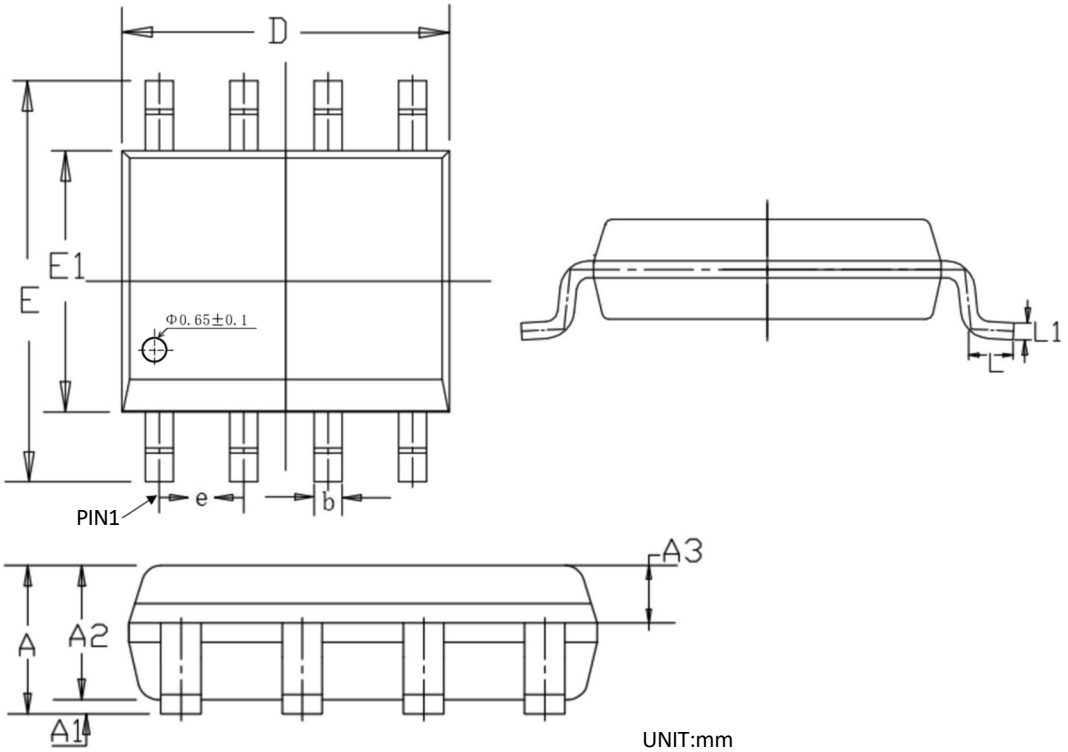
10. ORDERING INFORMATION

Ordering Information

Part Number	Device Making	Package type	Body size (mm)	Temperate (℃)	MSL	Transpo Rt	Package Quantit
XLMCP41010T-I/SN	XL41010	SOP-8	4.90*3.90	-40 to +85	MSL3	T&R	2500
XLMCP41010-E/P	XL41010P	DIP-8	9.25*6.38	-40 to +85	MSL3	T&R	2000

11. DIMENSIONAL DRAWINGS

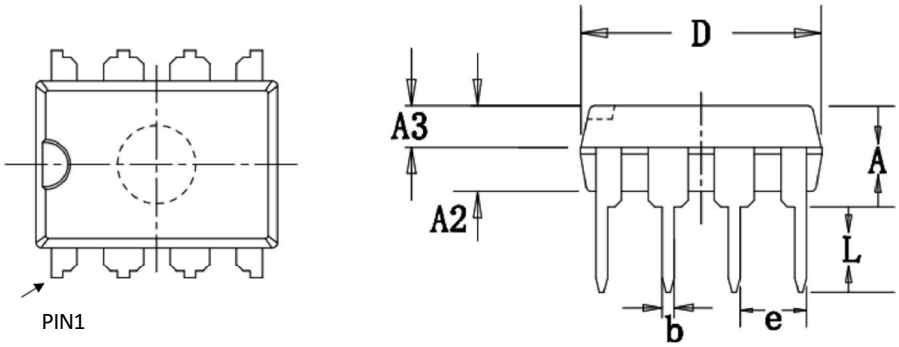
SOP8

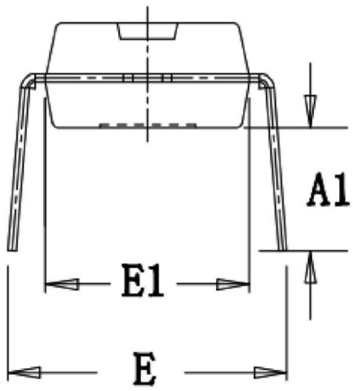


UNIT:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.450	0.600	0.750
L1	—	0.25BSC	—

DIP8





UNIT:mm

	MIN	NOM	MAX
A	3.600	3.800	4.000
A1	3.786	3.886	3.986
A2	3.200	3.300	3.400
A3	1.550	1.600	1.650
b	0.440	–	0.490
e	2.510	2.540	2.570
D	9.150	9.250	9.350
E	7.800	8.500	9.200
E1	6.280	6.380	6.480
L	3.000	–	–